Compute Node Status and Upgrade

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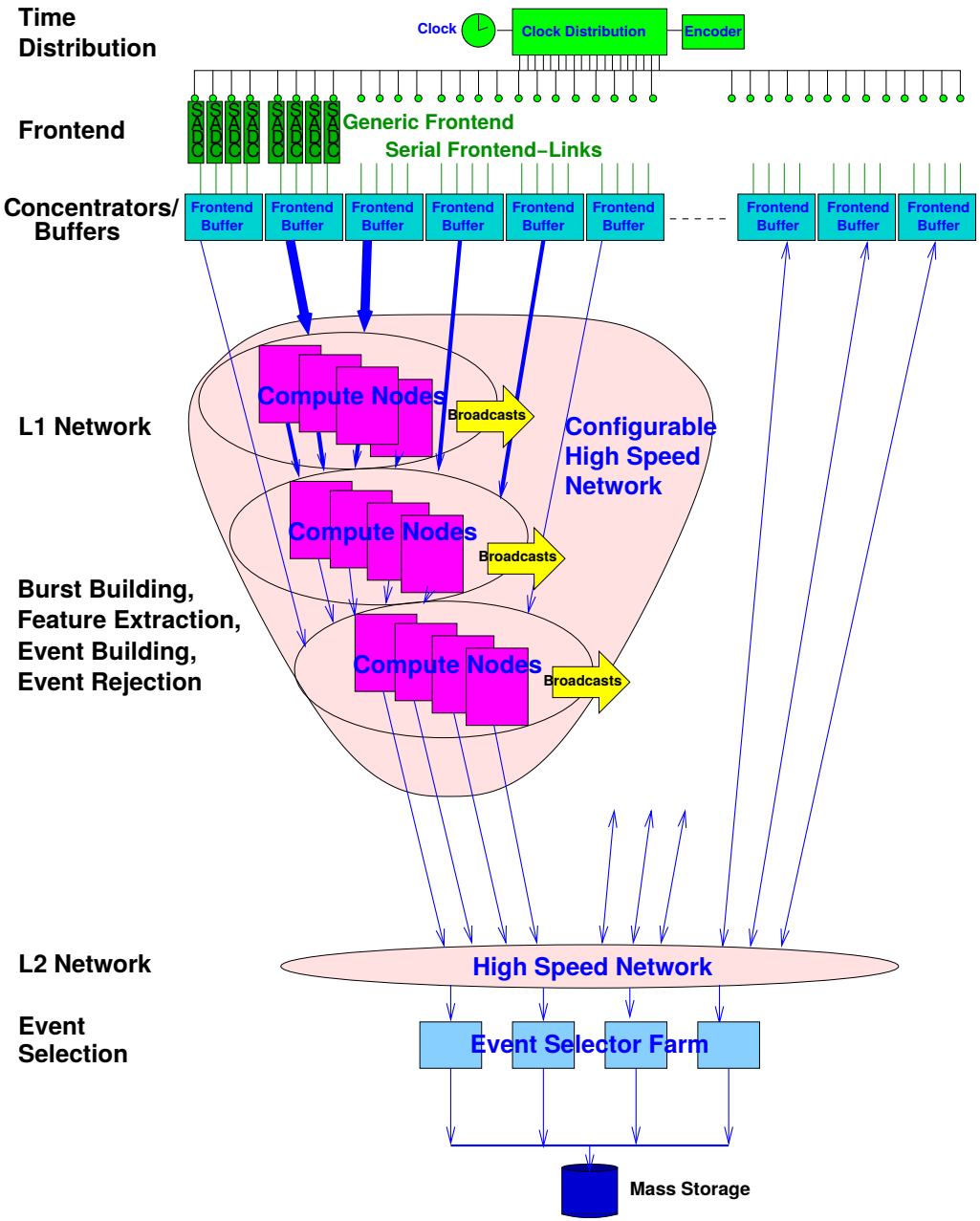
PANDA LIX. Collaboration Meeting

December 7, 2016
GSI

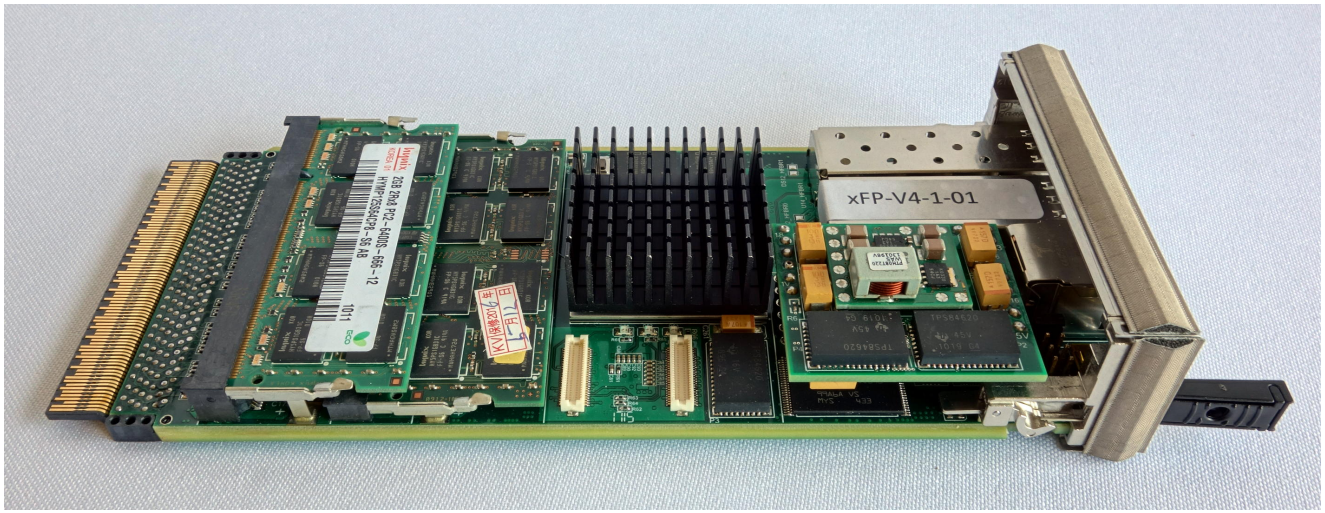
PANDA DAQ/Event Filter

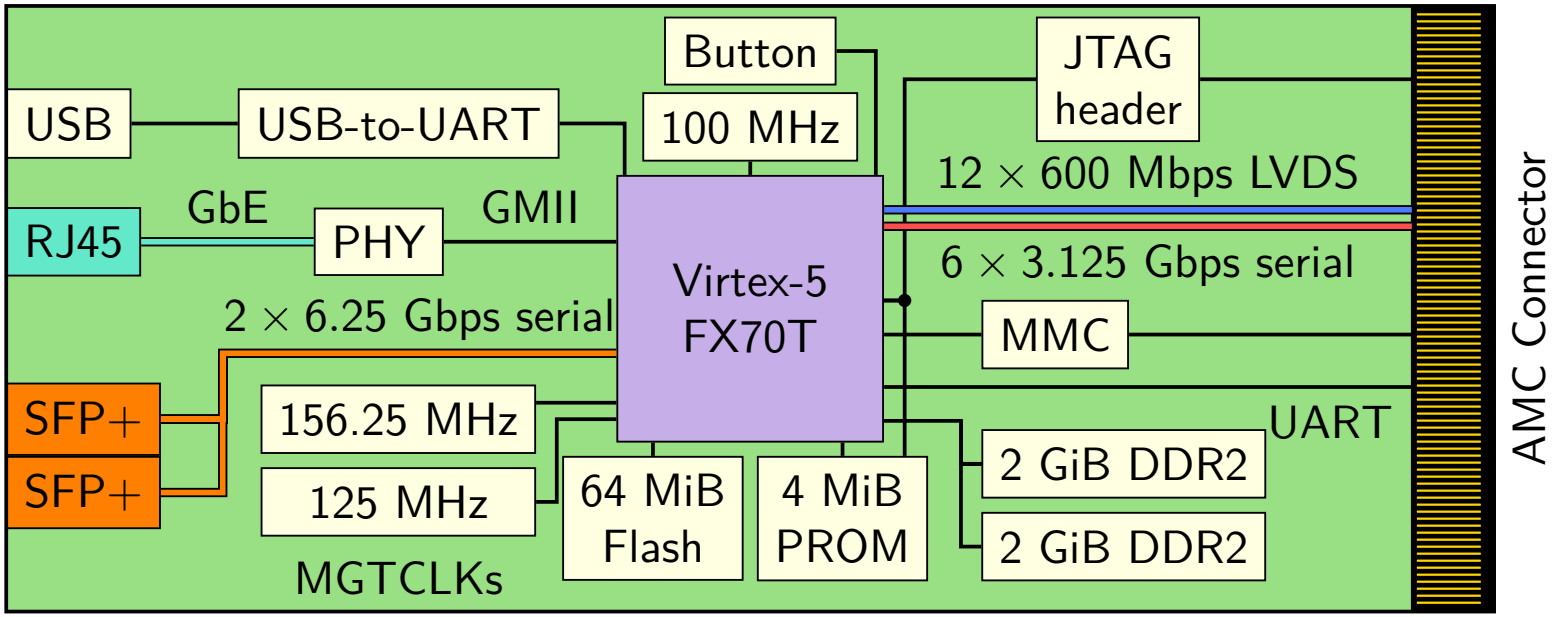


FPGA based

PC/GPU-farm based

xFP (xTCA-Based FPGA Processor) v4.0 (Nov 2014)





CNCB (Compute Node Carrier Board) v3.3 (May 2015)

- Virtex-4 FX60 FPGA as switch to ATCA backplane
- Four full-width AMC slots

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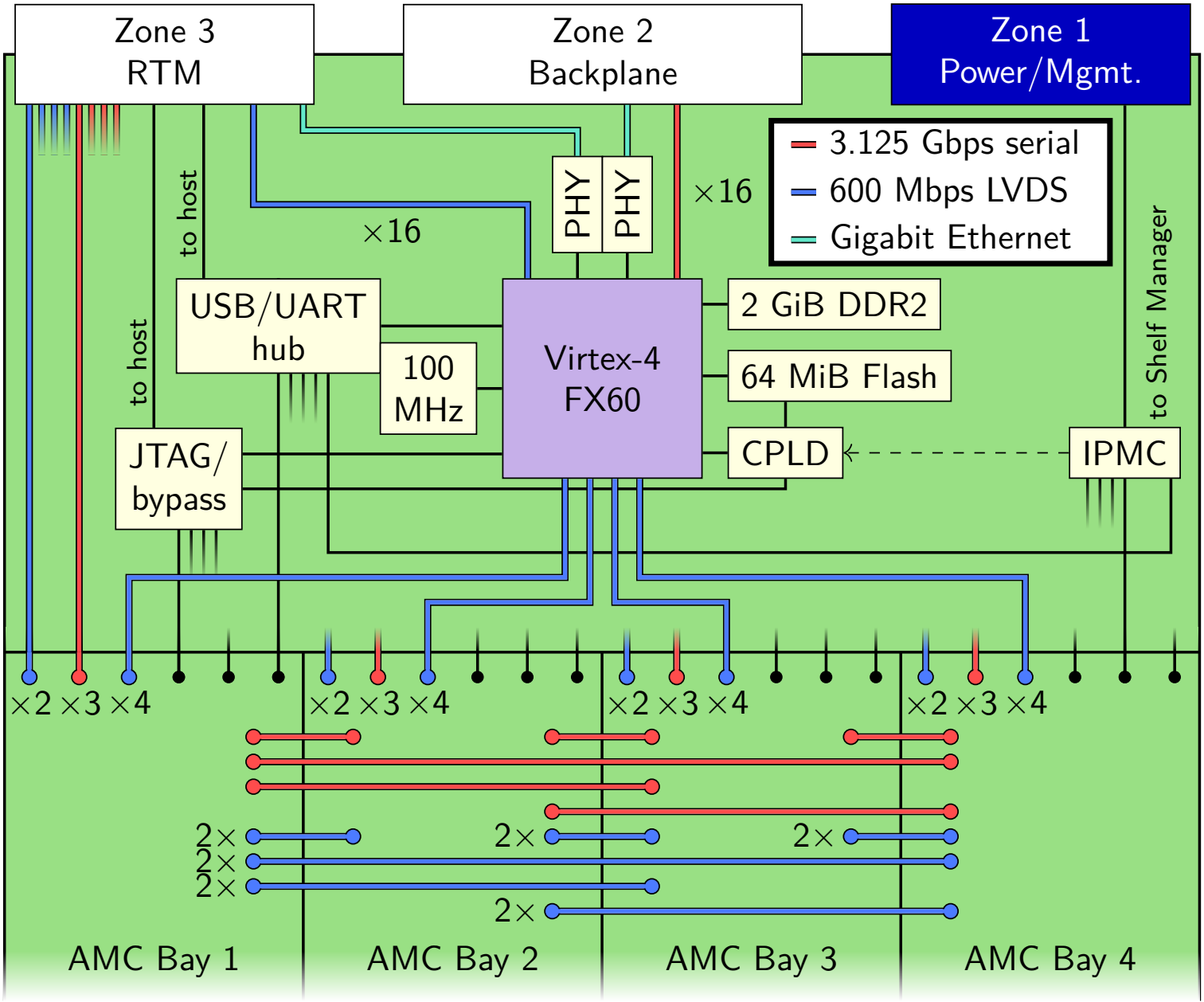
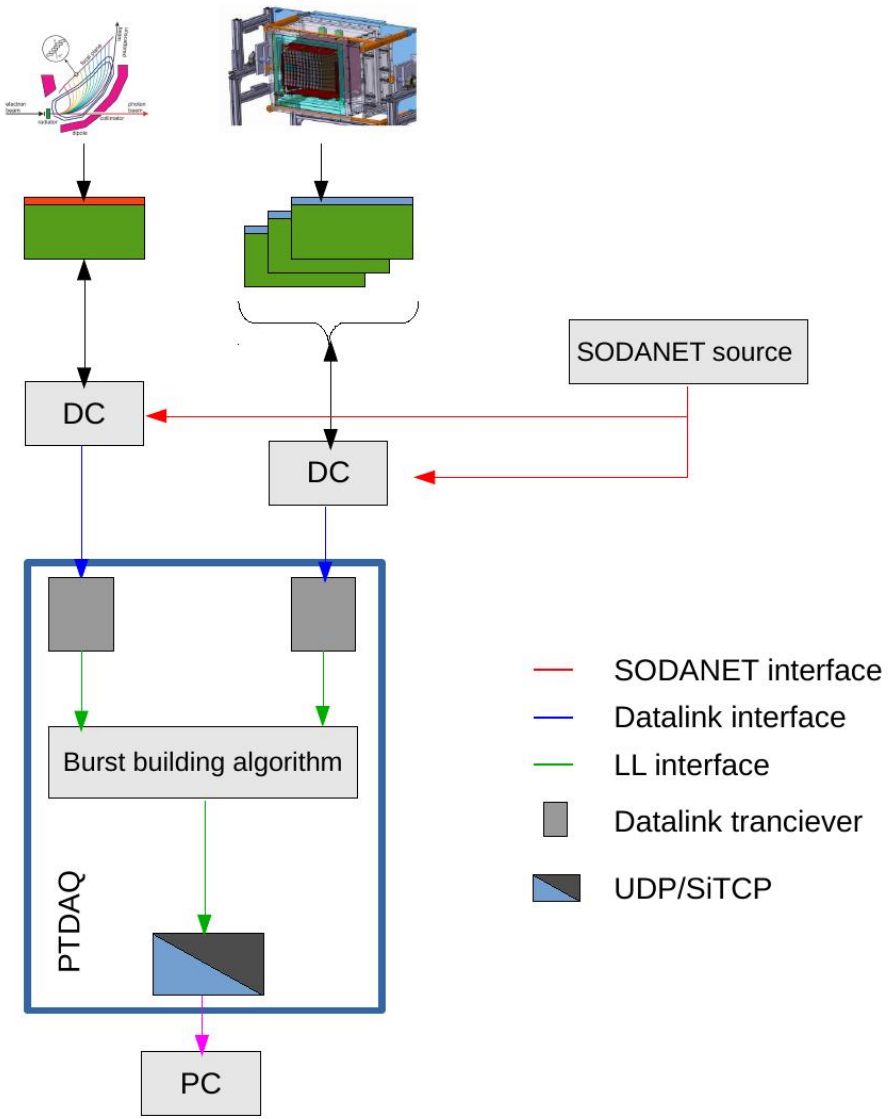


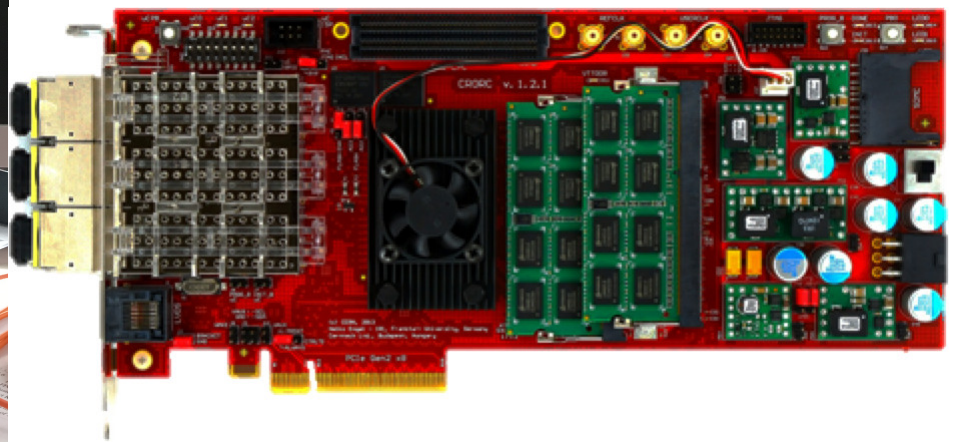
Compute Nodes in the ATCA Shelf

Prototype triggerless DAQ



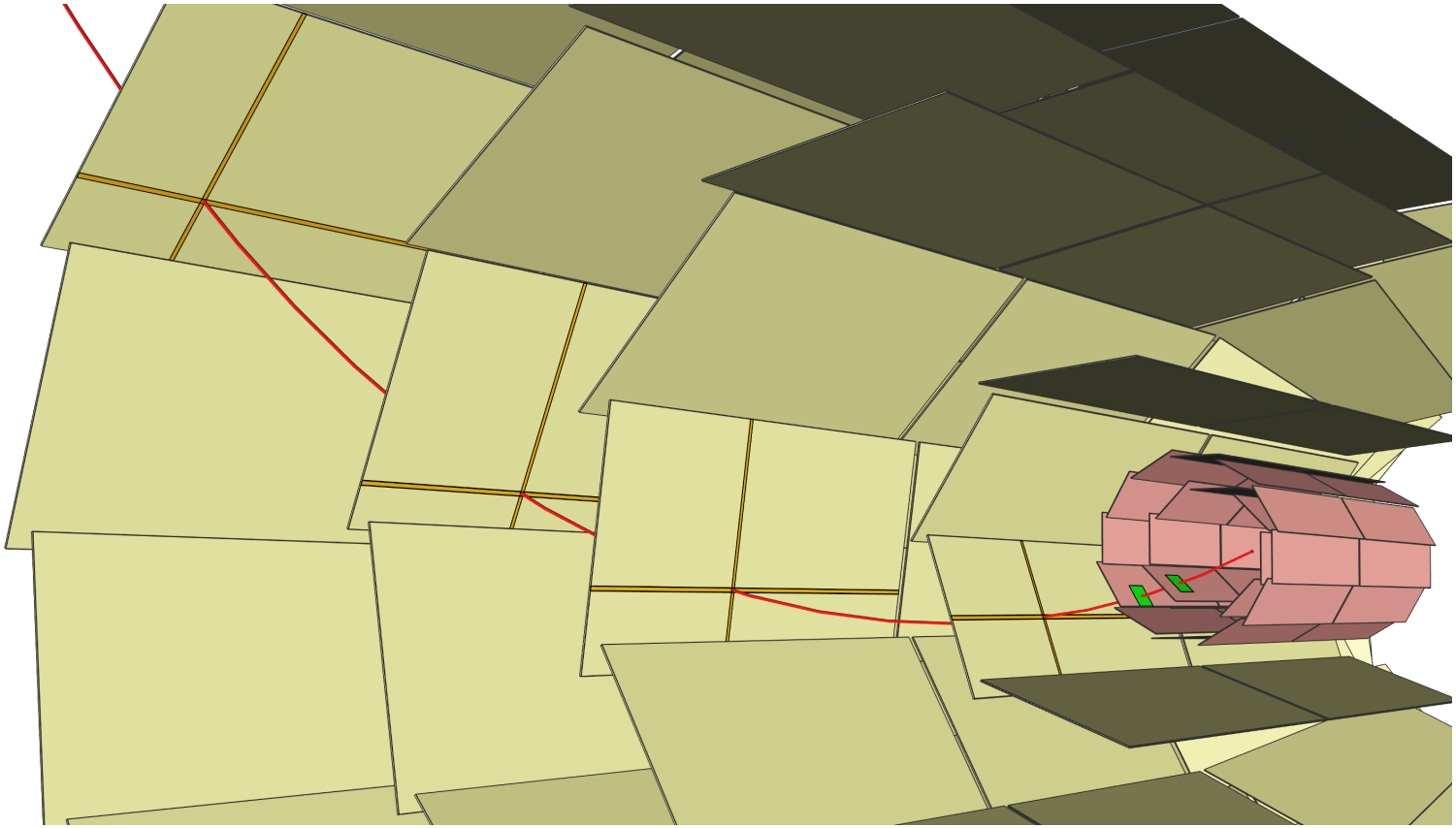
- Developed during M. Wagner's PhD thesis
- Tested during EMC beam-test at MAMI in 2015
- Read out with PTDAQ:
  - 48 crystals of Proto120
  - 16 channels of the photon tagger
- Successful burst-building of 88 million events without errors

Prototype of PCIe-Based Read-out System



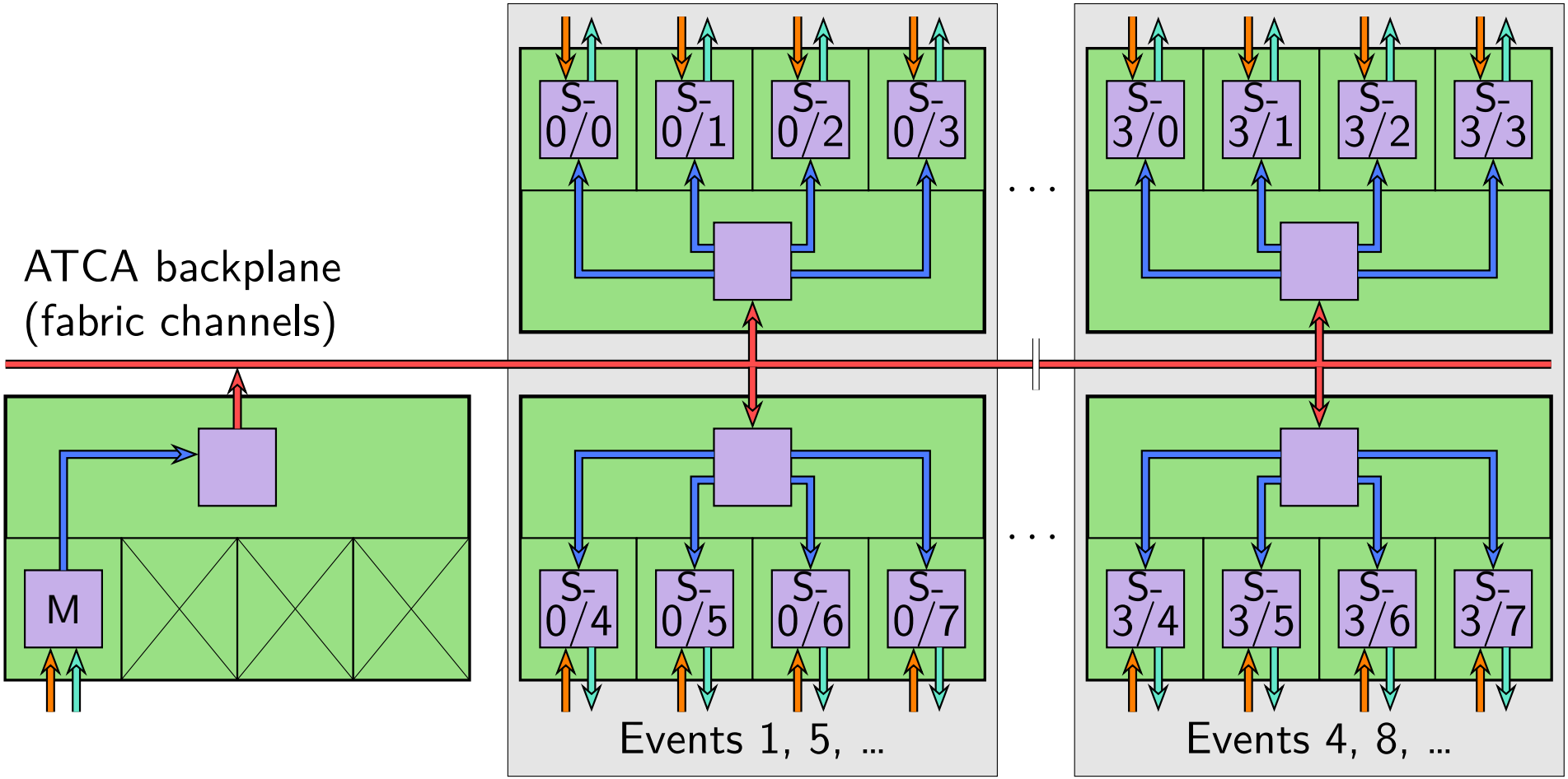
- Developed during S. Reiter's Master's thesis
- Data transferred to a PC with C-RORC PCIe card
  - Developed for ALICE DAQ, H. Engel et. al.
  - Virtex-6 FPGA LX240T
  - Gen2 x8 PCI Express
  - Three QSFP transceivers
- Data sent by 3 xFP cards, 12 $\times$ 1 Gbps total
- Tested up to 92.5 MB/s per link
- Stored via DMA, limited to 450 MB/s by SSD

Belle II: PXD Data Reduction with Regions of Interest



- Compute Nodes store pixel-detector data (20 GB/s) in RAM
- Regions of interest are received from high-level trigger (PC farm) and applied online
- Remaining pixels are sent to event-building system

Belle II: Compute Node Data Flow



- Pixel data stored in selector (S) AMC cards
- ROIs received by Merger (M) card, distributed over ATCA backplane
- Verified in beam tests with 1 Merger, 1 Selector

Compute Node Upgrade: Carrier Board

- **First stage:** upgrade CNCB (but remain compatible with current xFP)
- **FPGA:** Change to Xilinx UltraScale architecture

	Virtex-4 FX60 (CNCB)	Virtex-5 FX70T (xFP)	Kintex UltraScale 060 (Upgrade)
Registers	50k	44k	663k
LUTs	50k × 4-input	44k × 6-input	332k × 6-input
DSP Slices	128	128	2760
BRAM	4 Mb	5 Mb	38 Mb
MGT	16 × 6.5 Gbps	16 × 6.5 Gbps	32 × 16.3 Gbps
CPU	PPC405	PPC440	-

- No more hard-core CPU → Run slow control over MicroBlaze or a light-weight option like IPbus
  - Belle II experience shows that Linux-based slow control adds a lot of complexity

Compute Node Upgrade: Carrier Board

- **RAM:** 2 GiB DDR2 SODIMM $\rightarrow$ 16 GiB DDR4 (8 chips)
- **Configuration:** Flash/CPLD (slave serial) $\rightarrow$ automatic from NOR Flash (master BPI)
- **GbE switch:** 4 AMCs, 1 switch FPGA, 1 uplink to ATCA Base Interface
- **16.3 Gbps MGTs**
  - 4 links to each AMC card (currently: 4 $\times$ 600 Mbps LVDS)
  - 14 links to ATCA backplane
  - 1 link to RTM (10G Ethernet)
- **Programmable MGT clock**
- **Keep:**
  - JTAG chain/AMC decoupling
  - I2C buses, sensors
  - IPMC connector

Compute Node Upgrade: Rear-Transition Module

- On-board USB-JTAG programmer (Digilent)
- UART-USB interface for 4 AMC cards + switch FPGA
- USB hub
- SFP+ for switch FPGA 10G Ethernet

Outlook

- Upgrade for Compute Node Carrier Board is currently in design phase
- First prototypes planned for 2017
- Also interesting for Belle II upgrade $\rightarrow$ synergy
- Next phase: upgrade of AMC card:
  - Similar upgrade of FPGA and RAM
  - Many more high-speed front I/Os (e.g., Avago MiniPod)
  - In the meantime, current AMC cards can be used in the new carrier board