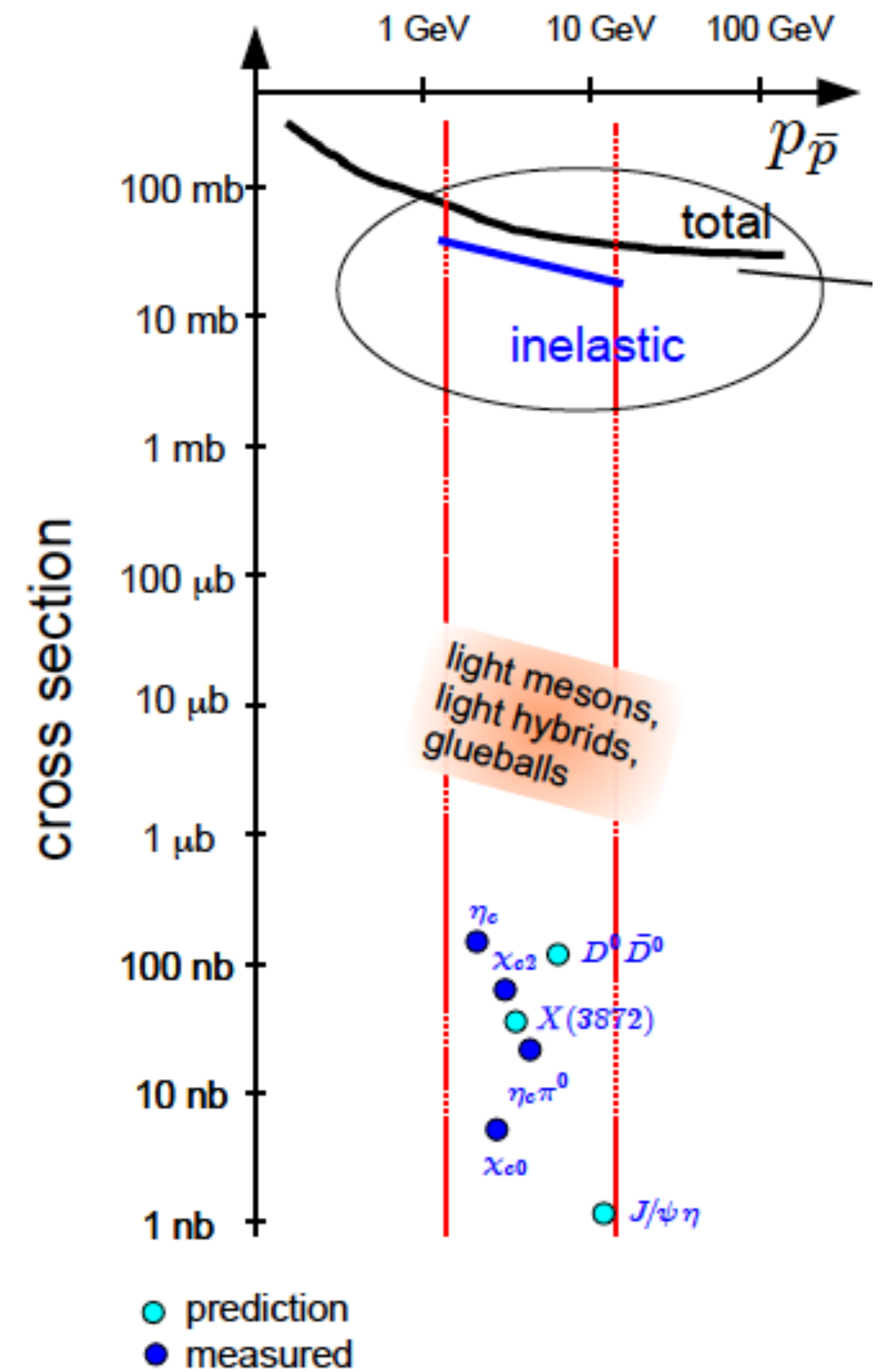
Towards a DAQT TDR

December 2016

Data Acquisition and Event Filtering

- Problem: finding the needle in the haystack
- total inelastic cross section
  - 50 mb
- Interesting physics
  - most channels < 100 nb
- 2x10^6 interactions /s
- Data rate after FEE reduction: 200 GBytes/s
  - 17 PBytes/day
- Goal for online event filtering:
  - reduce "background" by factor of 1000

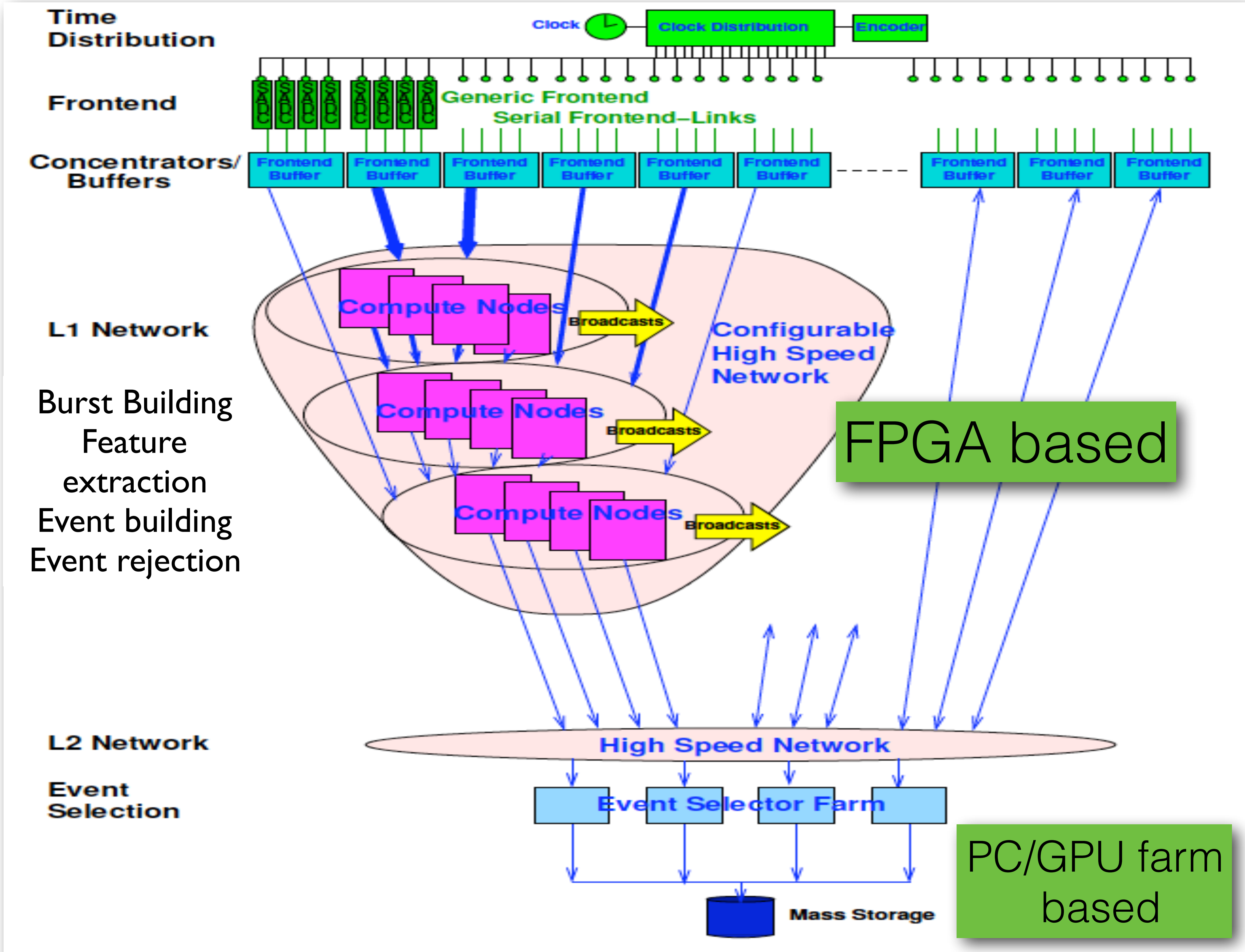


Challenges

- How much can we reduce the primary data rate ?
  - maybe up to factor 1000, some loss of efficiency
- Caveat: event based estimate, but overlapping data @ 20 MHz
  - A priori, there are no "events", there is just a stream of "data" from each sub-system
  - Worst case: if we cannot assemble events online, we have to store everything, because we cannot reject anything !
    - 200 GB/s -> 17 PB/day, compare to 30 PB mass storage/year @ FAIR Tier 0
      - Impossible !
  - **Even running at 200 KHz only would exceed the available yearly storage capacity**
- The PANDA physics program is not feasible without effective filtering, reducing the event rate by more than 2 orders of magnitude
- This works only if we are able to reconstruct most of the raw data in realtime. Massive challenge !
  - We need full time-based simulation and reconstruction software to judge feasibility and determine required resources (**not available now and for the foreseeable future, due to lack of manpower**)

Proposed workaround (Groningen DAQT workshop, April 2016)

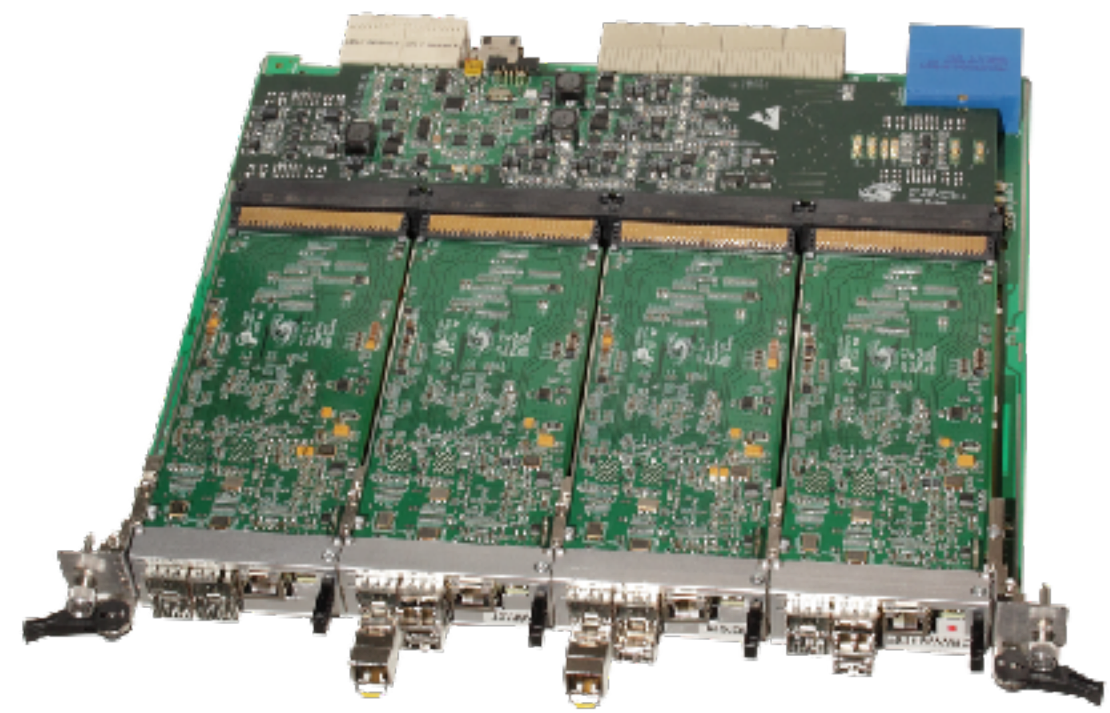
- **Staging**
  - **Phase 1**: DAQ and event filter for “save” event rates requiring no real-time treatment of overlapping events
    - Burst building -> event building
    - Event filtering performance can be evaluated with event-based simulations
  - **Phase 2:** Upgrade to 20 MHz



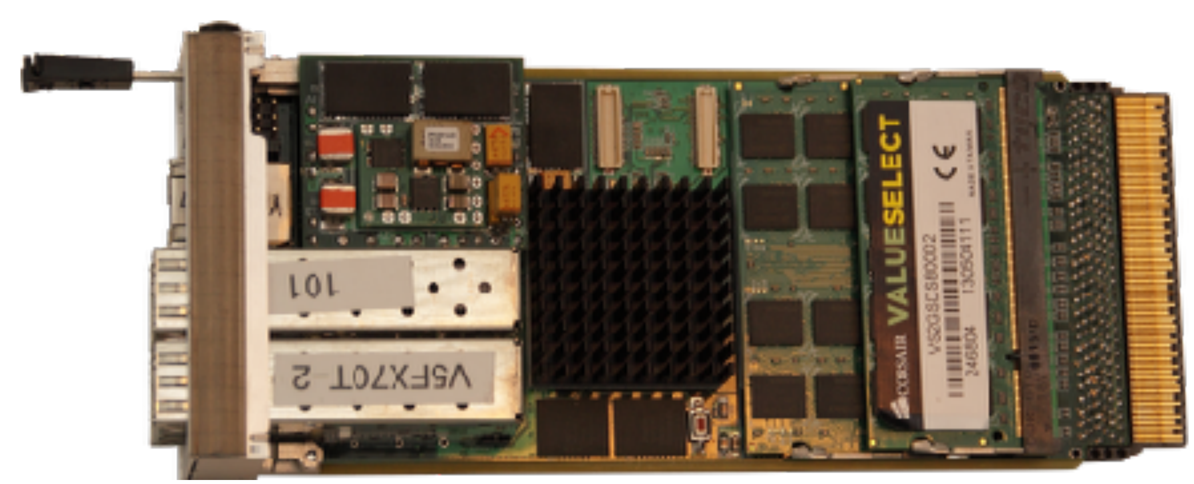
PANDA DAQ / Event Filter

Building Blocks (L1 network)

- FPGA based Compute Nodes (CN)
- ATCA standard, full mesh backplane
- 4 + 1 FPGA Virtex5 70FXT
- 16 optical links, GbE
- 18 GBytes DDR2 RAM



- Upgrade to Kintex Ultrascale architecture (see talk by Thomas Geßler)
- Factor 10 better performance
- Factor 5 better performance/price ratio



Contents of TDR

- **Introduction** : physics objectives, detector configuration
  - Cross sections, luminosities, detector performance (tracking, EMC, PID …)
- **Requirements** (event rates, event size, pile-up situation, storage capacity, event filtering capabilities, partitioning of DAQ, running modes…)
- **System architecture**
  - Building blocks (time synchronisation (SODAnet), data concentrators, data transport, FPGA based Compute Nodes, CPU/GPU farm, …)
  - Data format, interfaces and data flow
  - Event filter: partitioning and performance of algorithms (L1, L2), …
  - Run control system, error detection and recovery, Data Quality Monitoring (DQM)
- **Performance** simulations and measurements with prototype systems
- **Manpower, schedule and cost**

Pre-Requisits

urgently needed

Definition of requirements

- Physics programme of Phase I needs to be defined
  - Cross sections, background situation, detector configuration
  - Event rate, event size and required rejection factors, acceptable efficiency loss
    - Need simulation of gas detector performance to explore/define "safe" rate before pile-up destroys rejection capability for event-based approach

Partitioning and Performance of Event Filtering

- We need realistic event-based simulations for phase 1 physics channels with the staged detector setup (not : fast simulations, simulations with ideal tracking or ideal PID)
  - Unfortunately this still requires a significant development effort - limited by lack of manpower !
- We need to reconstruct the events both with the full off-line algorithms and with fast algorithms based on FPGA hardware
  - Example: STT tracking in FPGA takes 7 us / event vs. much longer but with better resolution with offline algorithm
  - This information is needed to define the partitioning of the event filter

Next DAQT Workshop

- April 10/11 near Giessen