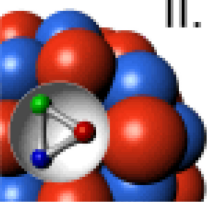


PASTA tests update

Alberto Riccardi

II. Physikalisches
Institut



PANDA LIX. Collaboration Meeting



Contents



1. PASTA overview
2. Board design
3. Setup used
4. Preliminary results
5. Conclusions

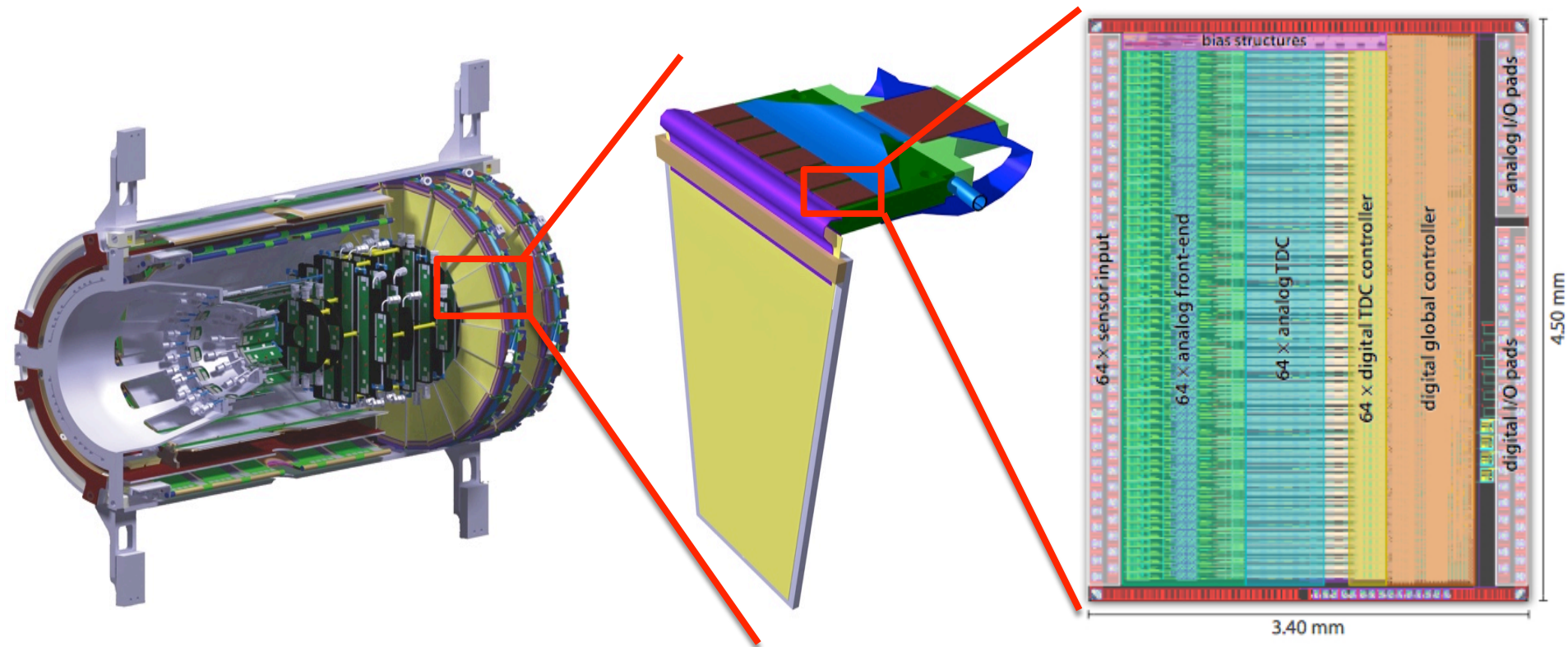
PAnda STRip ASIC (PASTA)

3

Micro Vertex Detector

Sensor Module

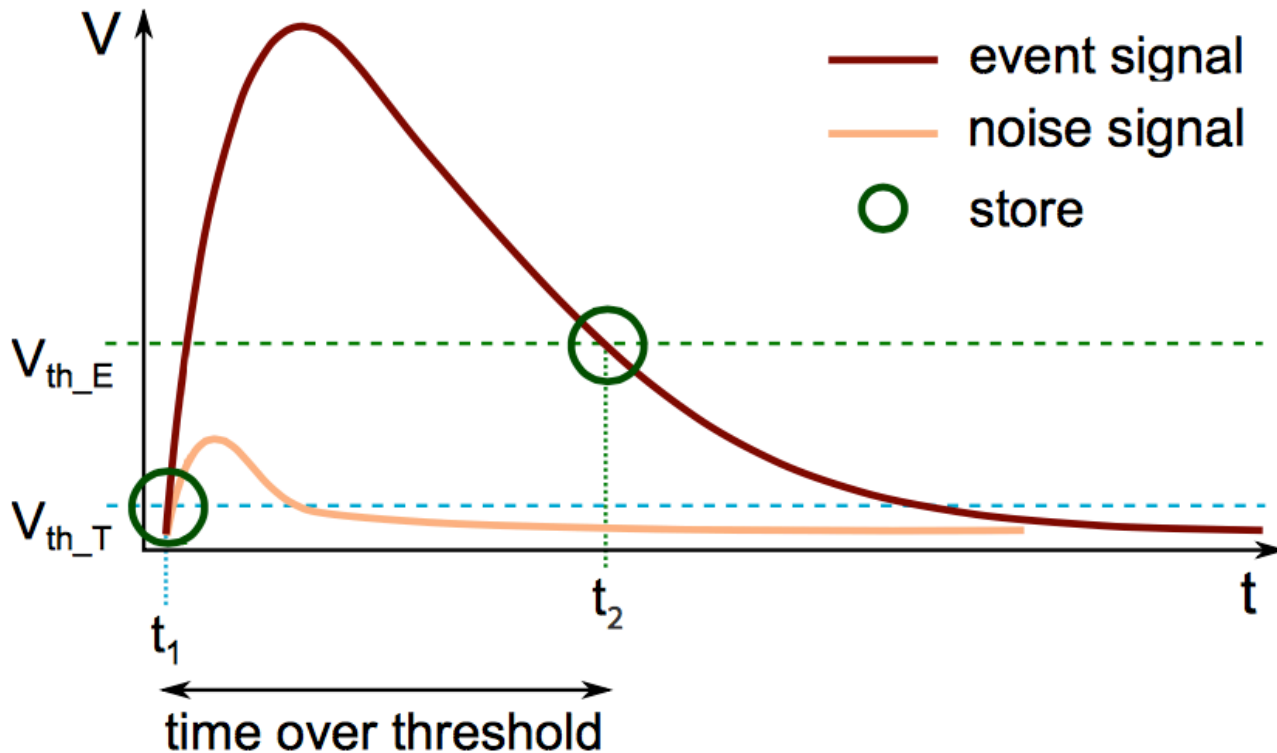
Readout ASIC



Measurement Concept

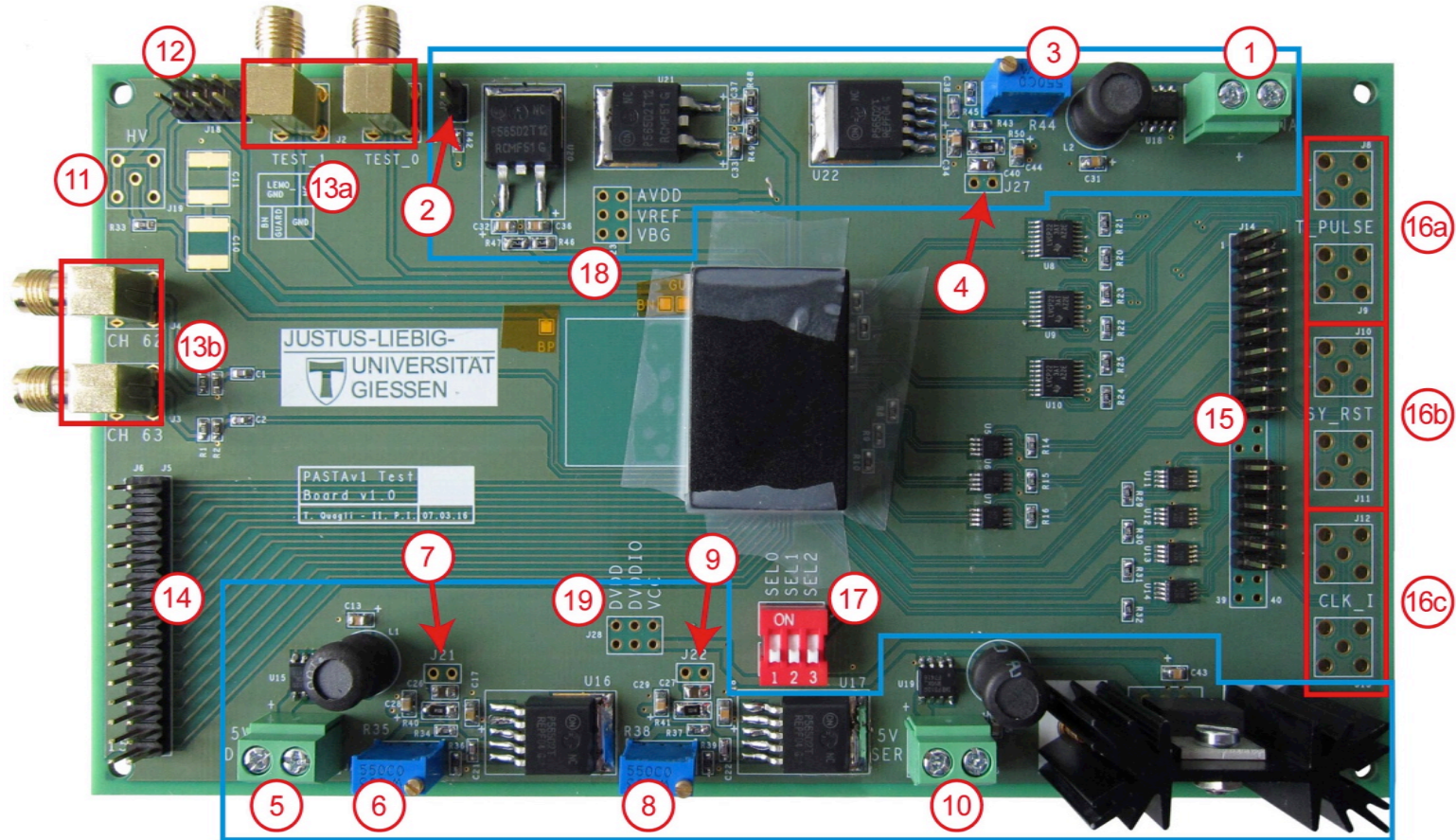
4

- Low threshold: better time stamp resolution
- High threshold: better jitter performance



DISH assembled

6



- 3 Boards equipped with PASTA
- 2 Boards with PASTA and a strip sensor

Readout softwares

7

JDRS - Julich

LabView - Turin

The screenshot shows the PASTA Software configuration window. It is divided into several sections:

- UDP connection:** Includes buttons for 'Send Global', 'Read Global', 'Send Channel(s)', and 'Read Channel(s)'. There are also checkboxes for 'All channels' and 'Only 0-1'.
- Configuration:** Includes 'Config TP Digital' and 'Config TP Analog' buttons.
- Global Digital Configuration:**
 - General configuration:** Includes 'Channel select (CS) as veto' (checkbox), 'Activate TAC refresh' (checked), 'TAC refresh period' (set to 2^14 clk), and 'Ch. counter interval' (set to 2^10 clk).
 - Clock settings:** Includes 'Input clock divider' (set to original), 'Clock output' (checked), 'Clock gating for TDC read logic' (checked), and 'Clock gating for TDC write logic' (checkbox).
 - Data output:** Includes 'Dummy data output' (checkbox), 'Double data rate' (checkbox), 'Transmission mode' (set to TX0), 'Data format' (set to Compact), and 'Fine time offset' (set to 0 clk).
 - Enable counting of ...:** Includes 'global SEUs' (checkbox), 'truncated events (full frame buffer)' (checkbox), and 'missed events (full event buffer)' (checkbox).
- Global Analog Configuration:**
 - Front-end configuration:** Includes 'Strip configuration' (n-side), 'Baseline voltage' (31), 'TOT amplifier bias current' (15), 'Preamplifier output voltage shift' (17), and 'Preamplifier feedback current' (14).
 - Peaking time adjuster current:** Includes 'p-strip' (14) and 'n-strip' (14) settings, with a 'buffer' (21) and 'reference' (LSB) option.
 - Local feedback current DAC:** Includes 'reference' (21) and 'LSB' (13) settings.
 - Hysteresis comparator bias current:** Includes 'stage 1' (8), 'stage 2' (14), and 'stage 3' (19) settings.
 - Ref. voltage for hysteresis comp.:** Includes 'p-strip' (15) and 'n-strip' (15) settings.
 - Charge sensitive amp. bias current:** Includes 'input' (13) and 'source follower' (23) settings.
 - Current buffer bias:** Includes 'output (I)' (21), 'input (I)' (14), and 'input (V)' (10) settings.
 - Baseline restorer:** Includes 'bias (I)' (30) and 'cascade (V)' (22) settings.
 - TDC configuration:** Includes 'Latched comparator voltage' (31), 'Transistor cascade voltage' (3), and 'Current generator' (2).

The screenshot shows the LabView software interface for data measurement. It features a grid of plots and control panels:

- Measurement Settings:** Includes 'timeout (ms)' (1000), 'Max retries' (0), 'CRC errors' (7), and 'CRC failed' (1).
- Plots:** A grid of plots showing 'Total events', 'Events selected', 'T coarse', 'E coarse', 'T SoC', 'E SoC', 'T EoC', 'T fine', 'T time', 'E fine', 'TOT', 'T coarse histo', 'E coarse histo', 'T SoC histo', 'E SoC histo', 'T EoC histo', and 'TOT histo'. Each plot shows data points over time (0 to 7200).
- Control Panels:** Includes 'Firmware' (A403), 'Clock frequency' (100 MHz), 'Channel' (A 900, B 0), 'fifo' (1800), 'First channel', 'TP mode', 'Frame sync', 'Last channel', 'TP phase', 'TP frame delay', 'Tac number', 'TP frame interval', 'First event index', 'TP num pulses', 'Tcoarse min', 'TP frame interval', 'Tcoarse max', 'Serial test pulses', 'Eliminate TdE=0', 'Ignore CRC errors', 'Parameter A', 'A coercion', 'Parameter B', 'B coercion', 'None', 'start', 'stop', 'steps', 'Plot colours', 'Start scan', 'Stop scan', 'Load data', 'Save data', 'Duration (min)', 'Display plot index', and 'Display B plot index'.

Configuration interface

Measurement Settings Debug Board 0 timeout (ms) 1000 Max retries 0 CRC errors 104 CRC failed 11 End Quit

Global config

TDC Igain 2	CB Ib1 14	IFDAC Igain 13	Signal polarity in-type	TDC read clock gating <input checked="" type="checkbox"/>
TDC Iref 2	CB Ib2 21	IFDAC Imin 21	Clock_out enable <input checked="" type="checkbox"/>	TDC write clock gating <input type="checkbox"/>
TAC Vcas_p 6	CB Vbias 10	PRE Ifn 14	Test pattern mode <input type="checkbox"/>	Clock divider 0
TAC Vcas_n 16	CSA Ib1 13	PRE Ifp 15	External veto enable <input type="checkbox"/>	TAC refresh 0
Comp Vcas 31	CSA Ibsf 23	PRE Ishift 17	Event mode Full	External TP enable <input checked="" type="checkbox"/>
Comp Vb 31	HCG DAC- 0	PTA Ibn 14	Events counter None	Tx DDR enable <input type="checkbox"/>
BLR Ib 30	HCG DAC+ 15	PTA Ibp 14	Counter interval 0	Tx mode Tx0 + Tx1
BLR Vcas 21	HC Ib1 8	PTA Ibuf 21	Fine counter kf 0	
	HC Ib2 14	TOT Ib 15	Fine counter saturate <input type="checkbox"/>	
	HC Ib3 19	Vbaseline 63		

Global test config

Cal enable Cal level 20
Debug enable Debug channel 0

Ext TP out

Ext TP out frame delay 0
Ext TP out pulse width 200
Ext TP out frame interval 20
Ext TP out num pulses 100

Fine time calibration

Kf 0
Clock frequency (MHz) 160
Frame ID bits 0

T TDC 1xTck 0 T TDC 3xTck 0
E TDC 1xTck 0 E TDC 3xTck 0

Default channel config

Channel enable <input checked="" type="checkbox"/>	Trigger mode 0
Test mode <input type="checkbox"/>	Sync chain length 1
Prediction mode <input checked="" type="checkbox"/>	Stop charge delay 0
E-branch validation <input checked="" type="checkbox"/>	TOT Ifb 8
Parallel flip-flop <input checked="" type="checkbox"/>	T threshold 0
T-branch delay enable <input checked="" type="checkbox"/>	E threshold 0
Unused <input type="checkbox"/>	T TDC IB 10
Events counter Valid	E TDC IB 10

Active channel config

Channel enable <input checked="" type="checkbox"/>	Trigger mode 0
Test mode <input type="checkbox"/>	Sync chain length 1
Prediction mode <input checked="" type="checkbox"/>	Stop charge delay 0
E-branch validation <input checked="" type="checkbox"/>	TOT Ifb 8
Parallel flip-flop <input checked="" type="checkbox"/>	T threshold 0
T-branch delay enable <input checked="" type="checkbox"/>	E threshold 0
Unused <input type="checkbox"/>	T TDC IB 10
Events counter Valid	E TDC IB 10

IO delays

Output delay 10
Serial delay 0
Tx0 delay 20
Tx1 delay 20

TP phase correction

0
Serial offset 9

Verify config

Global config errors

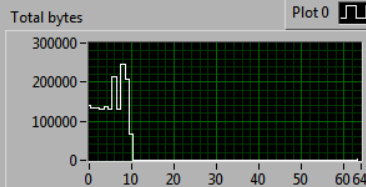
0

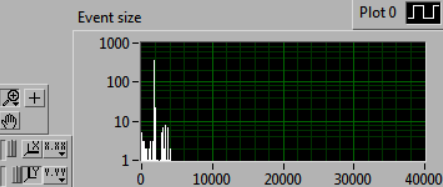
Chan config errors

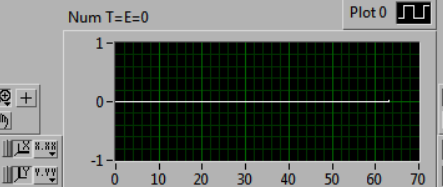
50600

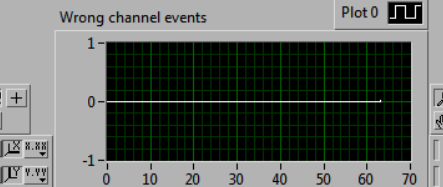
Default channel test config Disabled

Active channel test config Enabled

Total bytes Plot 0 

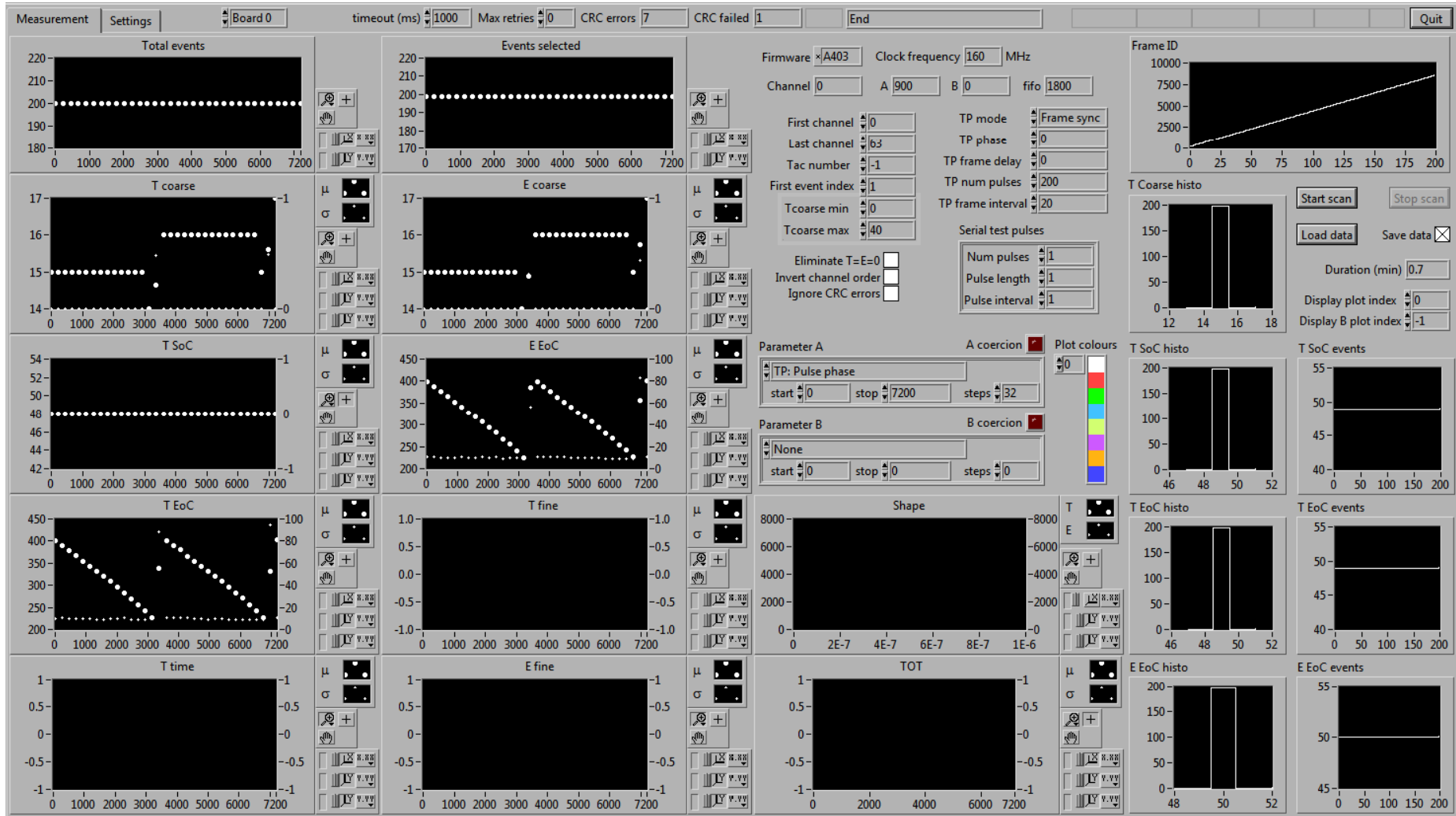
Event size Plot 0 

Num T=E=0 Plot 0 

Wrong channel events Plot 0 

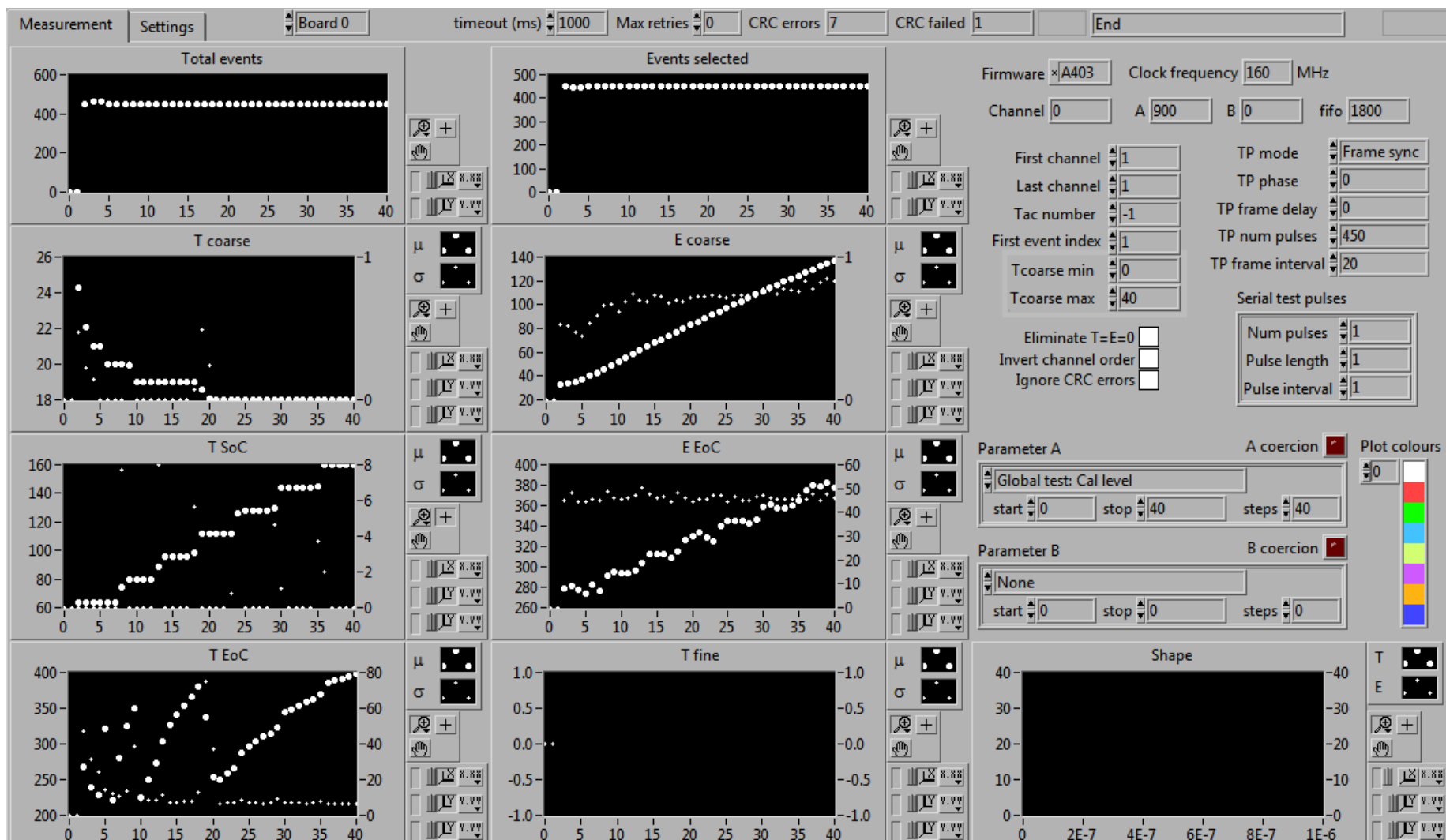
Measurements interface

9



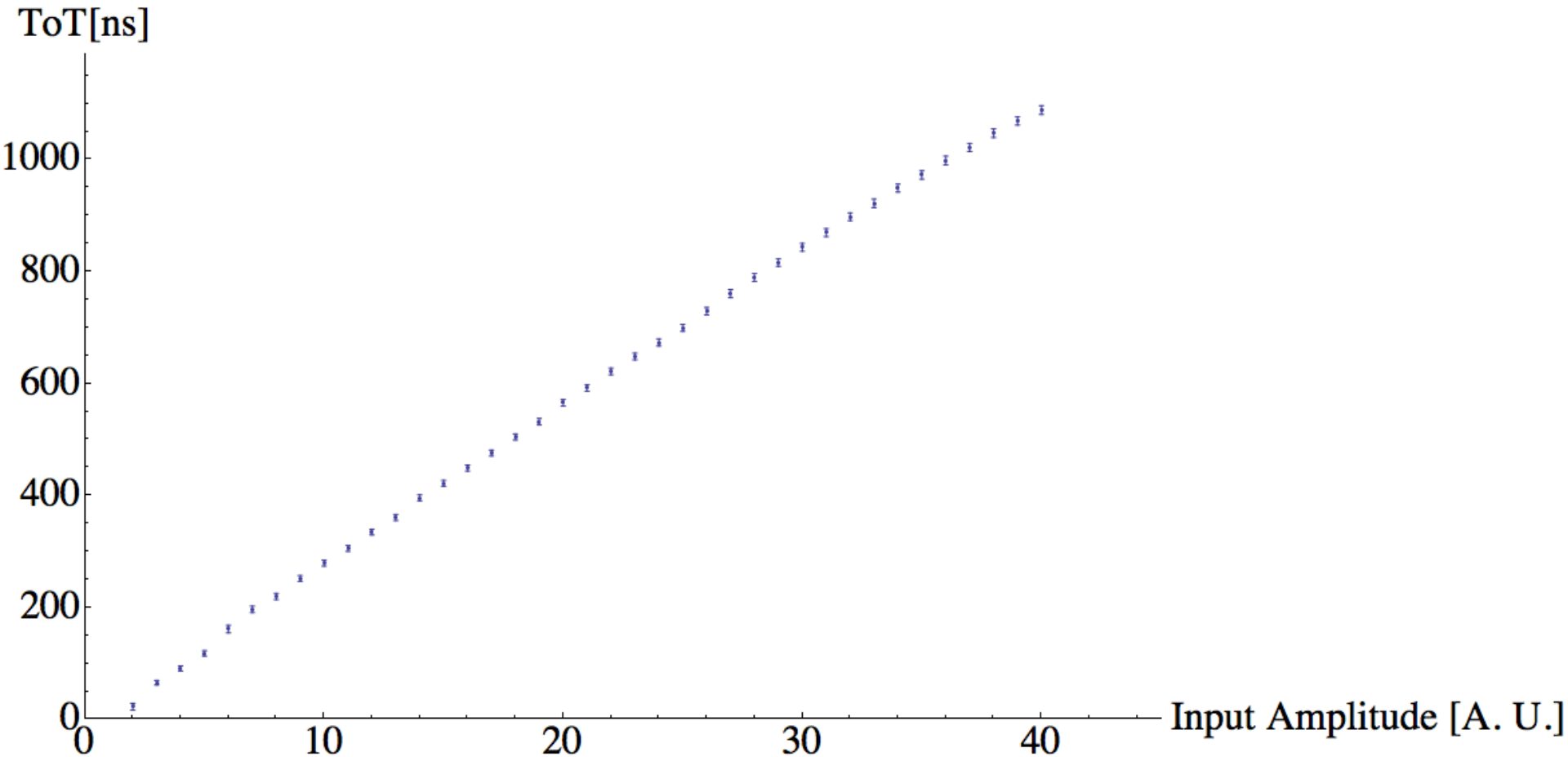
Preliminary FE linearity (1)

10



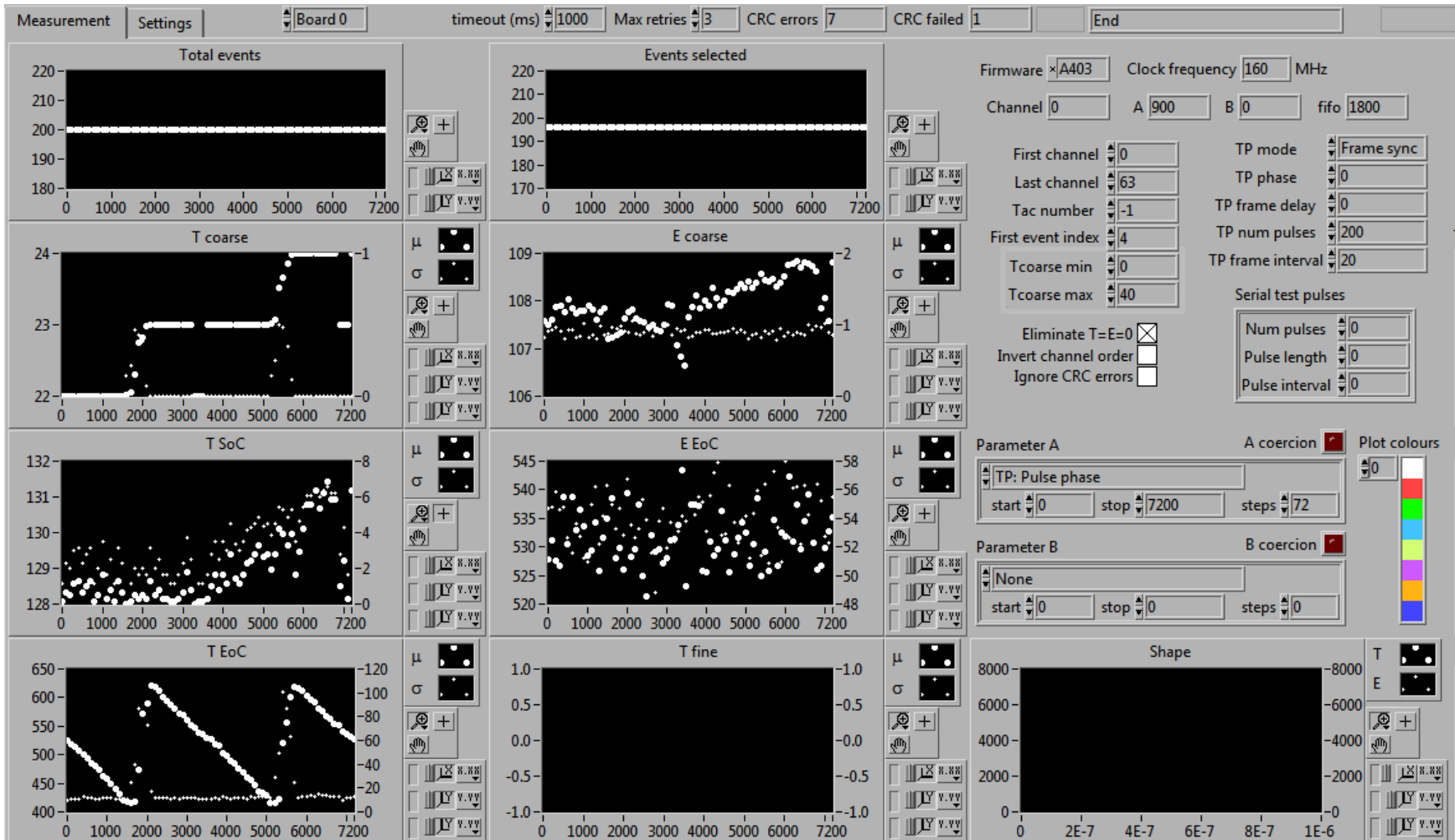
Preliminary FE linearity (2)

11



Preliminary TDC results (1)

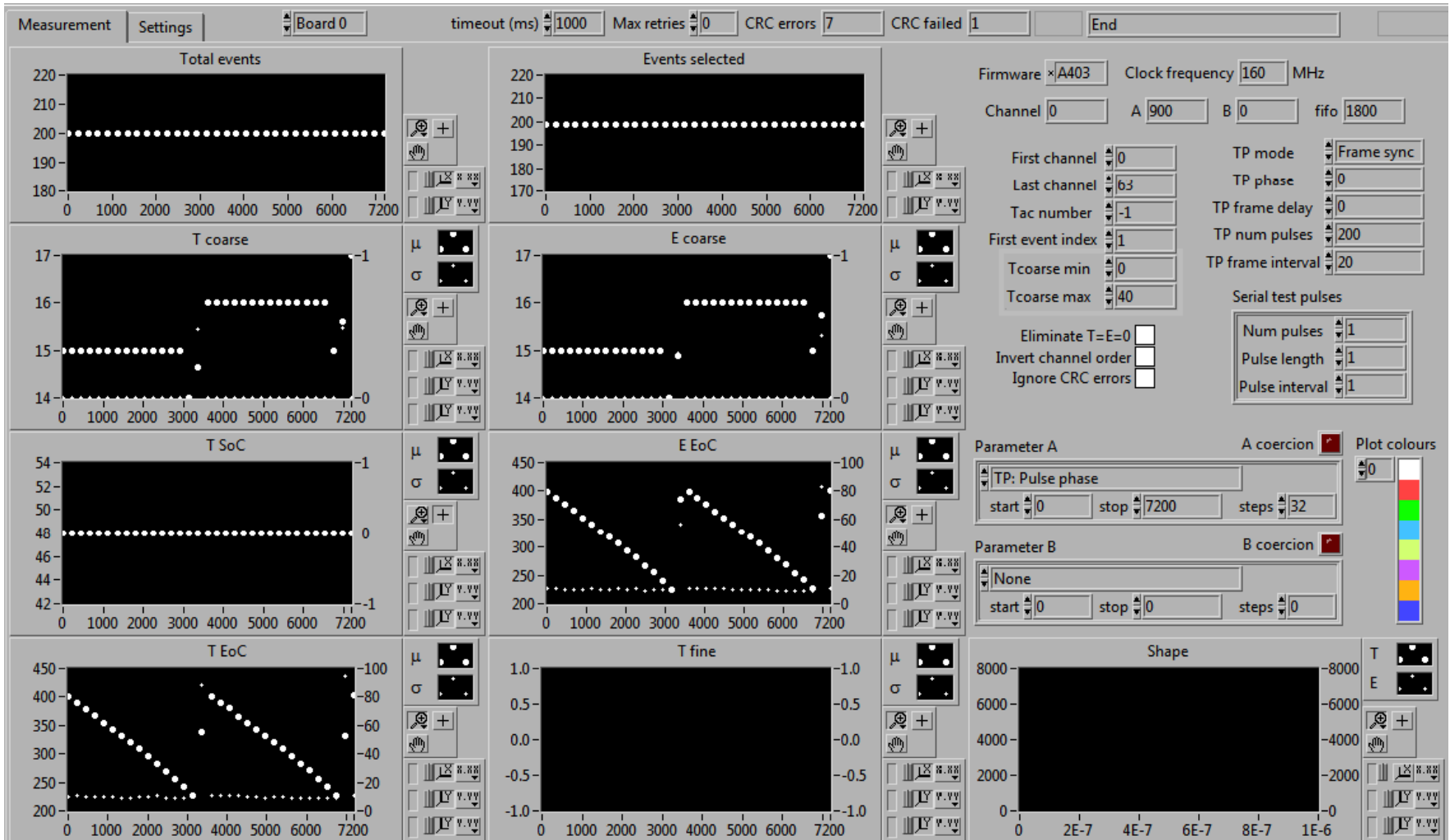
12



Input test pulses injected at the input of the Front End preamplifier

Preliminary TDC results (2)

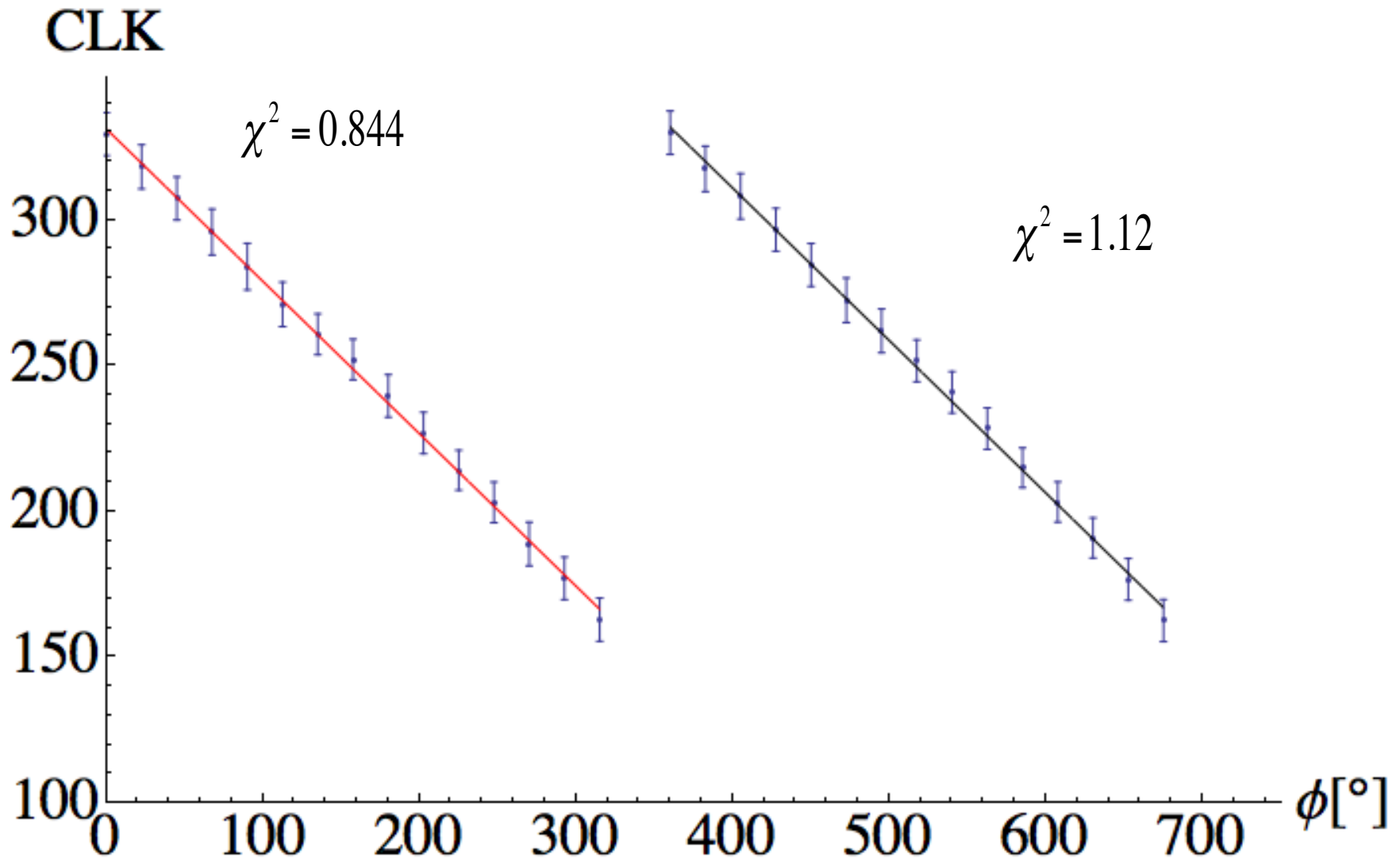
13



Input test pulse injected directly into the TDC

TDC linearity

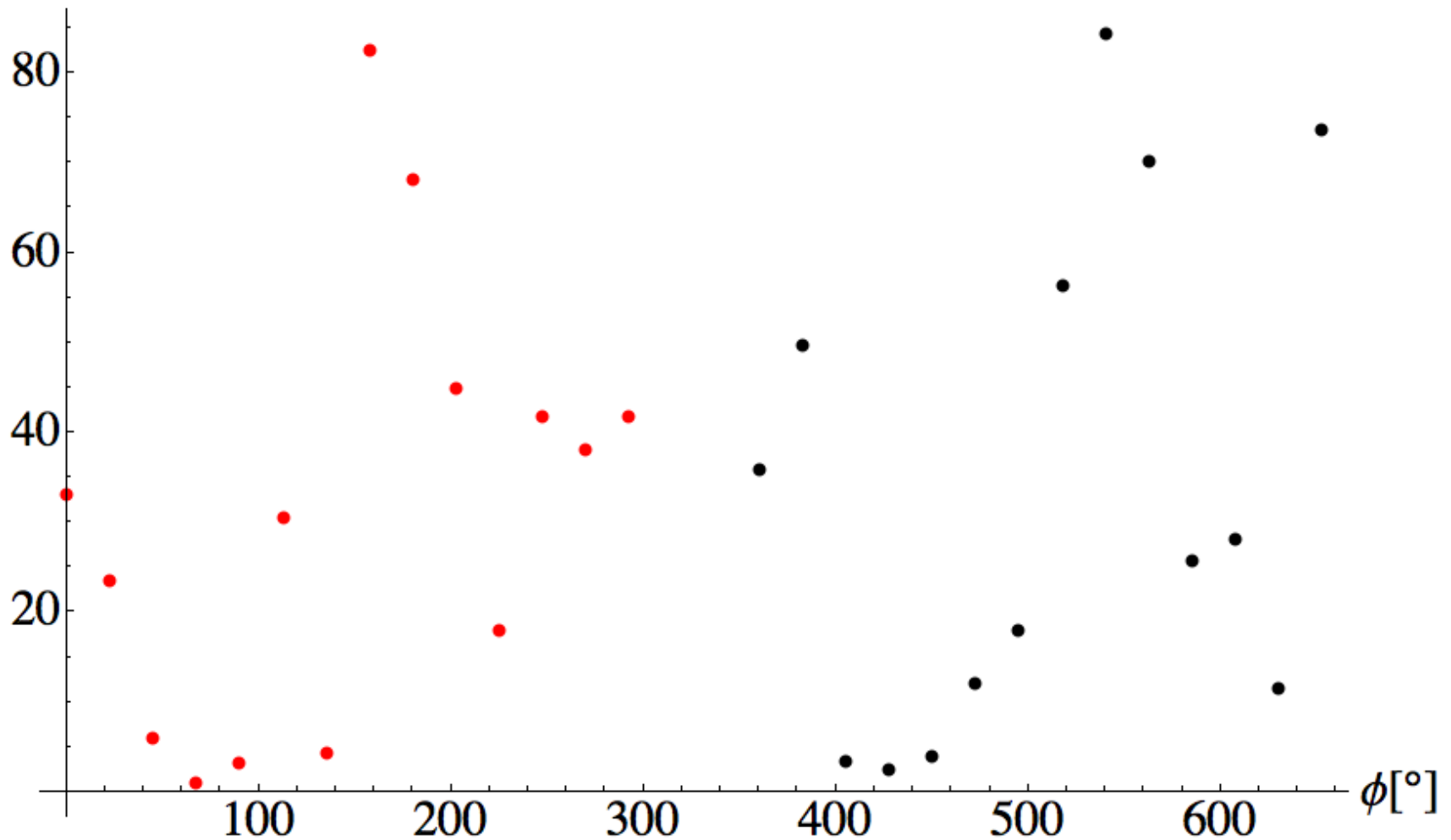
14



TDC errors

15

Error [ps]



Conclusion

16

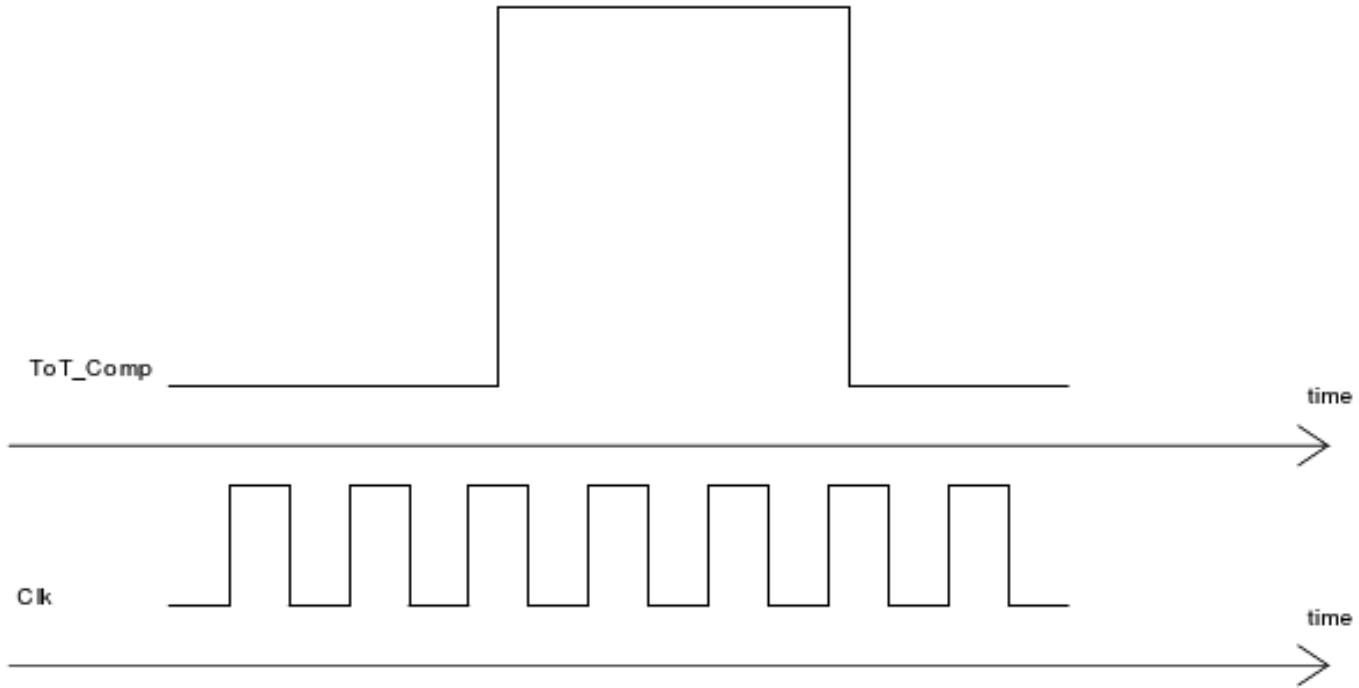
- PASTA is connected to the tests boards
- A complete readout system is under development
- PASTA characterization is started and the preliminary results are encouraging



Thank you for your attention

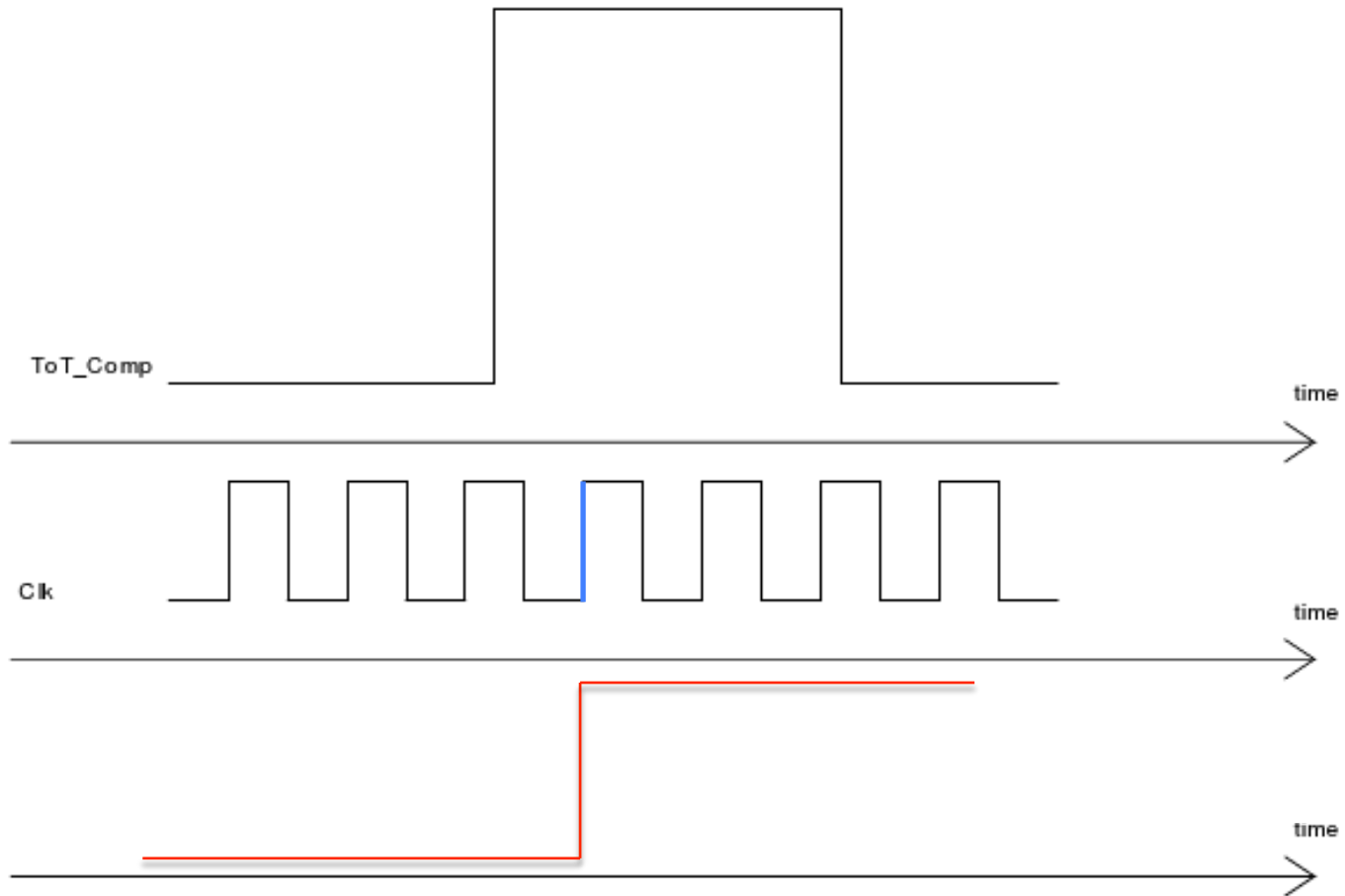
Timing

18



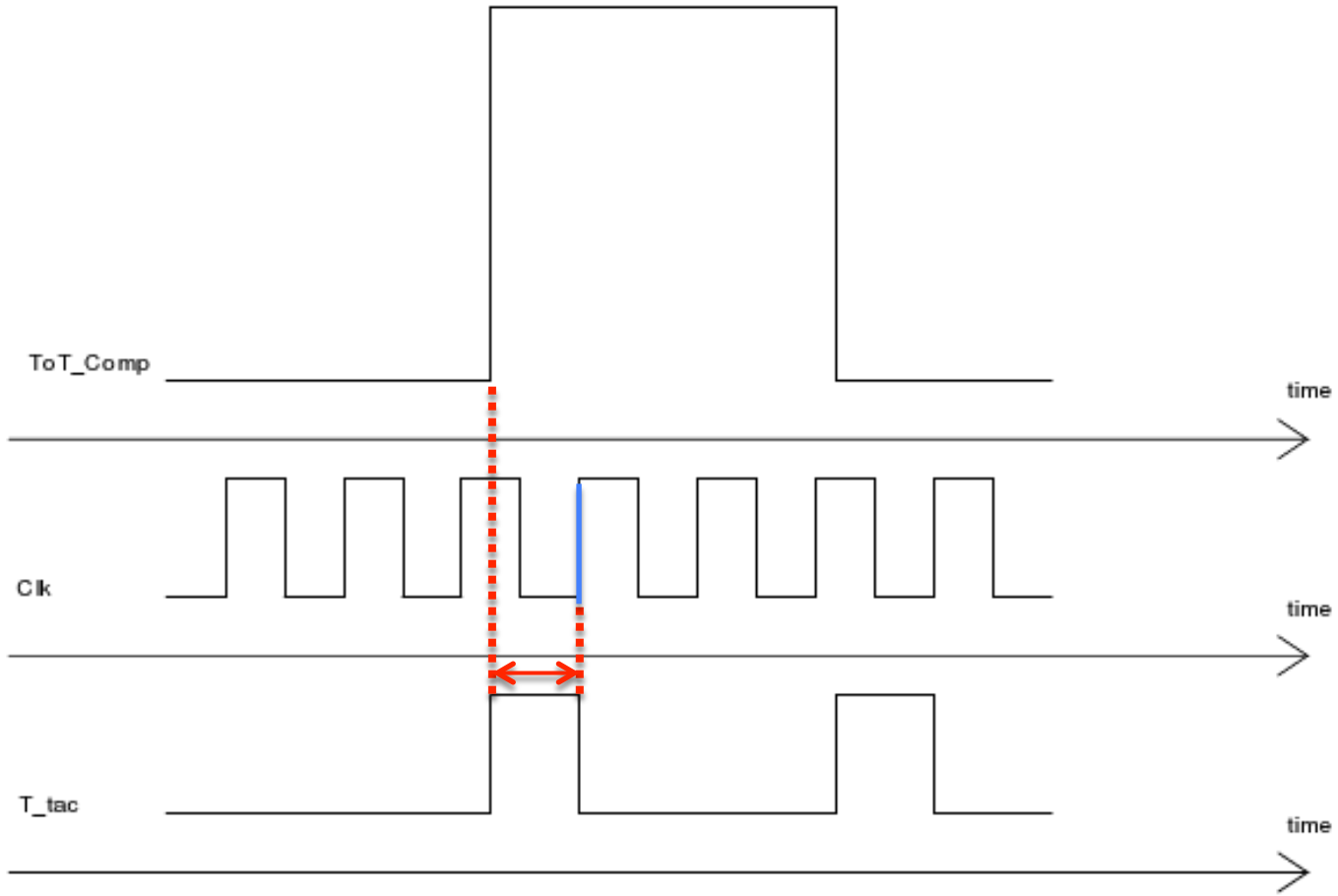
Timing

19



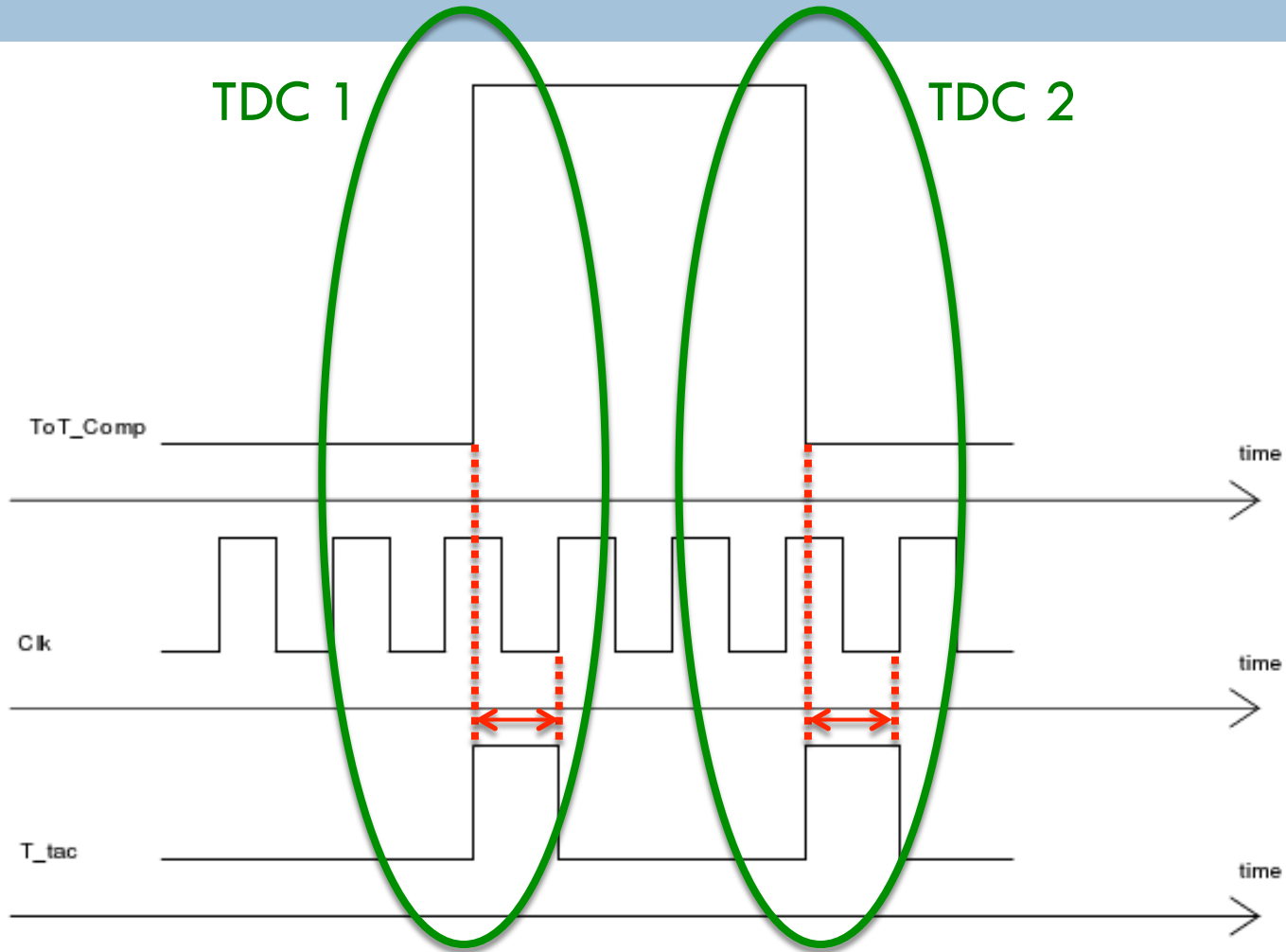
Timing

20



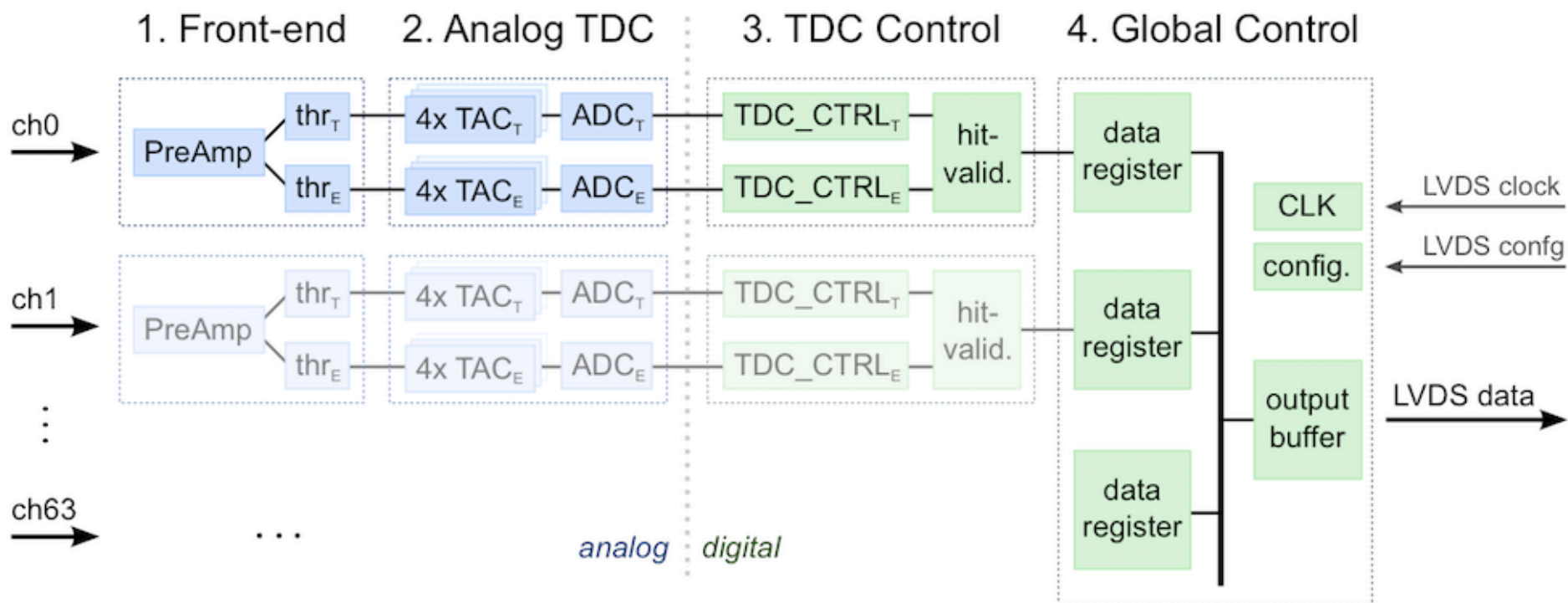
Timing

21



PASTA Architecture

22



Analog TDC Performance

23

