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Status Update on the Activities on PASTA

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Outline

PASTA Readout Chain

Fixes for Known Bugs

New Developments

Data Analysis - Preliminary

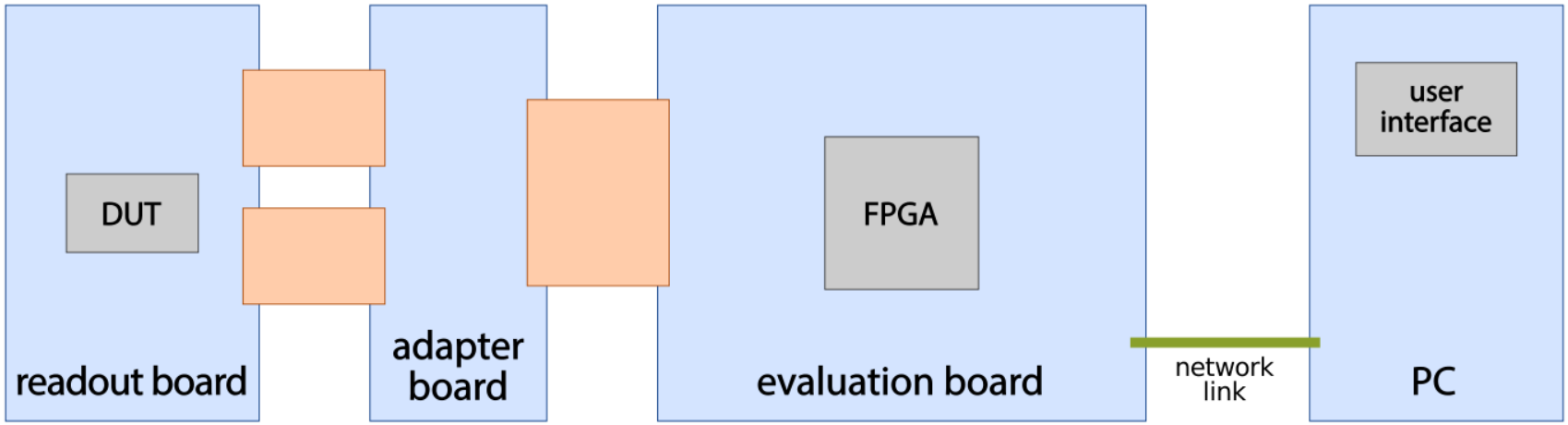
Summary

Outlook

JDRS: Jülich Digital Readout System

The basic components

Jülich Digital Readout System (JDRS).



Data conversion and communication with the PC:

- DUT: ToPix, PASTA
- evaluation board: Xilinx ML605 (Virtex-6 FPGA)
- firmware: VHDL

Configuration and data handling:

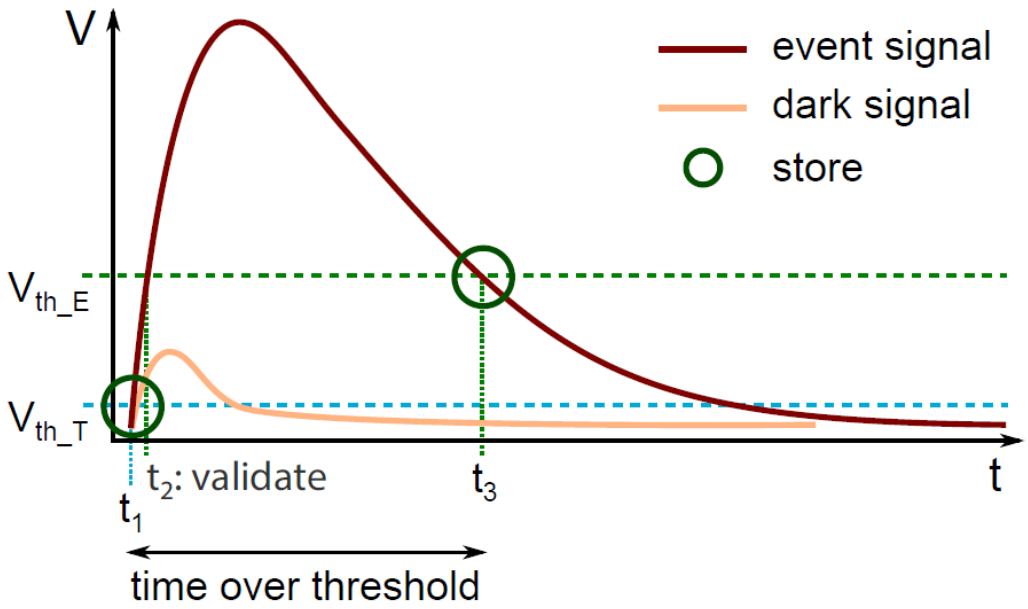
- PC
- software: C++
- **MVD readout framework (MRF)**
- **Qt-based GUI**

PASTA: PANDA Strip Asic

Free running readout chip for the strips

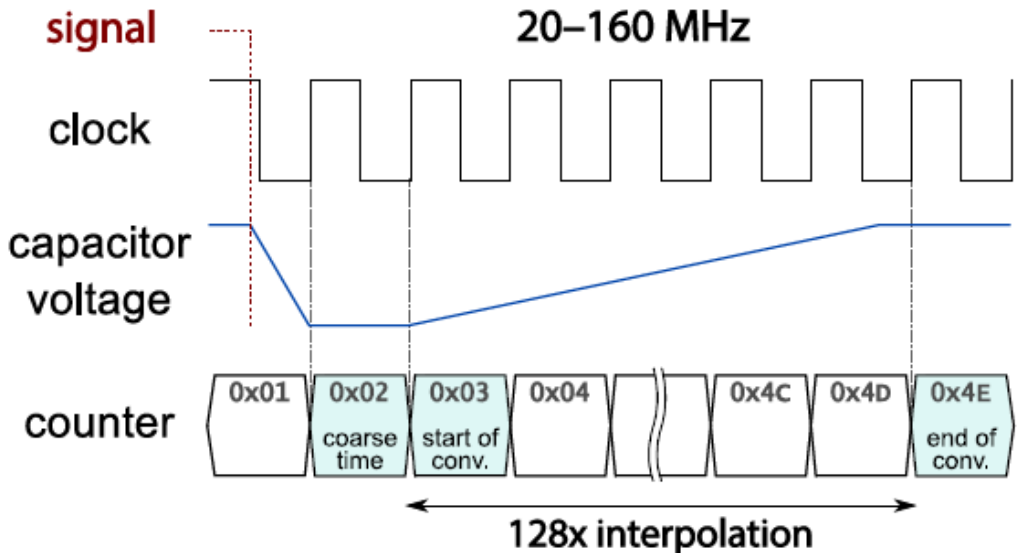
Concept: measurement of points in time based on two leading-edge discriminator outputs.

- Low threshold - time branch: resolve leading edge of pulse.
- High threshold - energy branch: falling edge, pulse length (i.e. deposited charge)



Timestamps

- Clock resolution: 6.25 ns (@160 MHz) - coarse timestamp.
- Enhanced resolution: up to 50 ps - fine timestamp.



- t_coarse $\rightarrow$ leading edge of the clk after threshold crossing.
- t_fine $\simeq$ t_eoc [1] - t_soc [2]

[1] end of conversion
[2] start of conversion

Bug Fixes

Bugs reported @MVD meeting during June CM have been fixed:

- bug in channel configuration (address)
- bug on 10b/8b decoding (synchronization)
- problem on the transmission line (inversion)

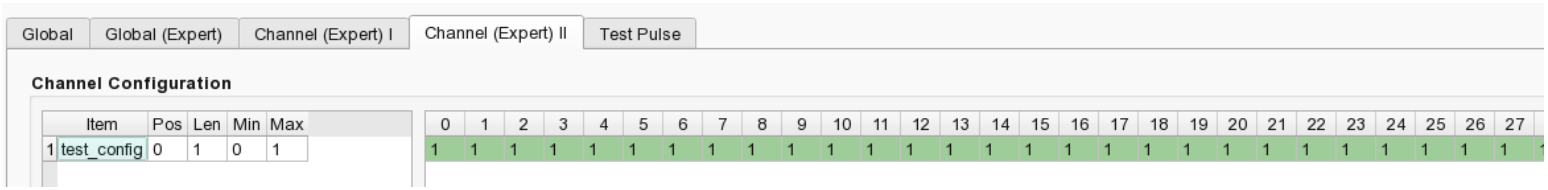
Another bug in the local configuration not visible during configuration, affected the behavior of the chip:

```
constant DEFAULT_CH_CONFIG : std_logic_vector(CH_CONFIG_SIZE-1 downto 0) :=
 '0'        & -- 41     finish config
-- analogue configuration
b"1010"    & -- 40..37 Iref_ratio, energy
b"1010"    & -- 36..33 Iref_ratio, time
b"00000"   & -- 32..28 HCLDAC_e
b"00000"   & -- 27..23 HCLDAC_t
'0'        & -- 22     not used
b"1000"    & -- 21..18 If
...
```

Channel Test Configuration

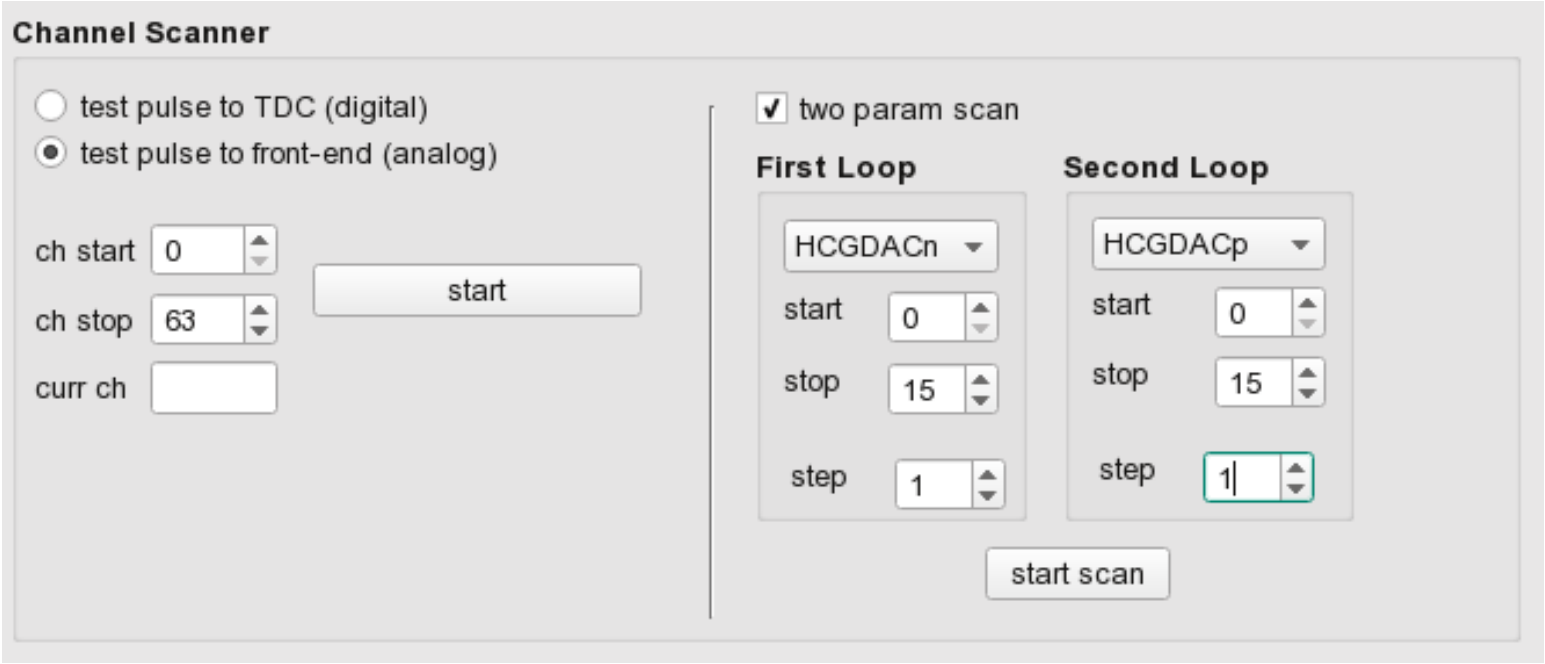
By default all channels are enabled in a test mode.
I.e. they all receive the test pulse.

ch_test_configuration $\rightarrow$ single channels to sensor or calibration circuit



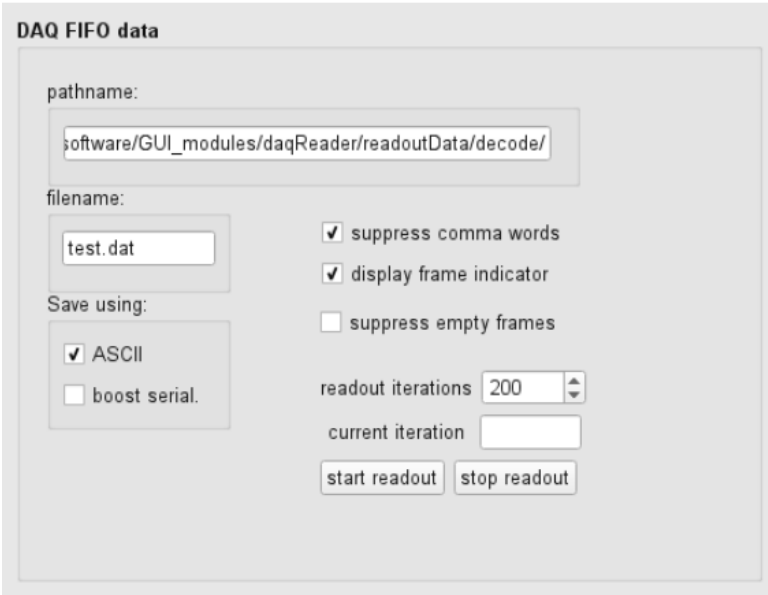
Channel Scan

- Define the type of injection.
- Scan a user define range of channels.
- Choose up to two parameters to sweep
  (at present, global thresholds and pulse amplitude available).



Data Handling

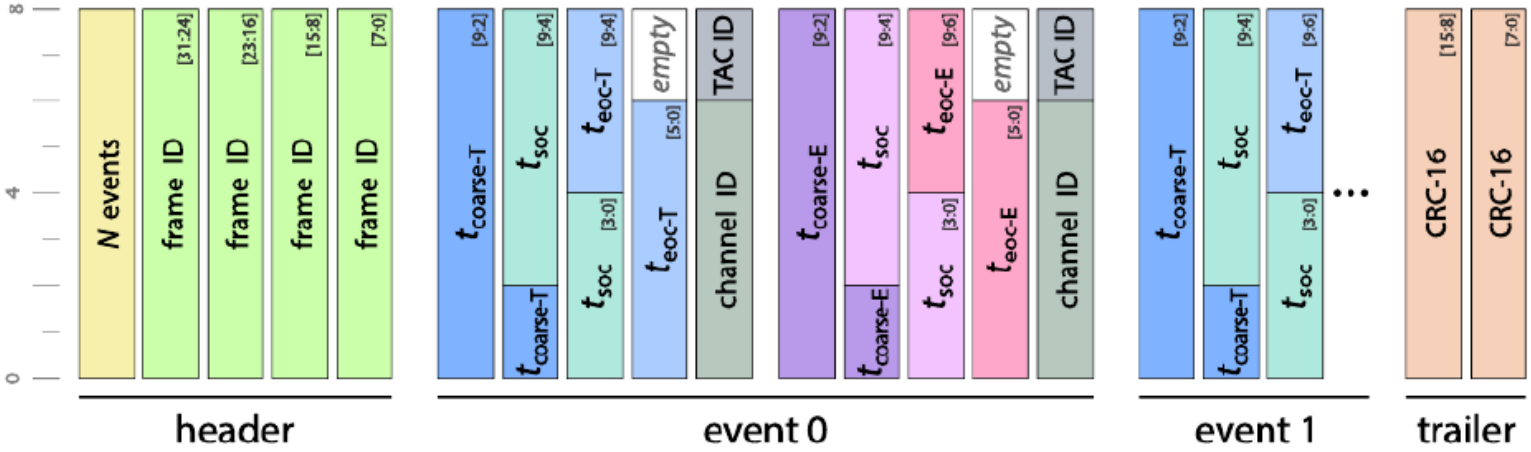
- FPGA data handling:
  - 10b/8b decoded data stored in FIFO.
- Software data handling:
  - request data from fifo.
  - store raw data in ASCII file (hex).
  - convert data word into usable object.



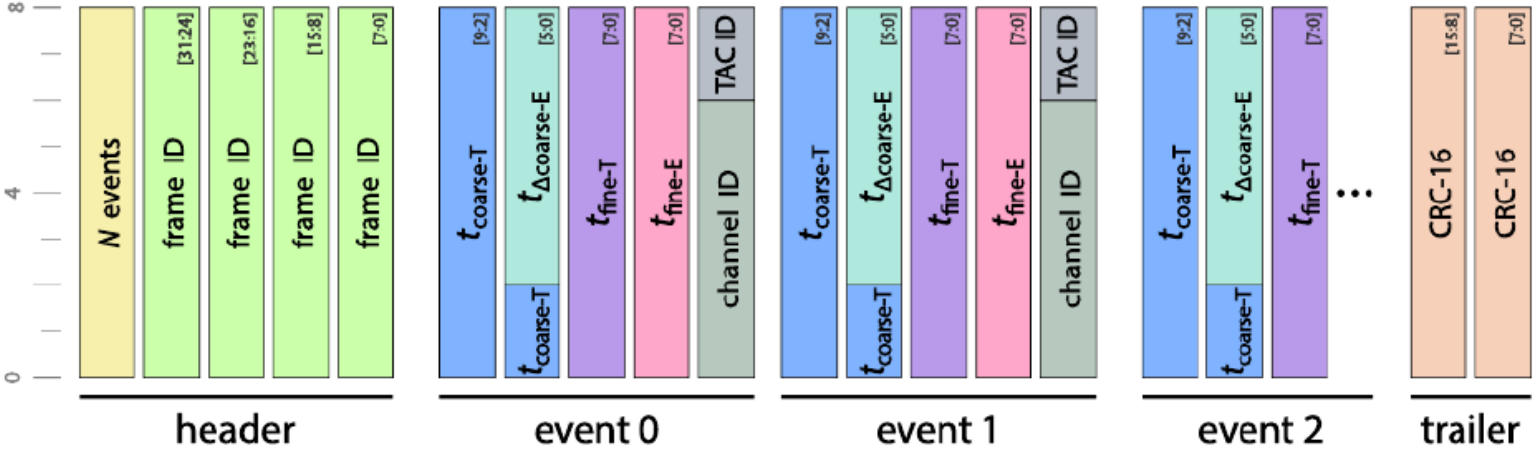
- Suppress comma words
- Display frame indicator
- Suppress empty frames

Data Format

Full mode: two words per event **not decoded in the software** .



Compact mode: one word per event **decoded in the software** .



Empty Frames Suppression

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- Problem:

After the FIFO buffer(s) are completely filled
$\longrightarrow$ data loss inbetween two readout requests.

- Solution:

Different (more or less) complicated options to fix this.
Quick and efficient workaround for testing phase
$\longrightarrow$ suppression of empty frames @FPGA level.
$\Longrightarrow$ Sufficient for high intensity beam?

Data Analysis - Preliminary

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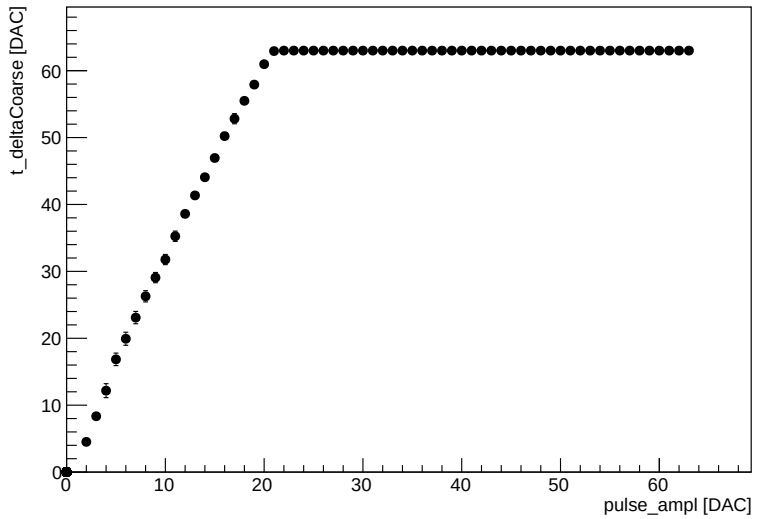
Offline data analysis in ROOT.

- Import decoded data from ASCII file.
- Store it in a TTree.
- Several macros available for different analysis.

TOT Linearity

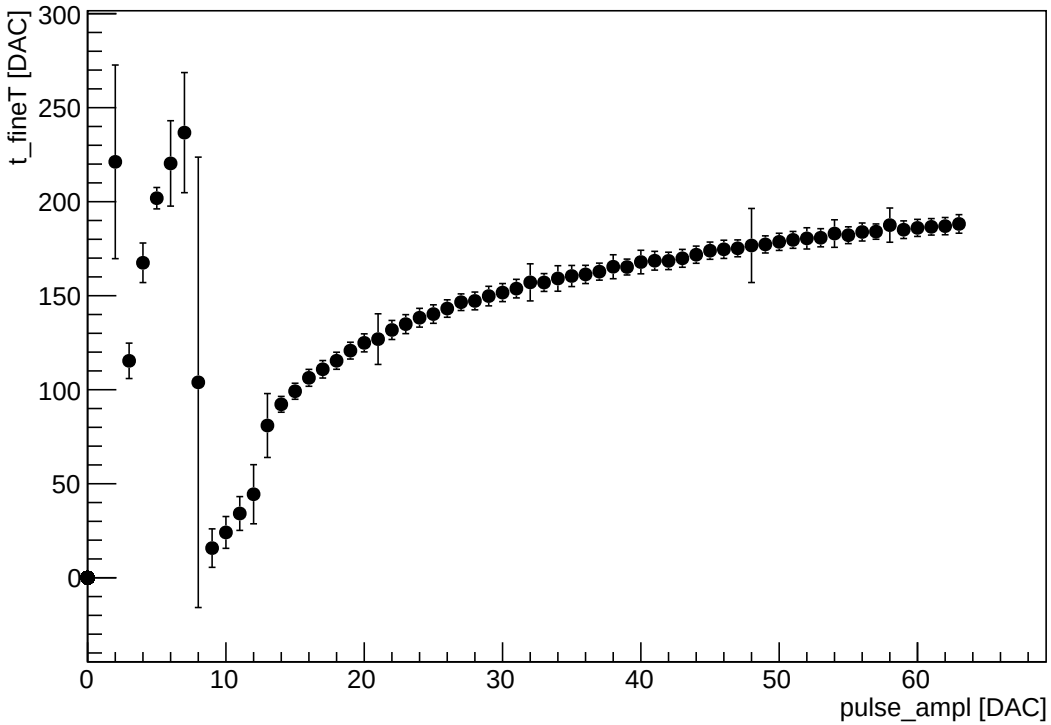
Rough extimation of the time over threshold: $t_{\Delta coarse} = t_{coarseE} - t_{coarseT}$



- Saturation at $t_{\Delta coarse=}$ 63 due to compact mode:
  $\longrightarrow$ value transmitted using only 6 bits.
- Maximum amplitude detectable @50 MHz: 1.3 μs.
- Maximum amplitude detectable @160 MHz: 400 ns.

Fine Time - Time Branch

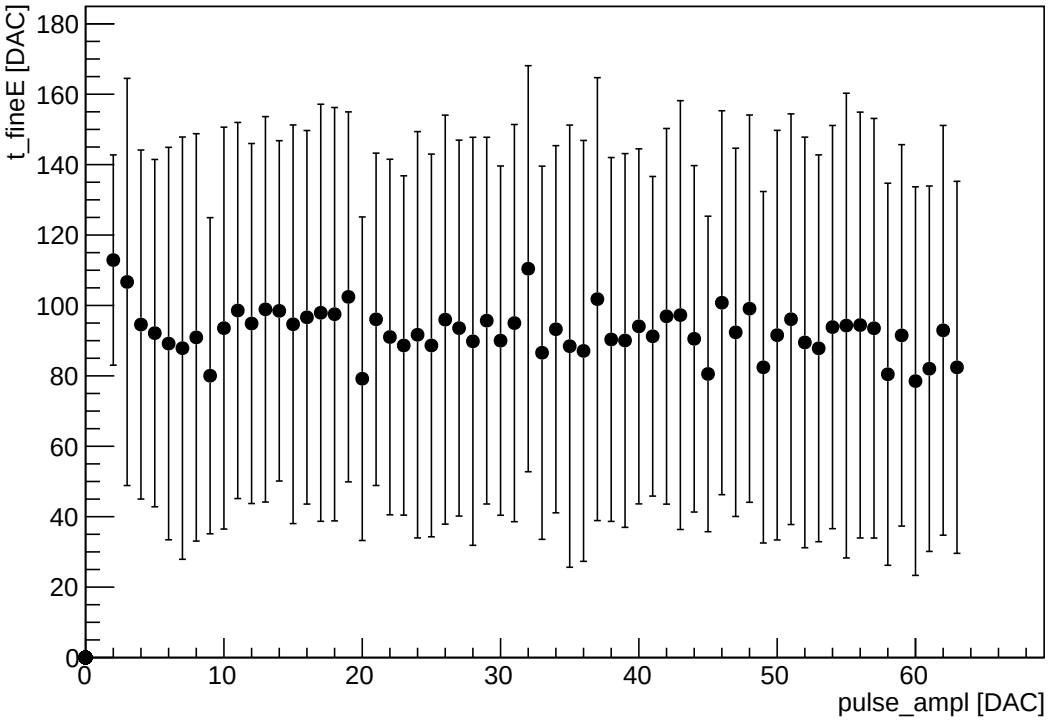
t_fine ≃ t_eoc - t_soc



- Discontinuity (probably) due to which clock edge is used for calculation (i.e. the first one after a falling edge).

Fine Time - Energy Branch

t_fine ≃ t_eoc - t_soc



- Falling edge slower than the rising edge.
- Susceptible to noise.
- Jitter in the timestamp.
- Quite big error bars. (?)

Threshold Scan - qualitative

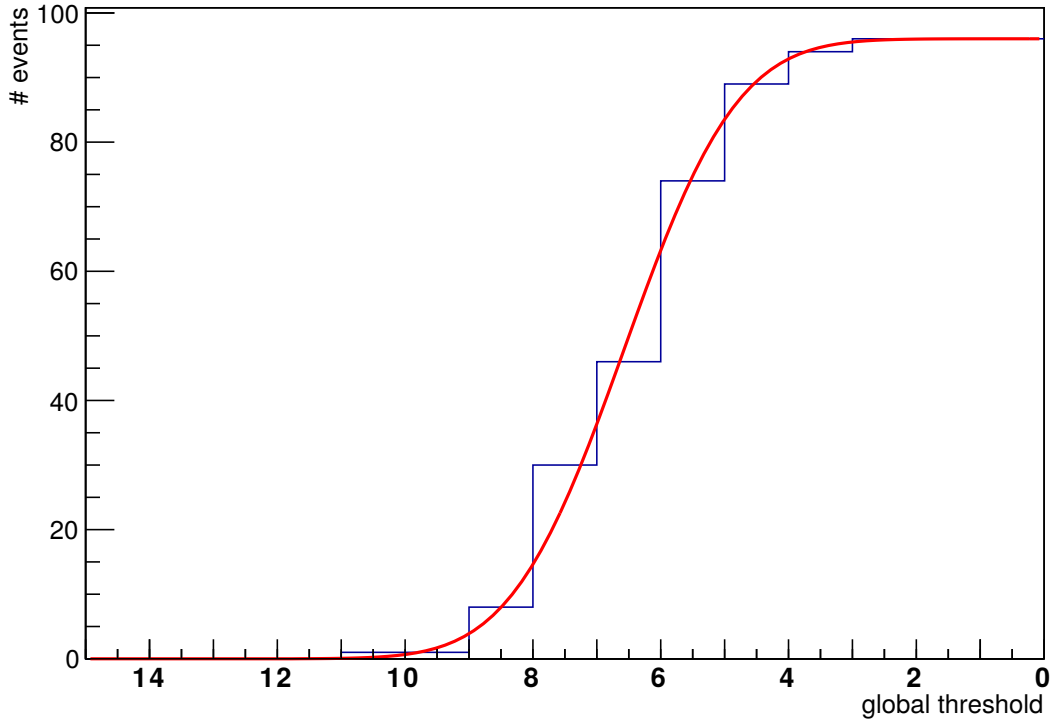
Global thresholds

- $\Delta_{th} = HCGDAC+ - HCGDAC-$
  $\longrightarrow$ midvalue of an interval with predefined amplitude.
- Sweep over Δ_{th} at fixed pulse amplitude.
- Expected: S-curve shape.
- Observed: box-like shape
  $\longrightarrow$ for pulse amplitude $>$ 2 the signal is already above threshold.

Threshold Scan - qualitative

Global thresholds

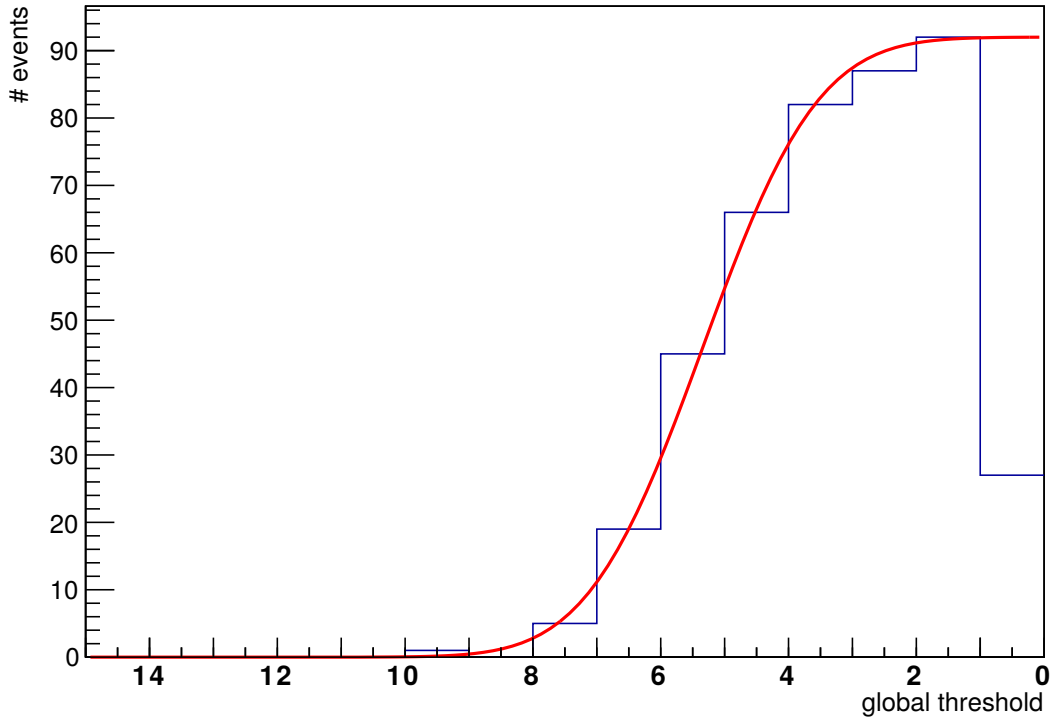
Pulse amplitude $= 1$



$$F(x) = \frac{n}{2}(1 + erf\frac{(x-\mu)}{\sqrt{2}\cdot\sigma}) \quad \text{where} \quad erf\frac{(x-\mu)}{\sqrt{(2)}\cdot\sigma} = \frac{2}{\pi}\int_0^x e^{-}t^2 dt$$

Threshold Scan - qualitative

- Not all the channels behave the same $\rightarrow$ no threshold distribution.
- Events loss at small Δ_{th} $\rightarrow$ lower limit of interval below baseline.



Possible improvements:

- fine tuning with local thresholds
- adjusting the baseline voltage

Summary

- Development of the JDRS is ongoing.
- Tools for first analysis of data from PASTA available.
- Overall behavior of the chip still unclear (e.g. channels behave differently).
- Need input from the experts on how to tackle this problem.

Outlook

- Calibration of the DAC for meaningful estimation of noise etc.
- Understand behavior of nasty channels.
- Continue analysis towards chip characterization.
- Continue developing JDRS with needed features.
- Implementation in the firmware of a test pulse with configurable phase shift wrt the clock.