Serial Adapter for I^2C / APFEL and 8 channel DAC ASIC

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Outline

Motivation

- Currently two different serial interfaces are foreseen to be used inside the barrel:
  - I^2C for High voltage DACs
  - APFEL serial configuration interface
- Both interfaces use single ended lines
  $\Rightarrow$ need ground connection $\Rightarrow$ Risk of ground loops
- Both interfaces are not compatible $\Rightarrow$ Requires additional cabling inside the magnet.

Wish for an adaptor circuit with additional analogue features raised up.

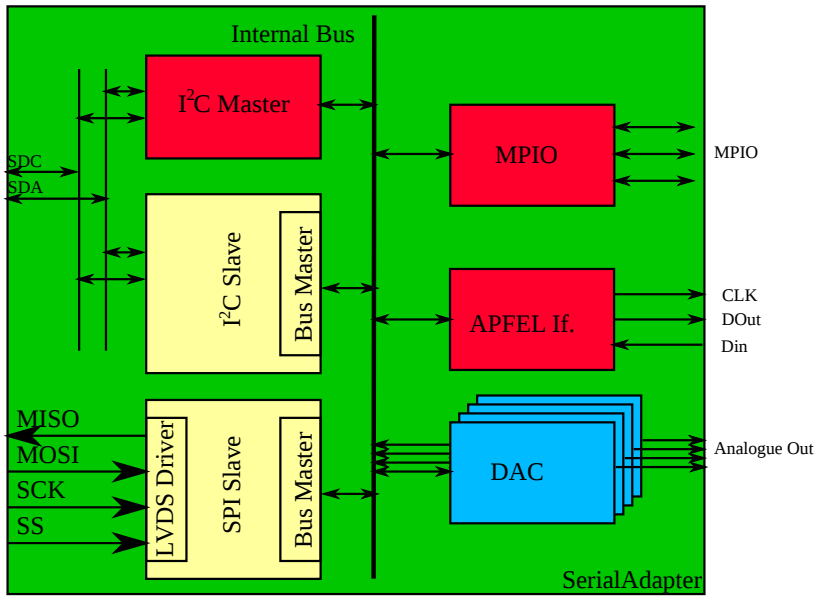
- Reuse of tested VHDL entities and available Analogue blocks
- Integration of 10 bit DACs for HV adjustment.
  $\Rightarrow$ Could also be interesting for End cap HV distribution

Outline

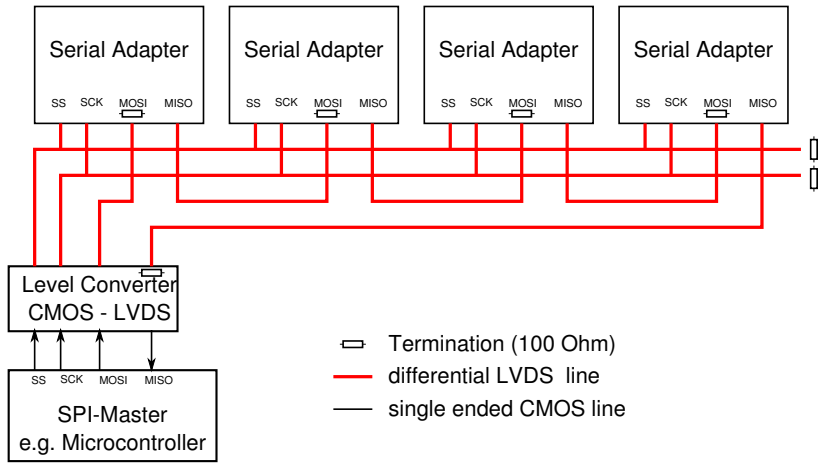
Chip Architecture

Global Architecture

Build an adaptor circuit with a common back end and front ends for I^2C, SPI and APFEL serial configuration interface



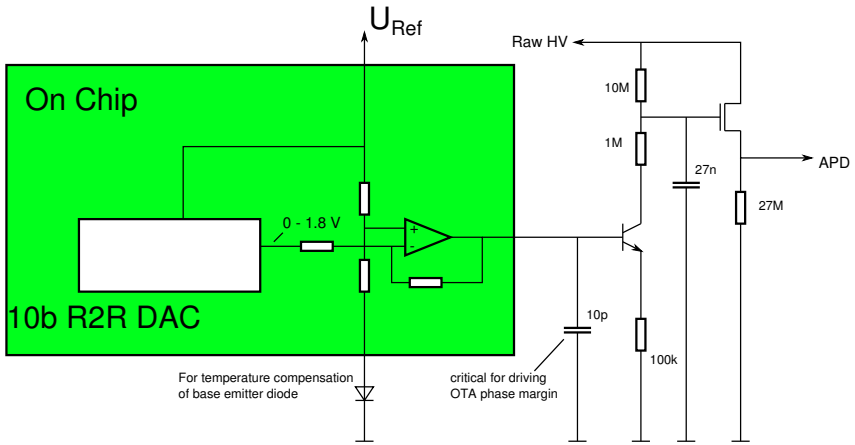
SerialAdapter Block Diagram



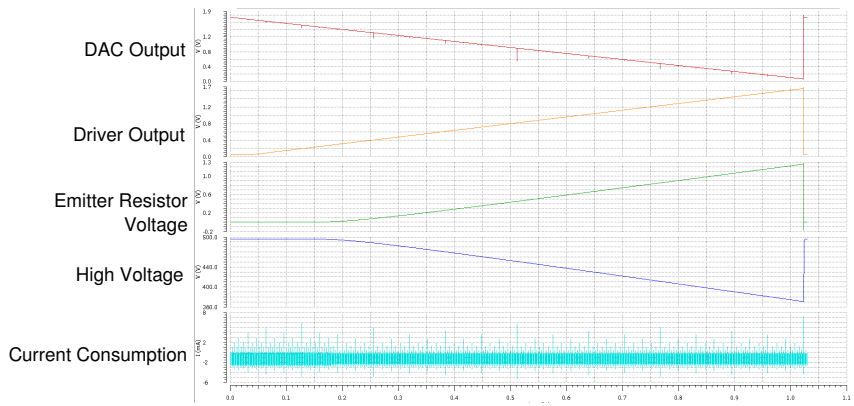
SPI back end connection

Chip Architecture

Analogue Part



Circuit of HV Adjustment

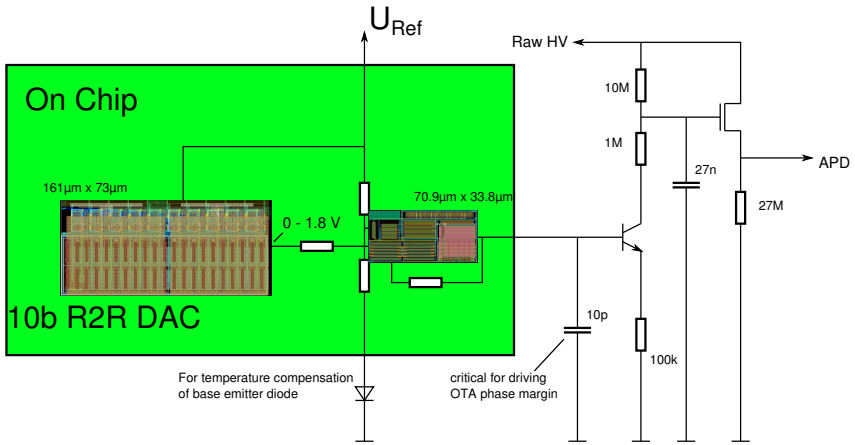


Spice Simulation

- 10 bit R2R DAC already used in several ASIC projects
- OTA design taken from HitDetection
- Same external circuit as on current HV distribution PCB

Chip Architecture

Analogue Part



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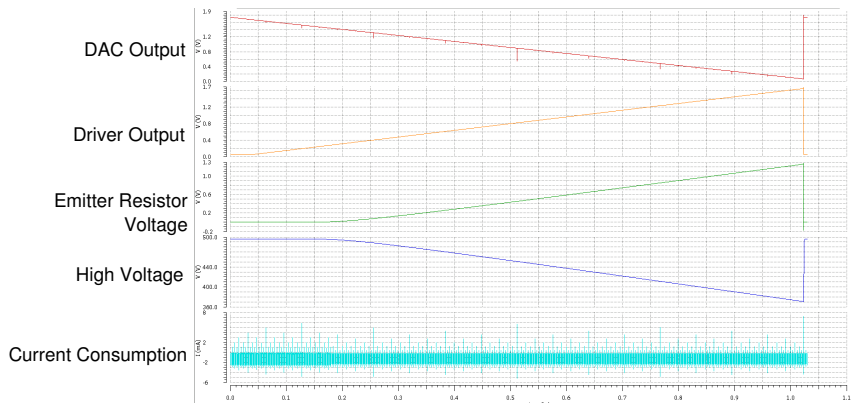

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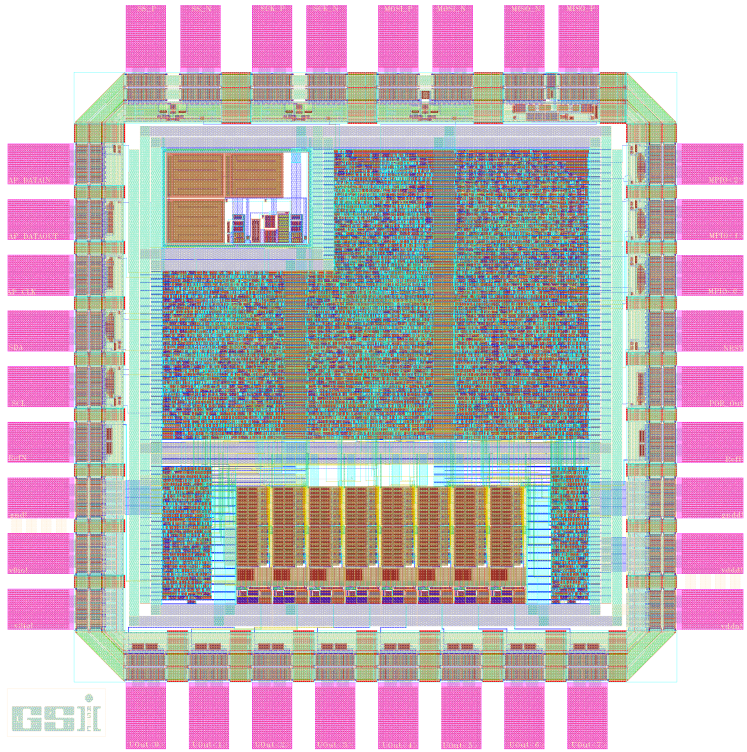
Status and Schedule

- First Idea: March 2016
- Project launch with financing by University of Bonn after September CM meeting in Mainz
- November 28th: Dead line for tape out
- Expected delivery in February 2017
- Packaging in QFN32 in early spring
- Prototyping costs: $\approx$ €5660



$1.5 \times 1.5\ \mathrm{mm}^2$ Mini ASIC in UMC 180 nm CMOS technology

Backup

Costs

- 1 Mini@sic Block

Number of Chips		Total costs	Packaging	Cost/chip
30	(min. number)	€3160	€2500	€188.67
180	(one slice)	€9660	€2500	€67.56
270		€16600	€2500	€106.11
4050	(full barrel)	€35050	€5000	€9.89

Digital Design Flow