SADC Status

Johannes Müllers
for the CBELSA/TAPS collaboration

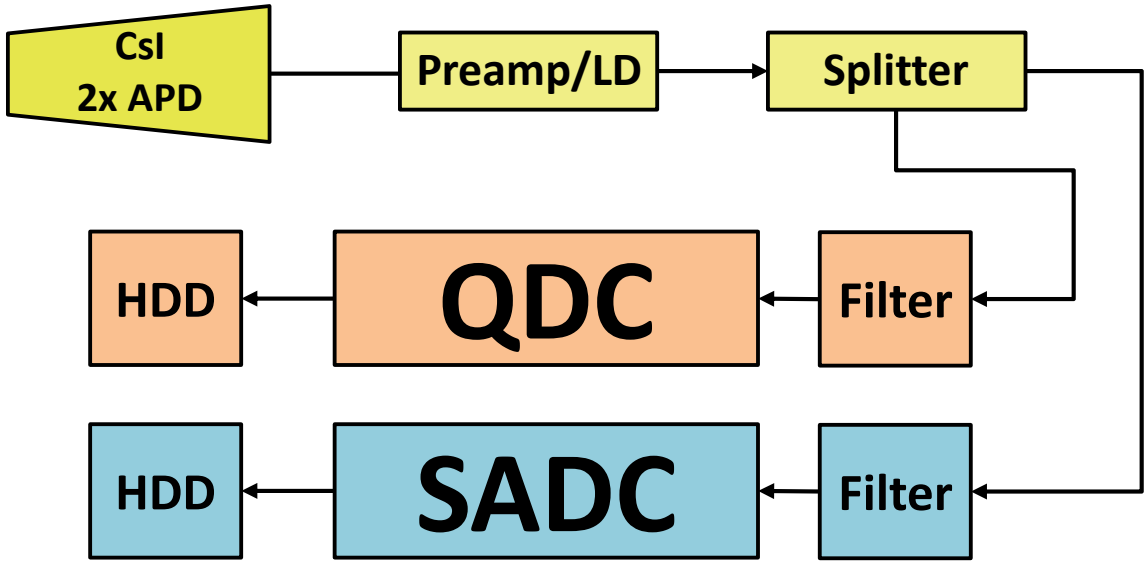
Contributors: Pawel Marciniewski (PANDA), Timo Poller, Christoph Schmidt, Jan Schultes, Ulrike Thoma, Georg Urff

Rheinische Friedrich-Wilhelms-Universität Bonn

Reminder

→ Upgrade of
Filter + Digitization
(PHD thesis)

→ First runs:
old and new stages
run in parallel

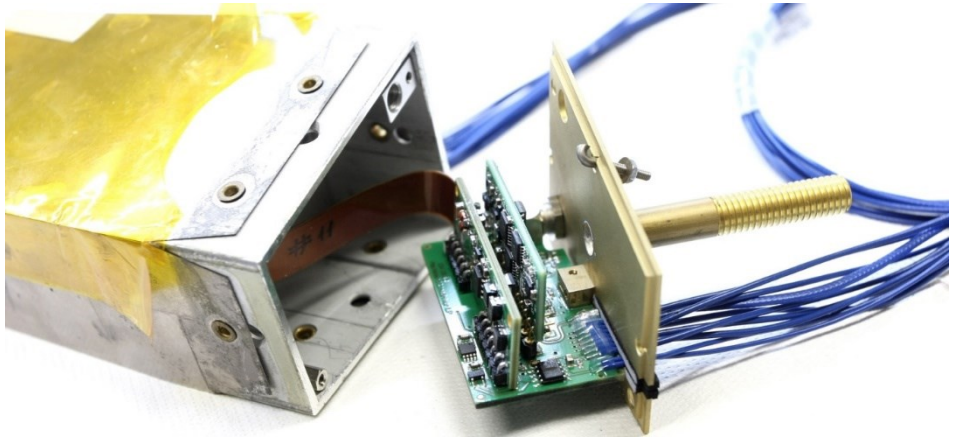


Aims:

→ Faster readout

→ Separate uncorrelated
cluster hits

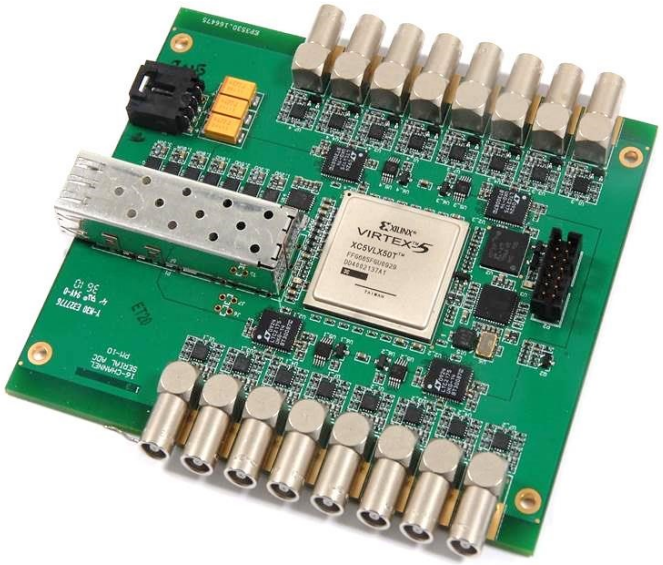
→ Pileup recovery

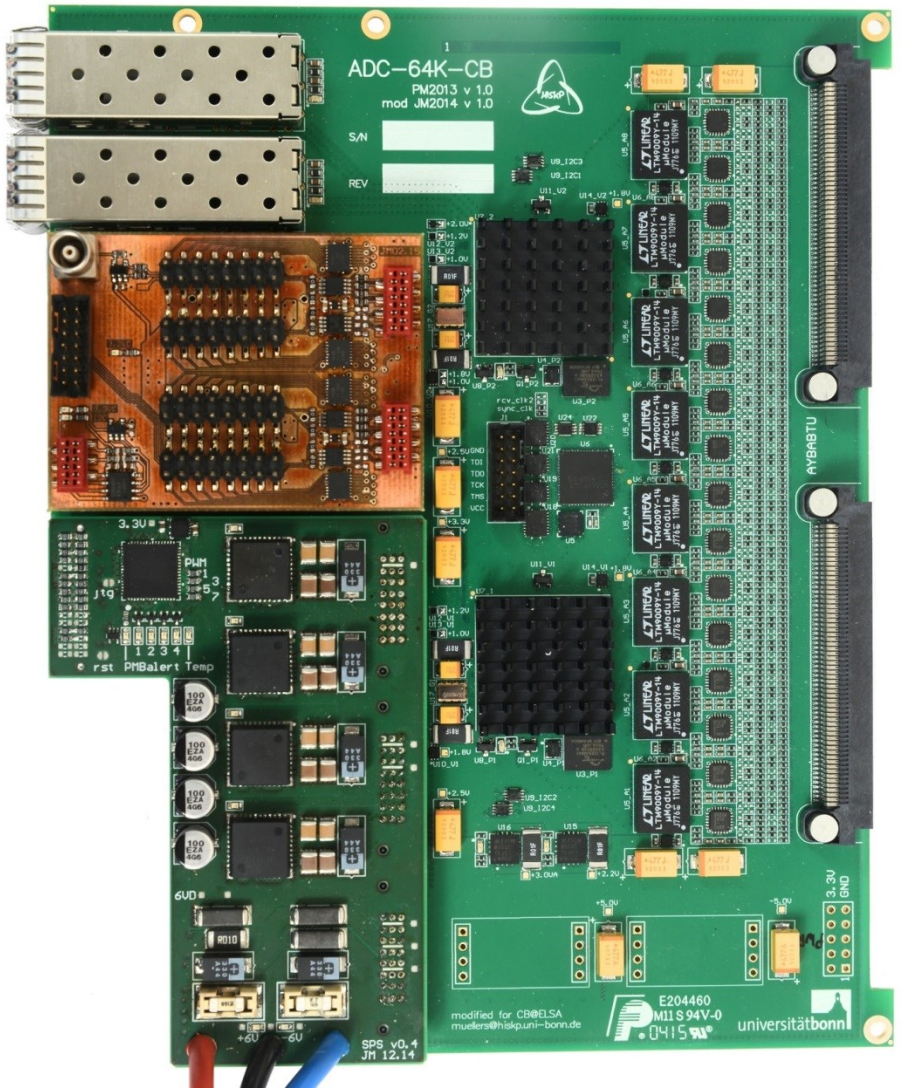


Reminder

(Dev.: P. Marciniewski for the PANDA collaboration)

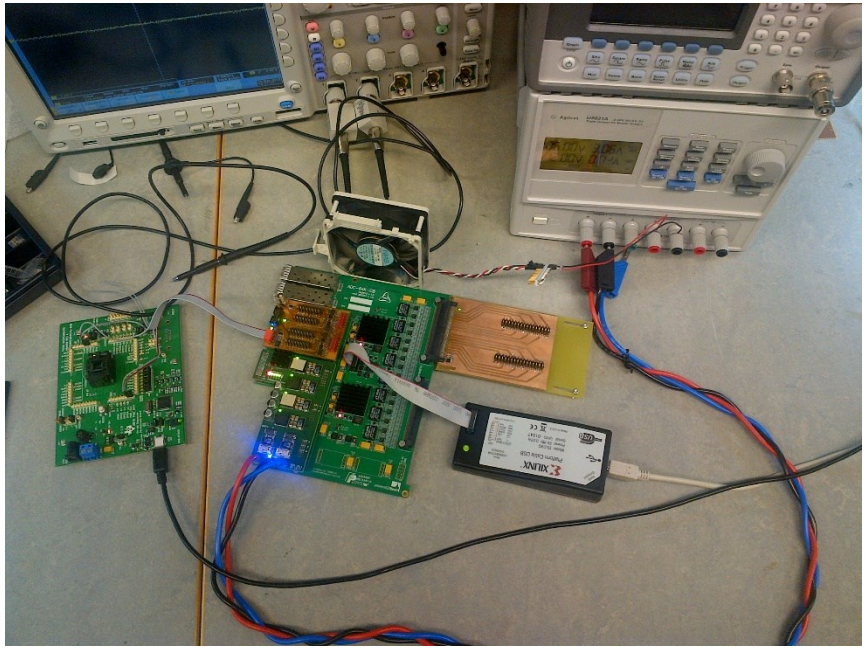
- **Q1..Q2/2015:**
  Test of 16ch Prototype
- **Q3..Q4/2014:**
  Modification of 64ch Prototype
- **Q2/2015:**
  Arrival of 64ch Prototype



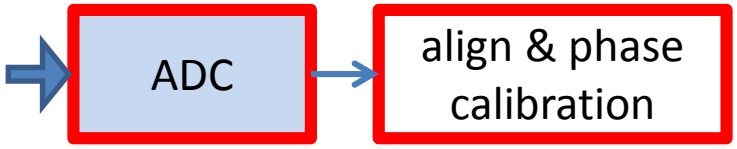


SADC Development in 2015

- **SADC has been tested in the lab**
- **Prototype was working (minor bugs)**
- **Auxiliary hardware was working (Power supply, Slowcontrol)**
- **Trouble with „scrambled data“**



Phase Calibration & Alignment



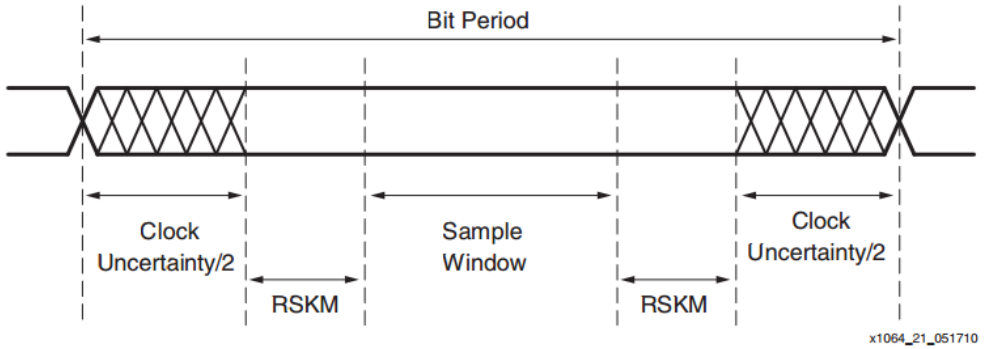
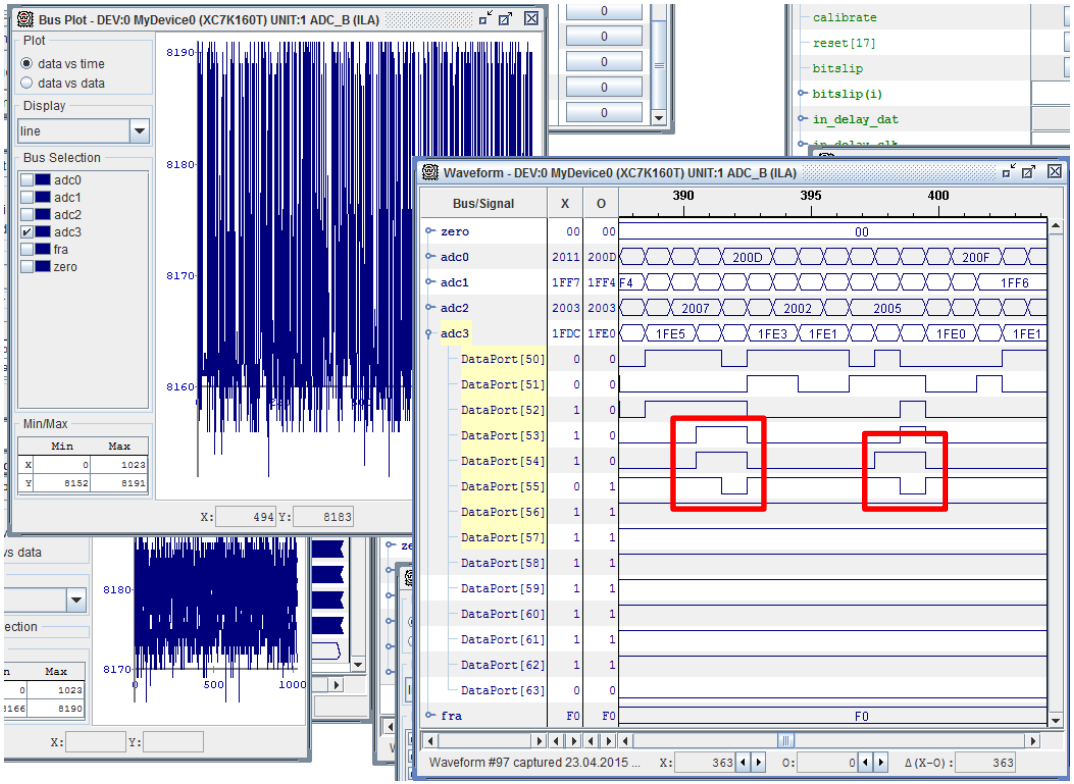


Figure 21: **Receiver Skew Margin**

- **Serialized data needs phase calibration**
- **CLOCK and DATA signals need to be aligned (different signal paths)**
- **Xilinx Example Design very complex**
- **Own solution very simple (yet working)**



Phase Calibration & Alignment

ADC programmed to send fixed pattern

find unstable configuration (delay += 72 ps)

calculate safe configuration

Alignment (3303 → 3330) „Bitslip“

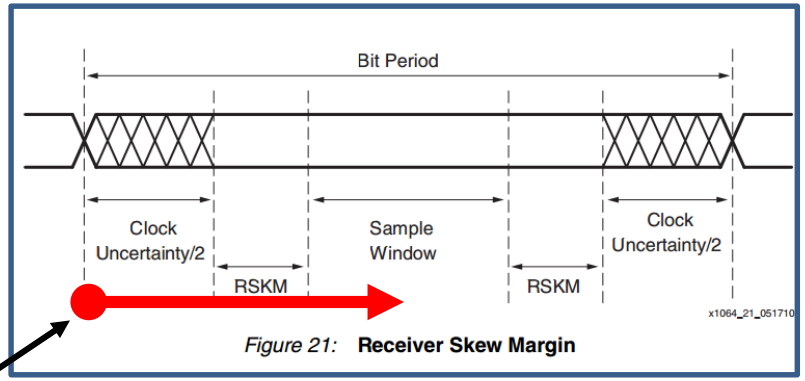
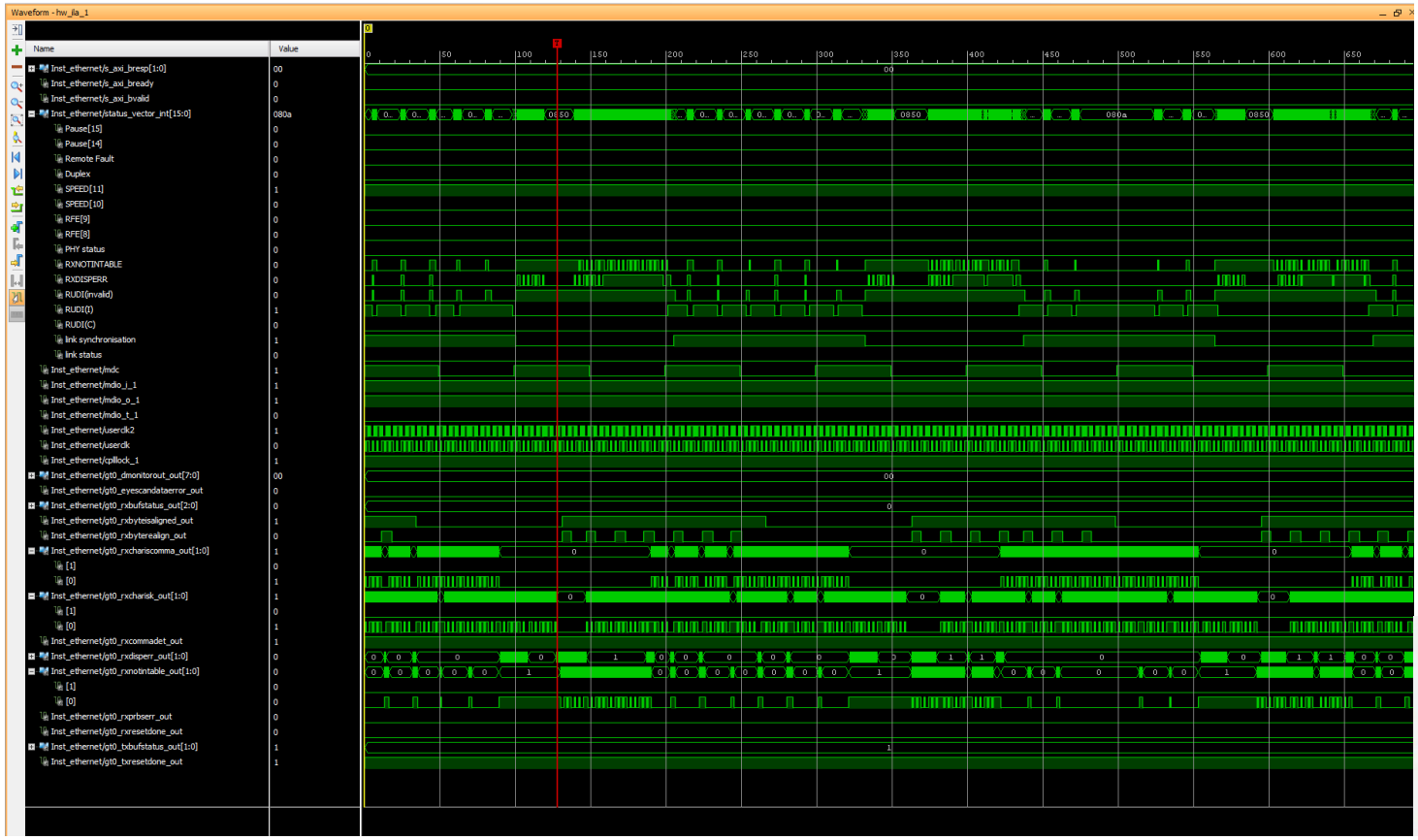


Figure 21: **Receiver Skew Margin**

delay | data

Network Implementation

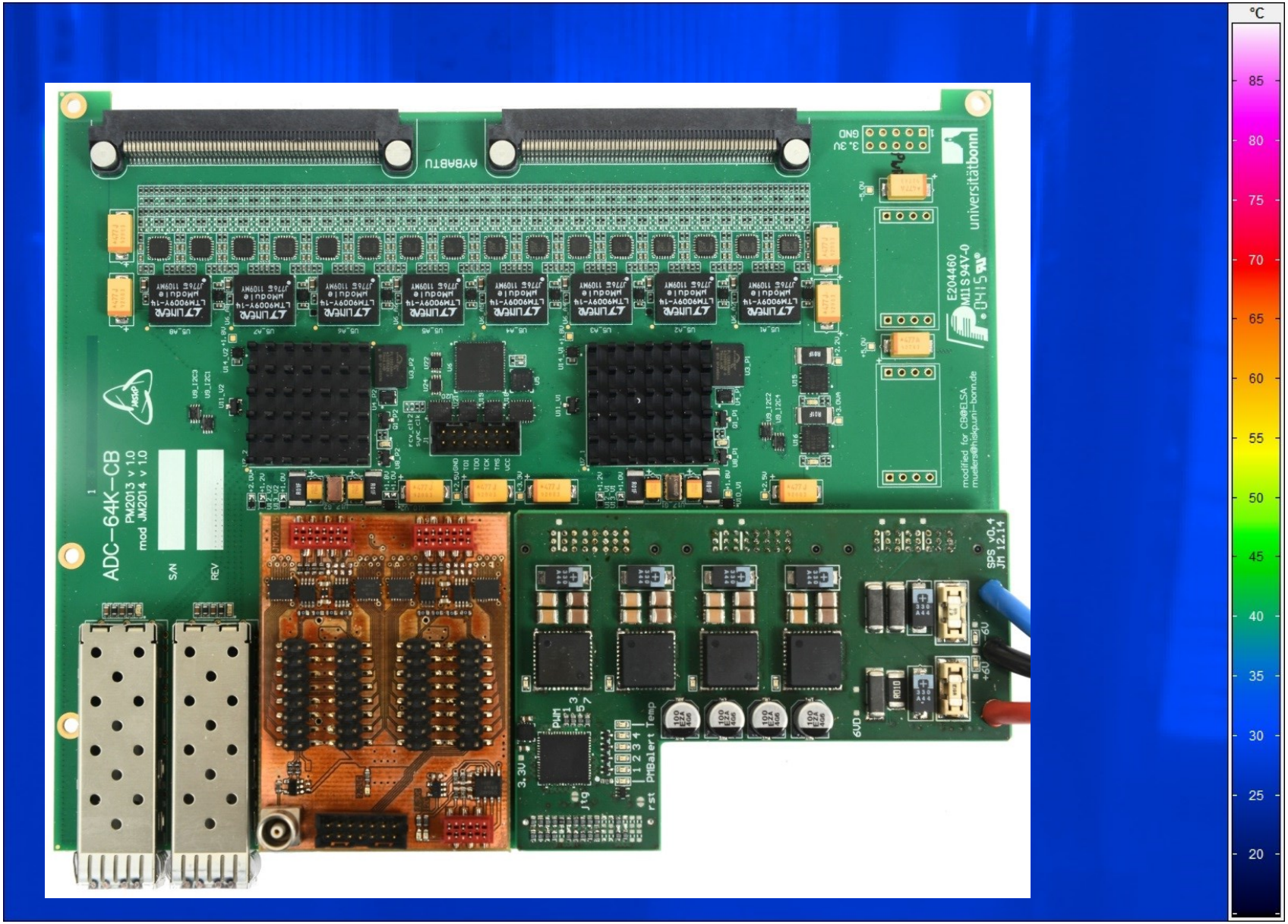
- SADC has 2 SFP ports (Copper / Fiber)
- can be used for Ethernet, Fibrechannel, PCIe, Aurora, … you name it
- Ethernet implemented already on 16ch SADC (only MAC)
- UPD/IP from OpenCores.com implemented



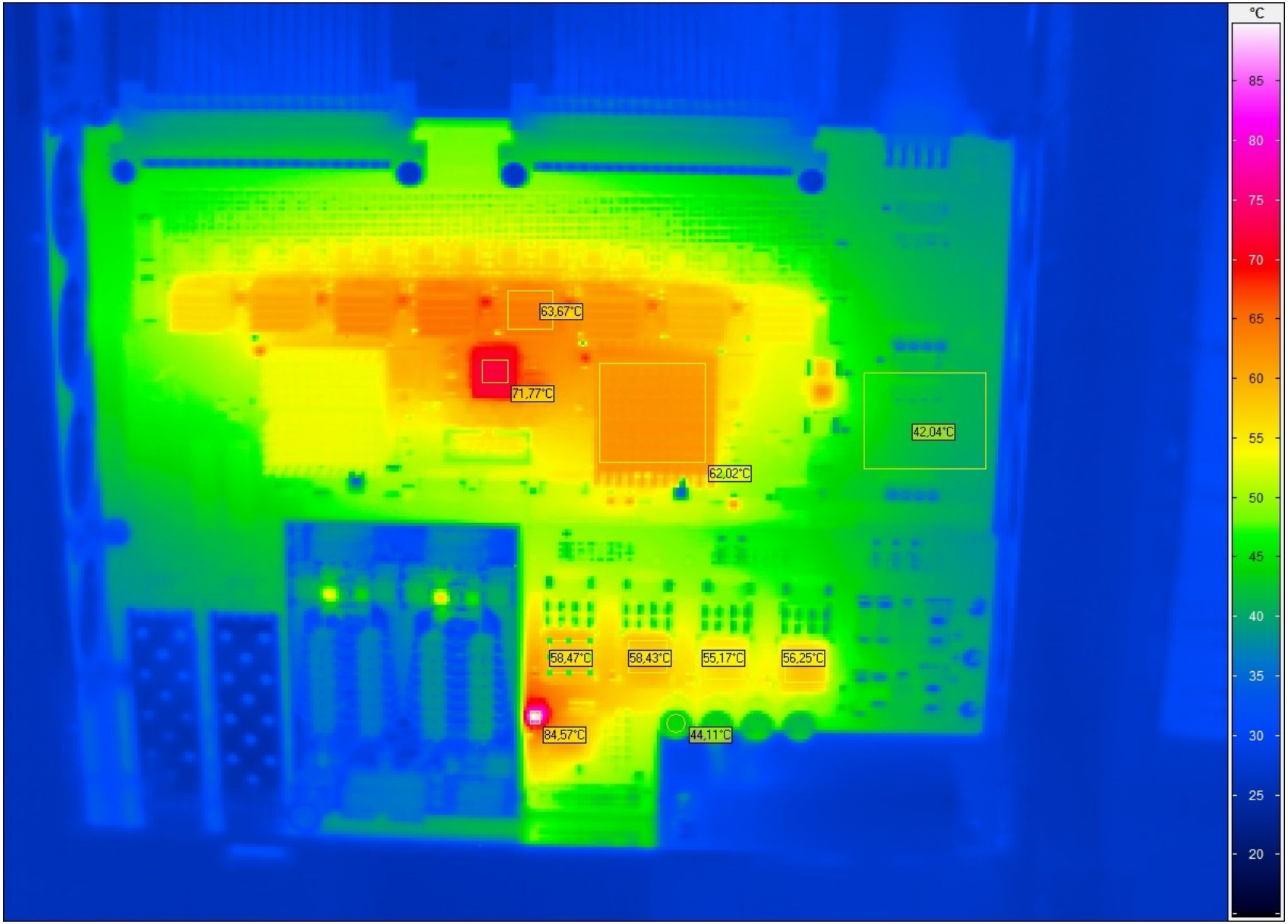
SADC moved (Lab → Real World)

- „SADC Prototype Rack“:
  - IBM x3650 Server
  - NIM Crate with SADC + Slowcontrol
  - Gigabit Ethernet Switch
  - FPGA Programmer
  - …
- Setup moved to Neunerblock (Q4/2015)

Cooling

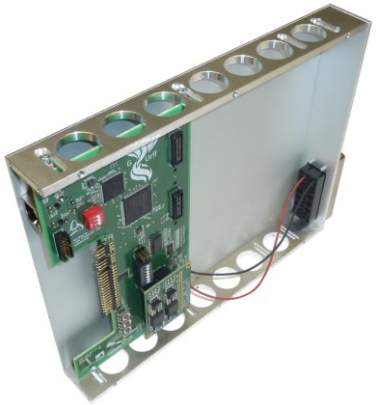

°C
85
80
75
70
65
60
55
50
45
40
35
30
25
20
ADC-64K-CB
PM2013 v 1.0
mod JM2014 v 1.0
S/N
REV
universitätbonn
E204460
modified for CB@ELSA
mueller@hiskp.uni-bonn.de
SPS v0.4
JM 12.14
PMBalert
Temp
rst
jtg
3.3V
6VD

Cooling


°C
85
80
75
70
65
60
55
50
45
40
35
30
25
20
63,67°C
71,77°C
62,02°C
42,04°C
58,47°C
58,43°C
55,17°C
56,25°C
84,57°C
44,11°C

Slowcontrol Module

- Master thesis Georg Urff
- Slowcontrol of SADC
  (voltages, currents, temperatures)
- Configuration of periphery
  (adjustable baseline, …)
- Managment of Trigger / Busy / Reset / …



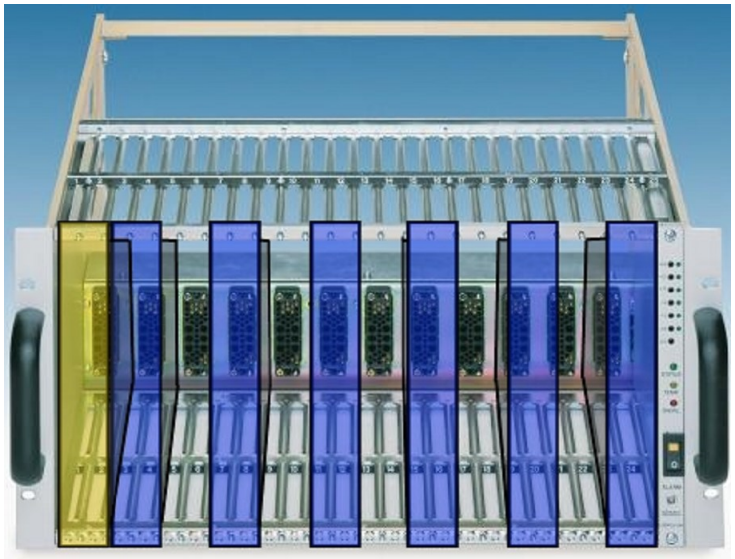
- Architecture:
  - Spartan 6 LX9
  - Dedicated 100 Mbit/s Ethernet IC

- Prototype finished in Q3/2015
- Now: Programming of Slowcontrol Daemon
  with Telnet and SQL access

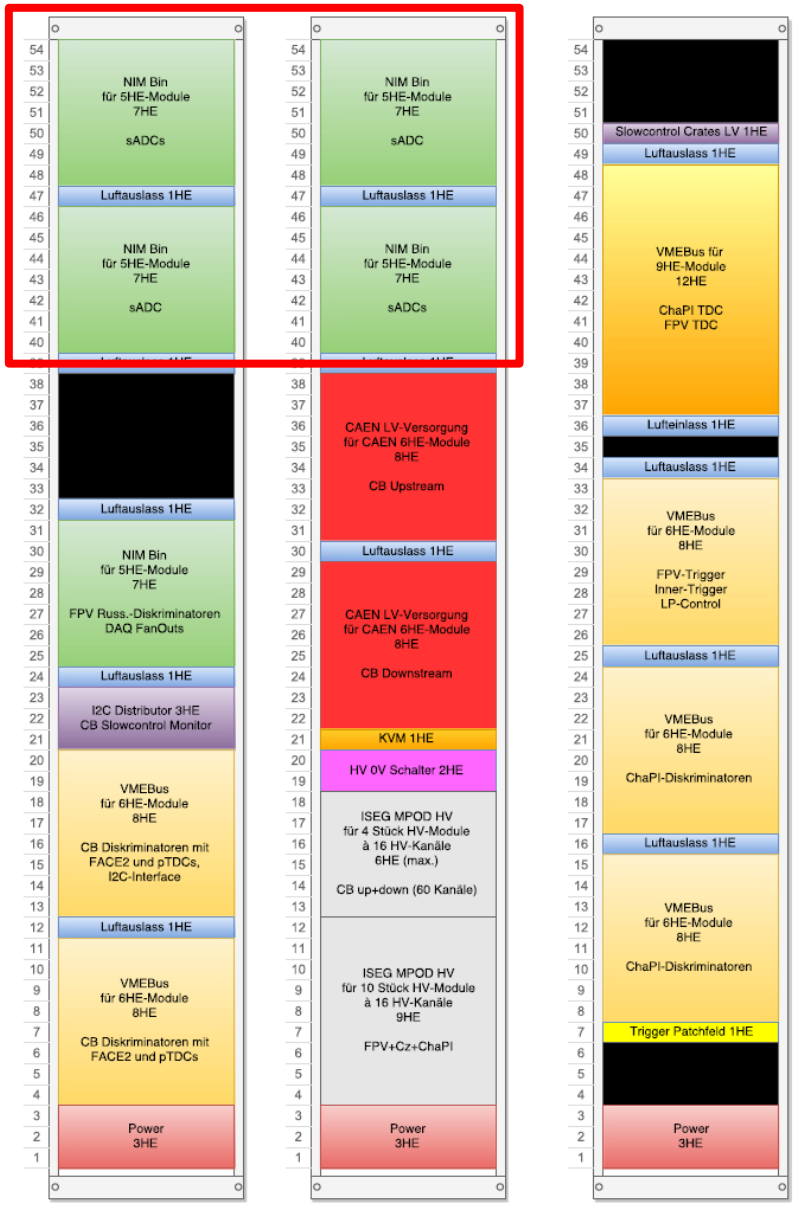
Poster HK45.72

Installation in CB Area

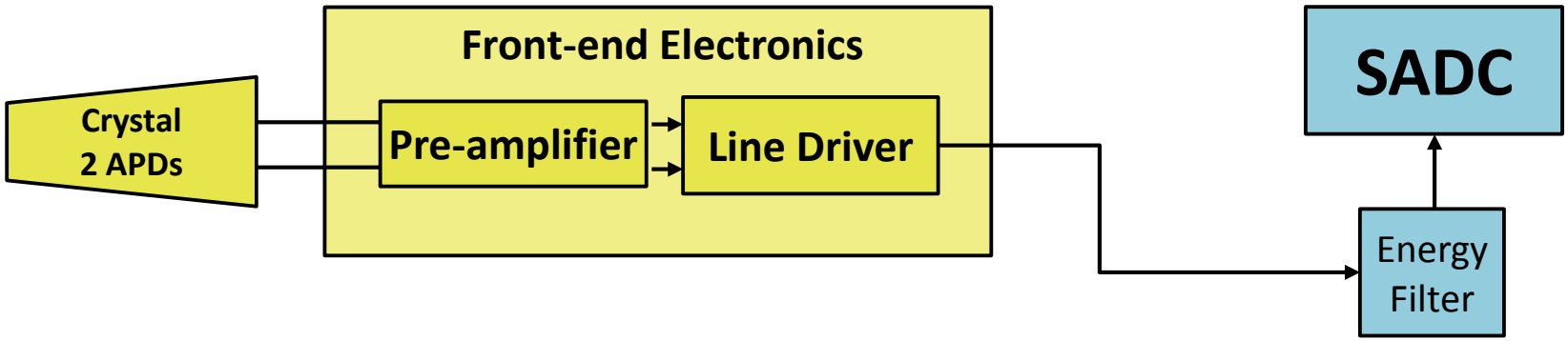
- 4 NIM Crates (12 slots each)
- 24 SADCs for Barrel
  → 6 per Crate + Slowcontrol
- COULD fit in 2 NIM Crates BUT:
  - Slowcontrol has to be moved (Back of crate? Redesign!)
  - Cooling?
  - Cabling?



- Dual range setup?...

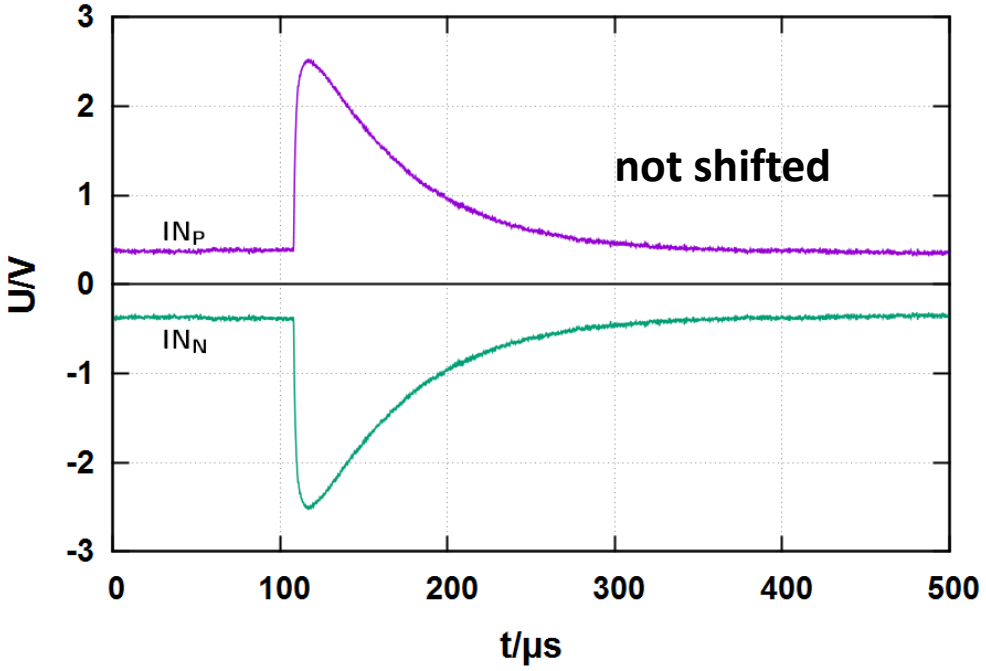


Baseline Shifter

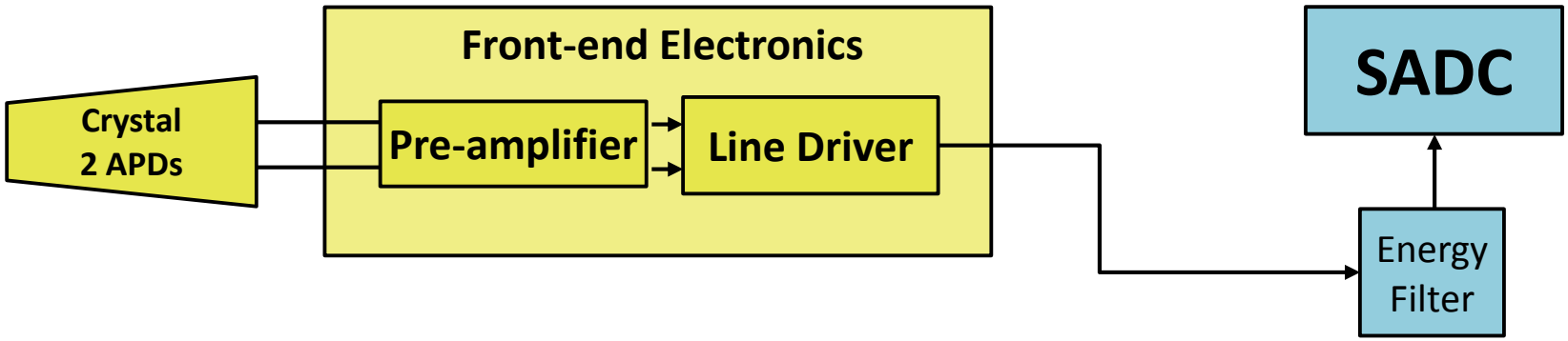


- Differential signal transfer
- <u>Unipolar difference</u>

- Low losses in parallel termination
- Half scale of SADC (13 bit)

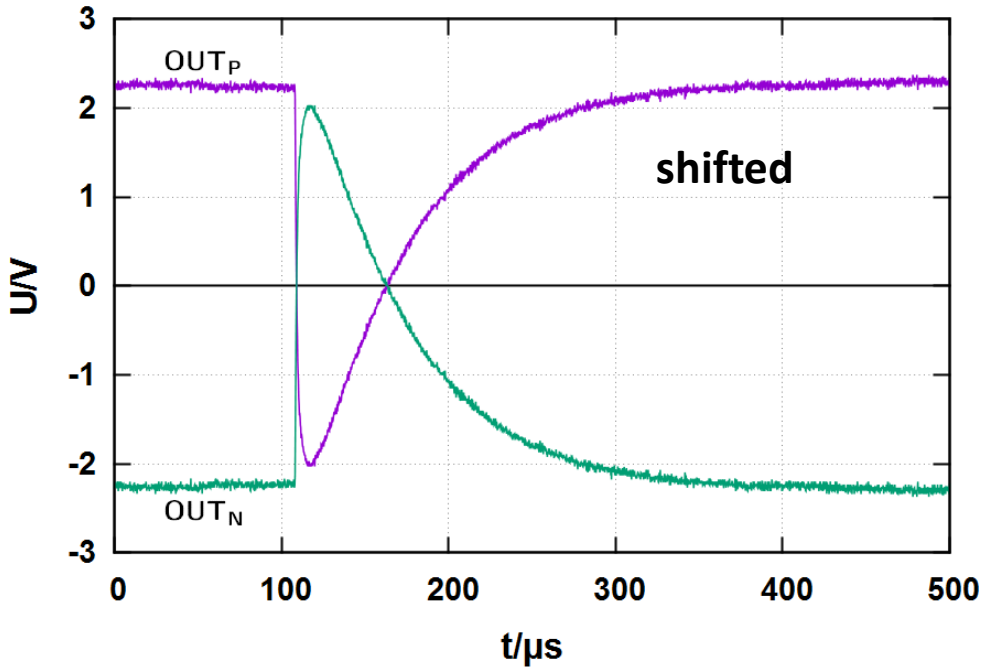


Baseline Shifter



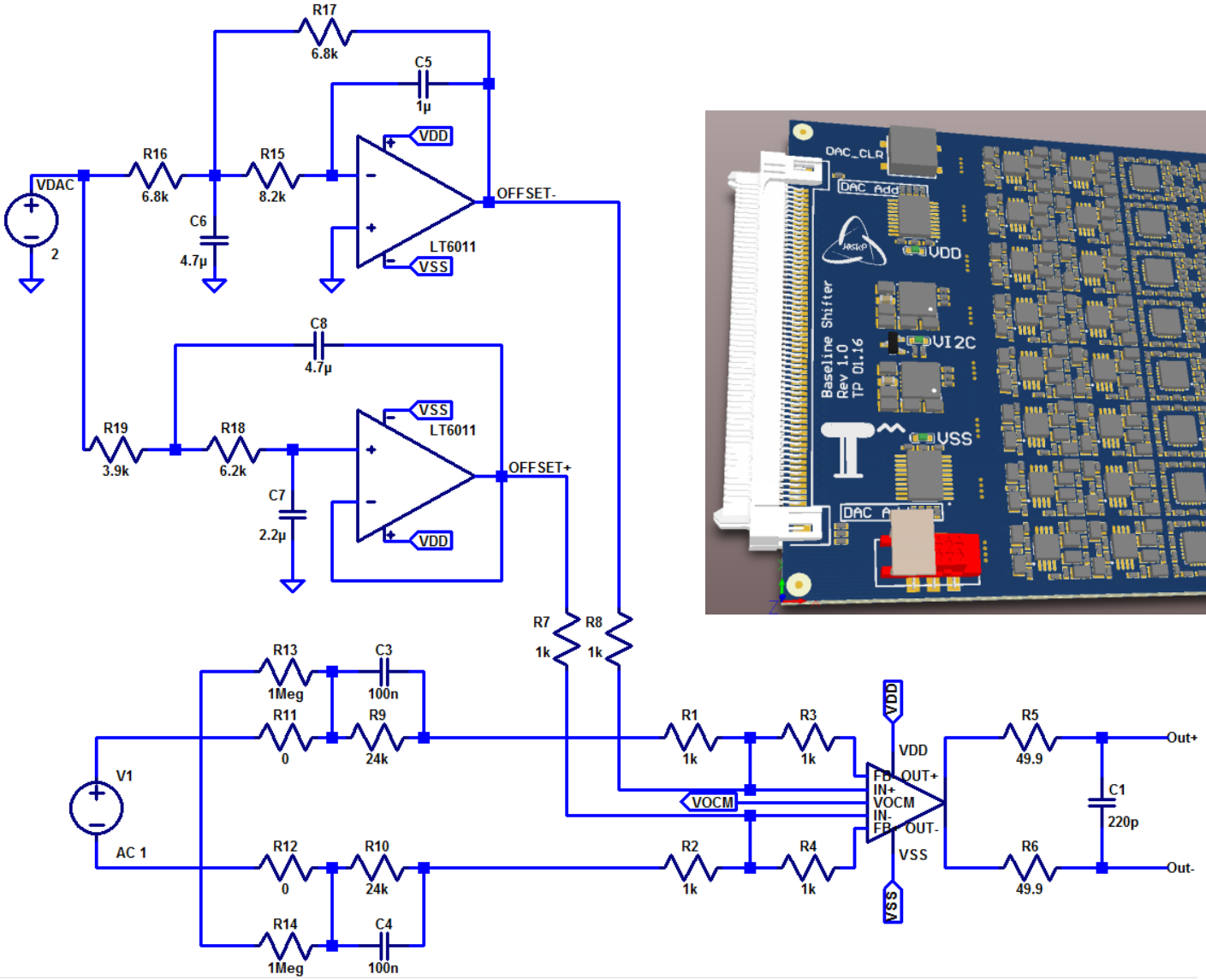
- Differential signal transfer
- Bipolar difference

- Use series termination
- Full scale of SADC (14 bit)



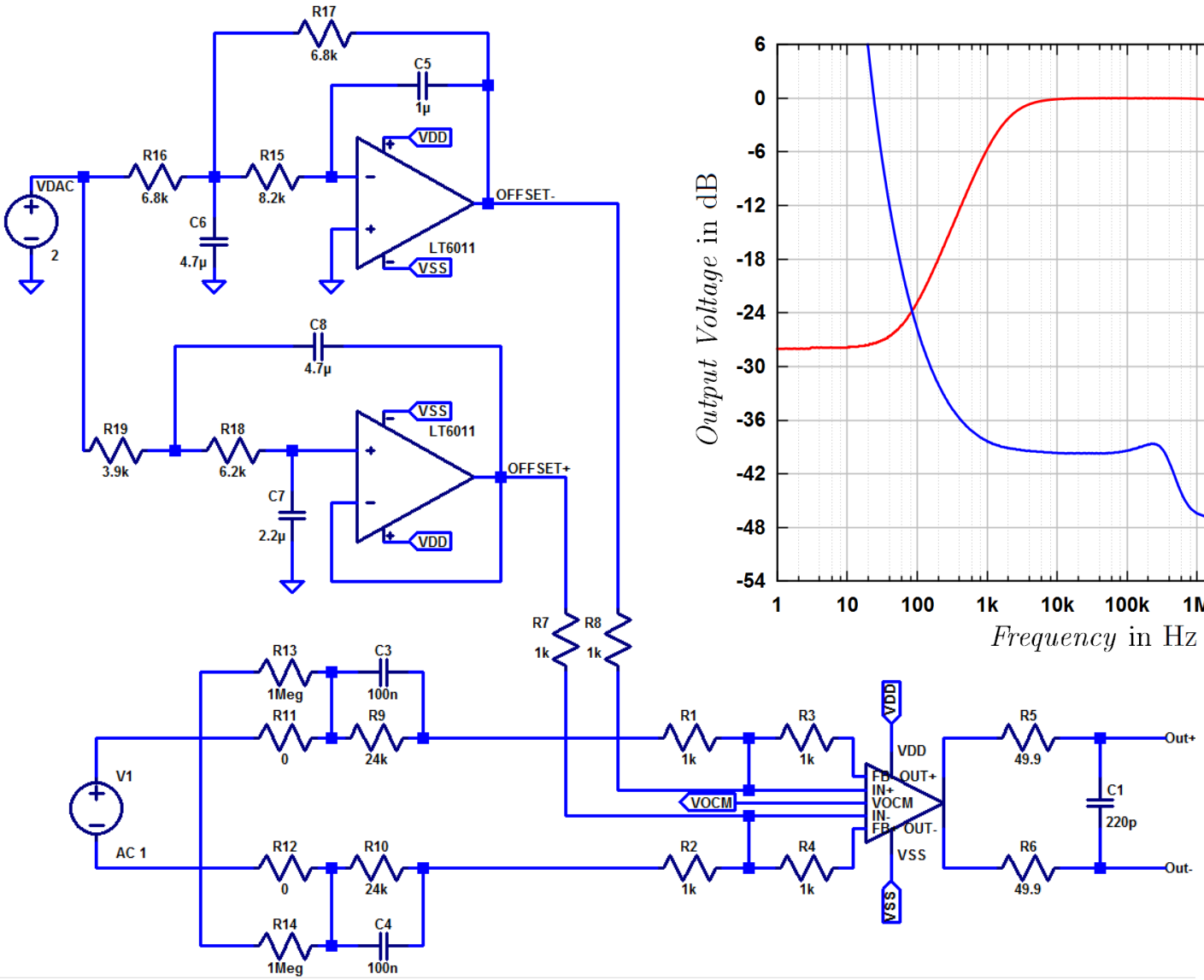
Baseline Shifter

(Timo Poller, Poster HK45.72)



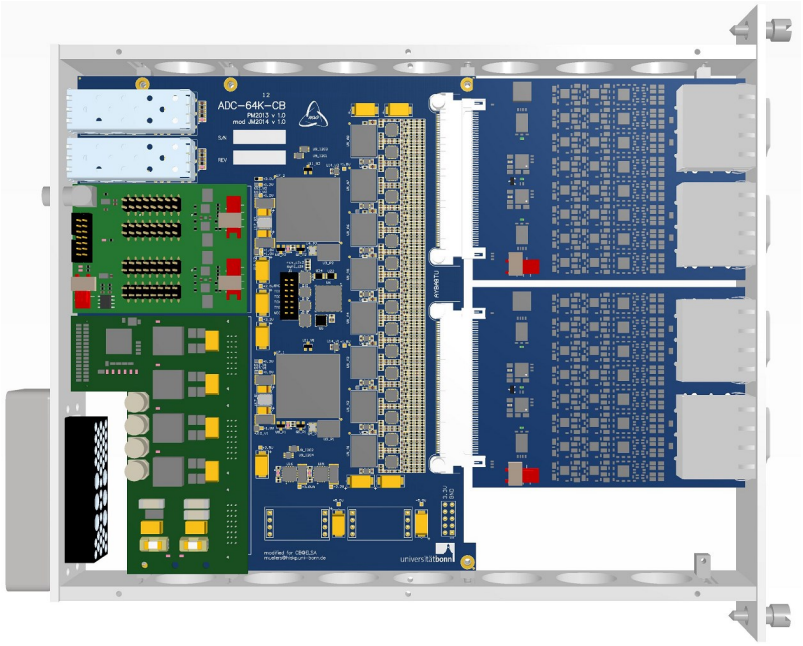
Baseline Shifter

(Timo Poller, Poster HK45.72)



Summary & Outlook

- **Send new (final) prototype to production Q2/2016 (Marciniewski/Müllers)**
- **Work on Backplane for SADC interconnection (Schweitzer/Müllers)**
- **Work on analog/digital filters (Poller/Müllers)**
- **Work on feature extraction (Schultes/Müllers)**
- **Work on Software Backend (Schultes/Schmidt)**
- **Work on Slowcontrol Daemon (Urff)**



Ende

Thank you for your attention!

Questions?

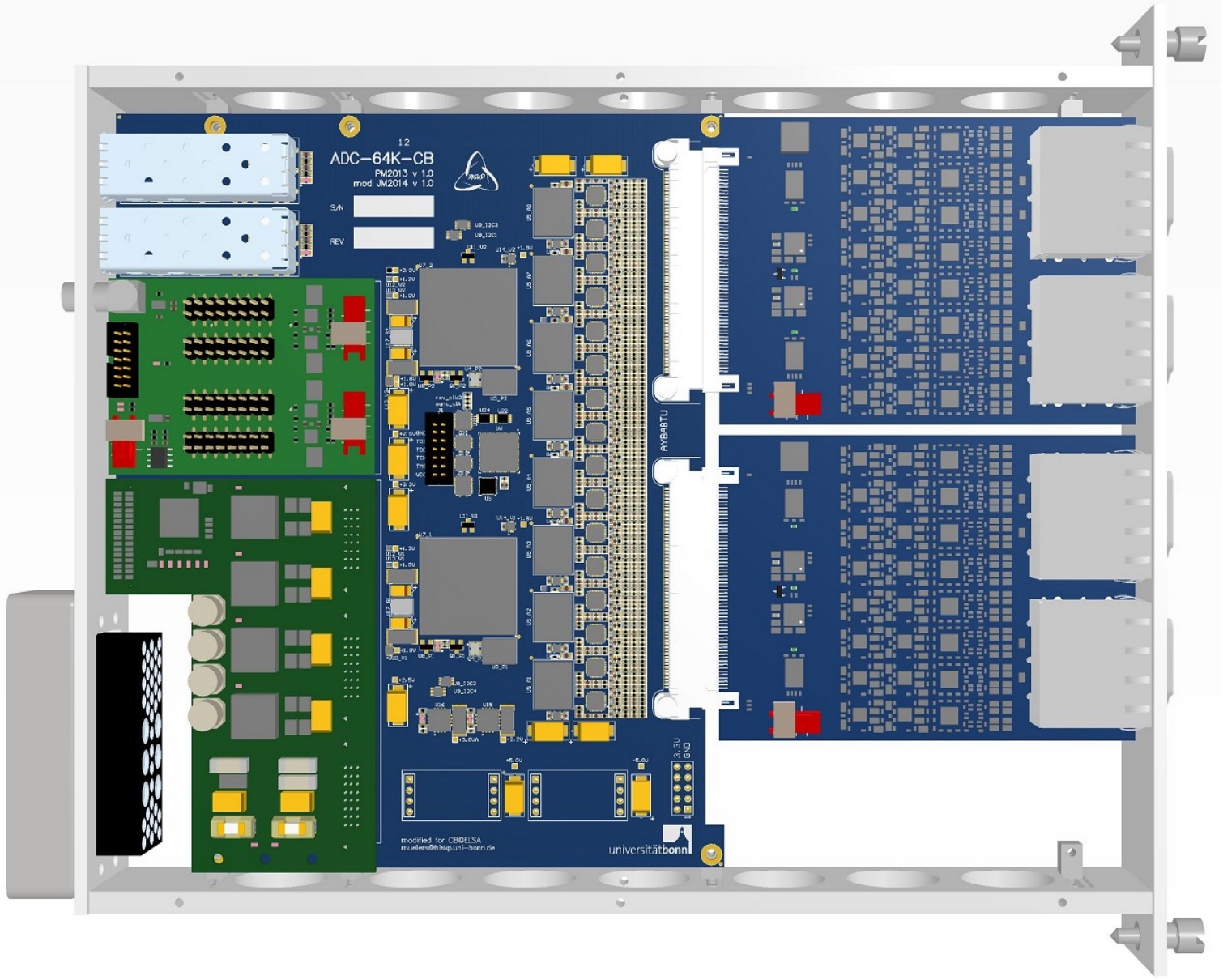
Outlook

CB Meeting 2015

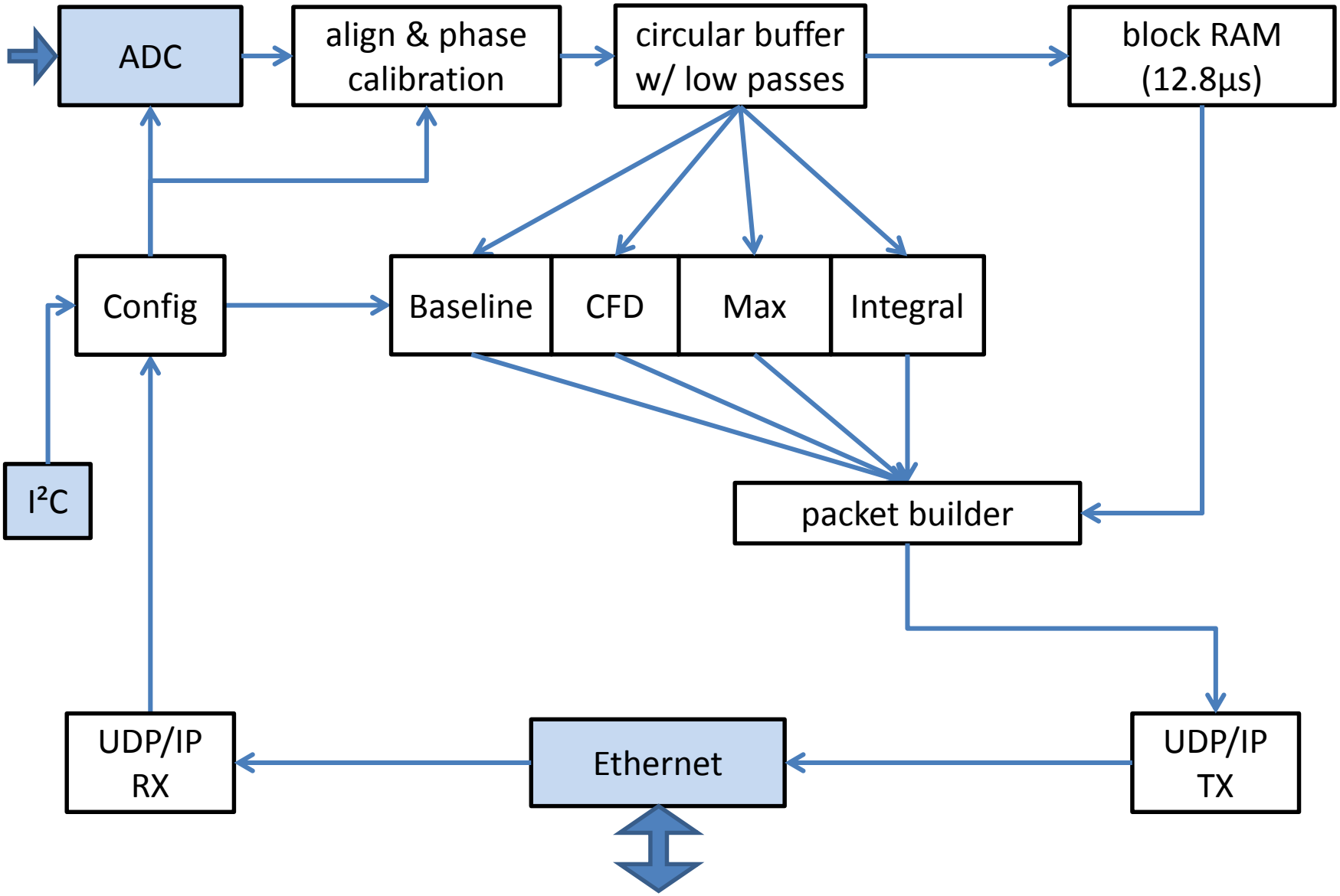
- → Pick up CB-SADC64 (tomorrow)
- → Electrical testing (Q2)
- → FPGA design (Q2..Q3)
- → PCB design for next prototype / final revision (Q2..Q4)
- → Series production & installation in experiment (2016)

Thank you

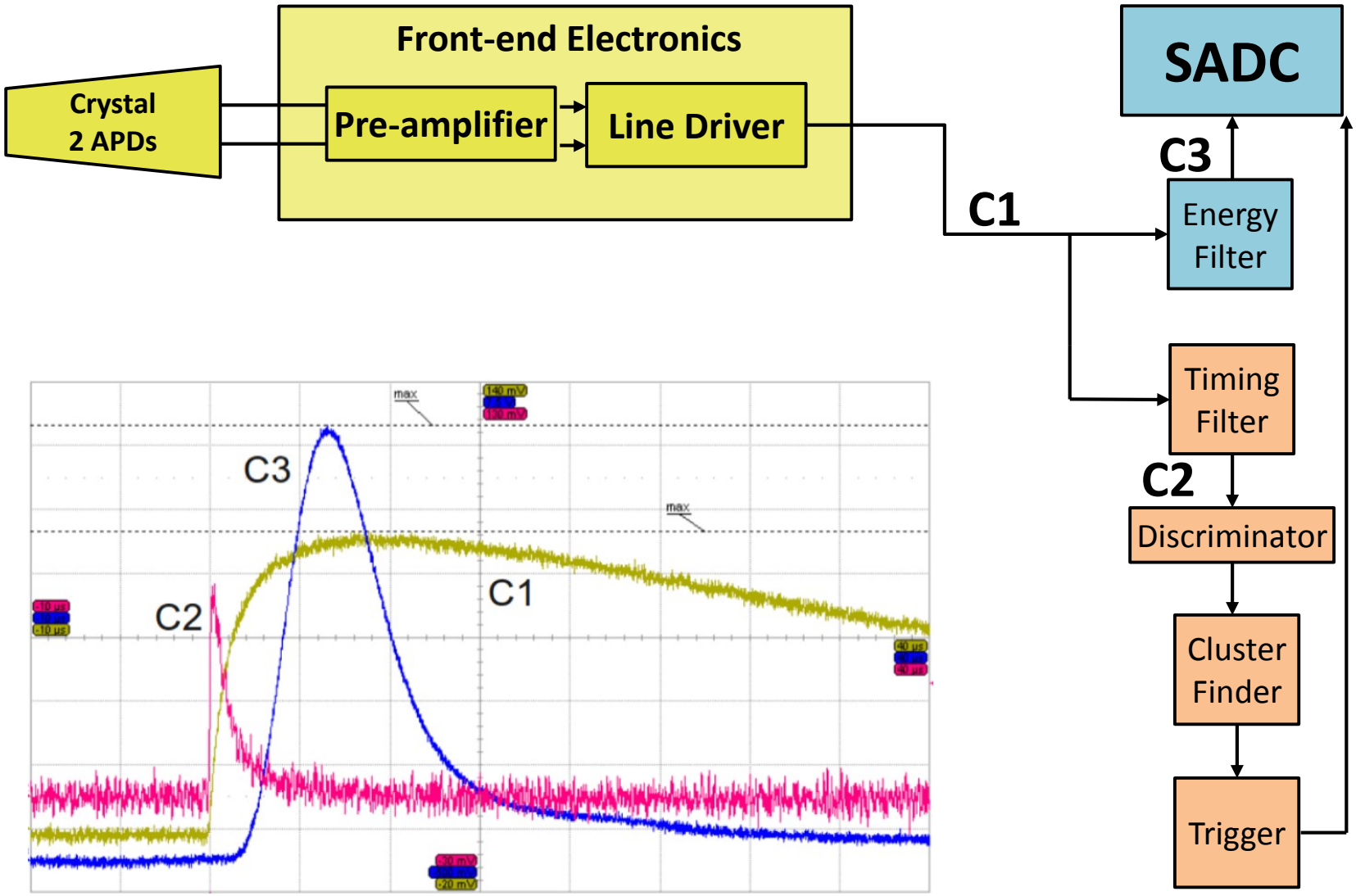
SADC (CAD)



VHDL (FPGA) Design

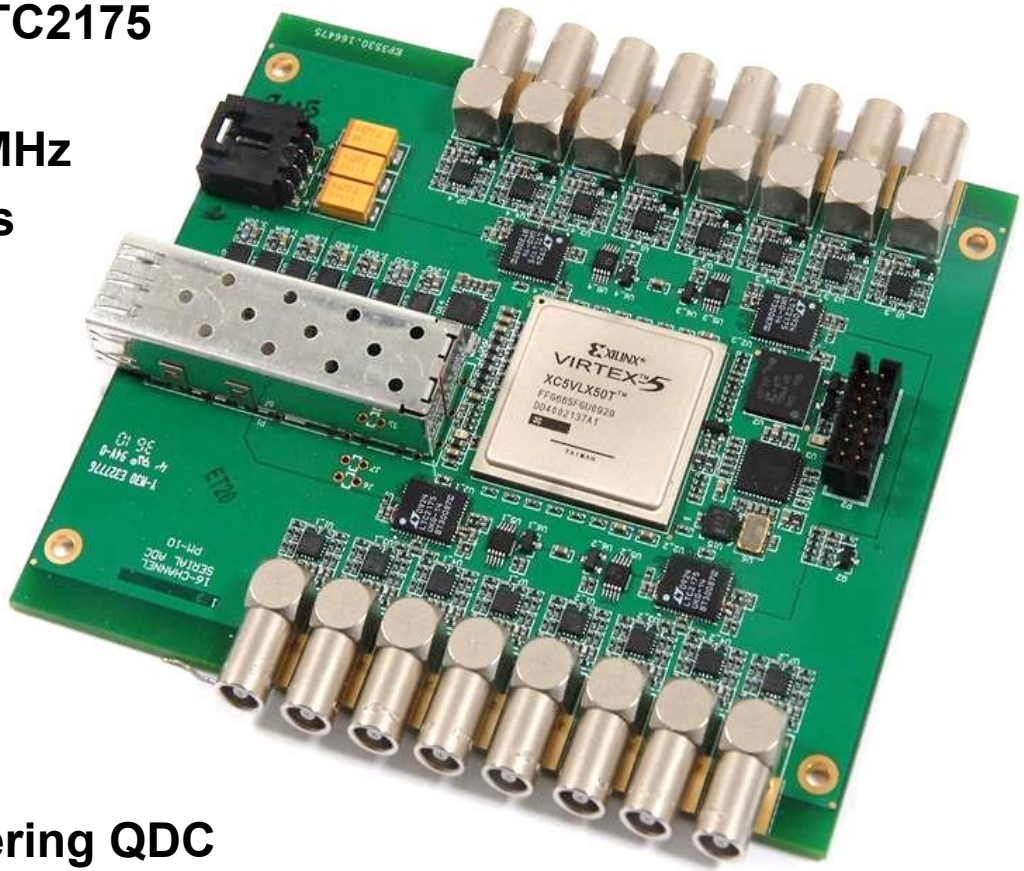


Signal Transfer



First prototype (16 channels)

- Developed as prototype for PANDA (P. Marciniewski)
- ADC: Linear Technologies LTC2175
  14bit, 125MHz, 4 channels
- Xilinx Virtex-5 LX50T @ 125MHz
- 16 single ended LEMO inputs
- SFP Interface



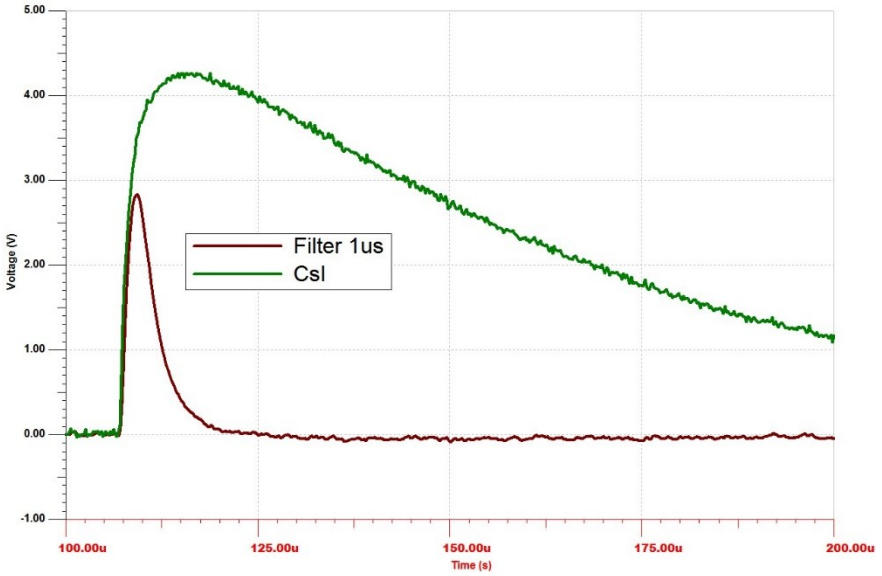
- Overall satisfying results
- Implementation of self-triggering QDC
  with Gigabit Ethernet
- but: needed higher channel density

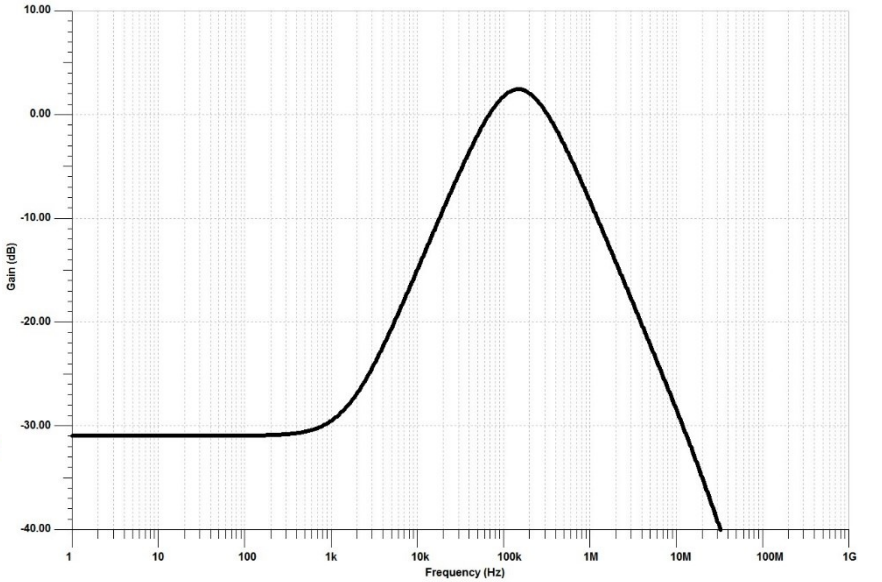
Onboard analog shaping

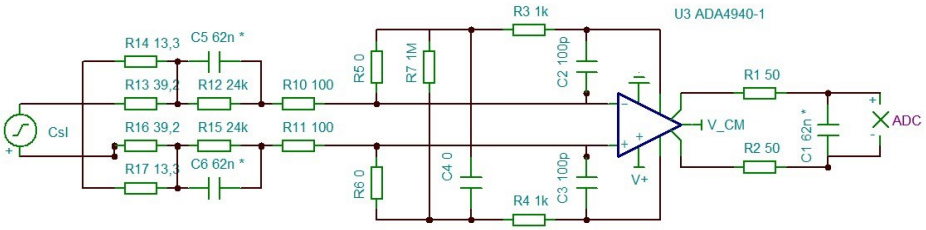
Analog input stage of SADC:
- → **passive highpass (with PZ cancellation)**
- → **quasi-3pole lowpass**

Will be used for
- → **CRRC shaping**
- → **Aliasing-filter for ADC (LP)**

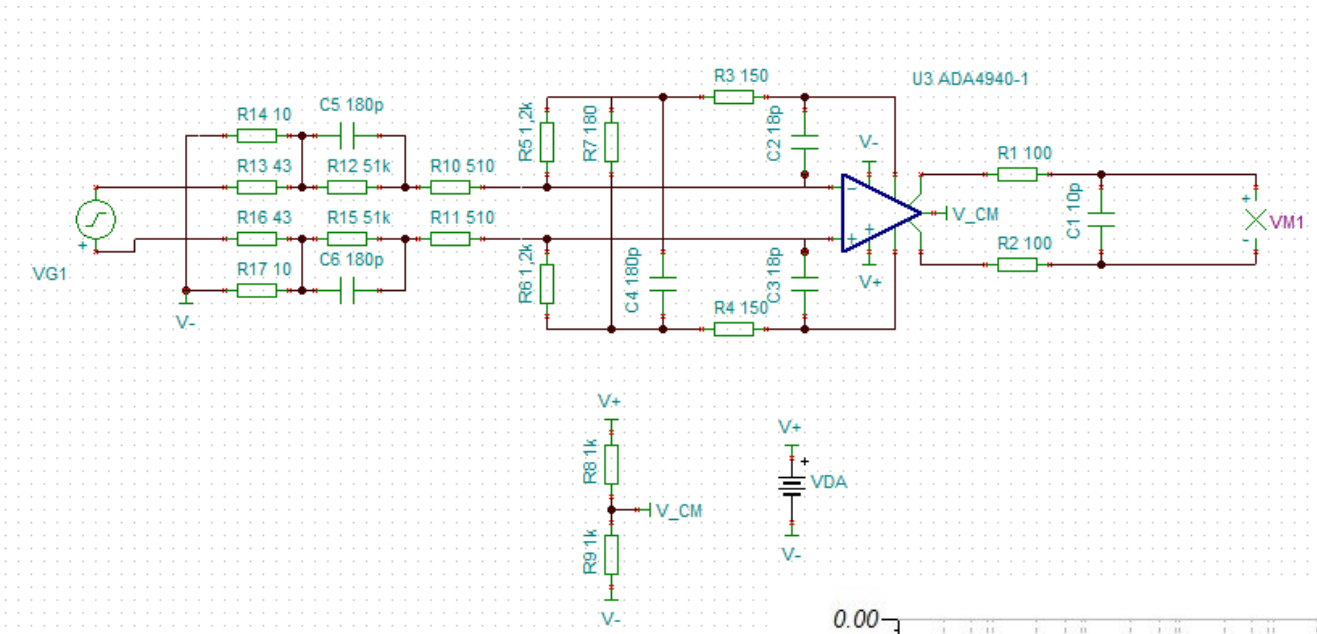
In prototype:
- → **Attenuating input buffer with aliasing filter**
- → **reconfiguration possible**

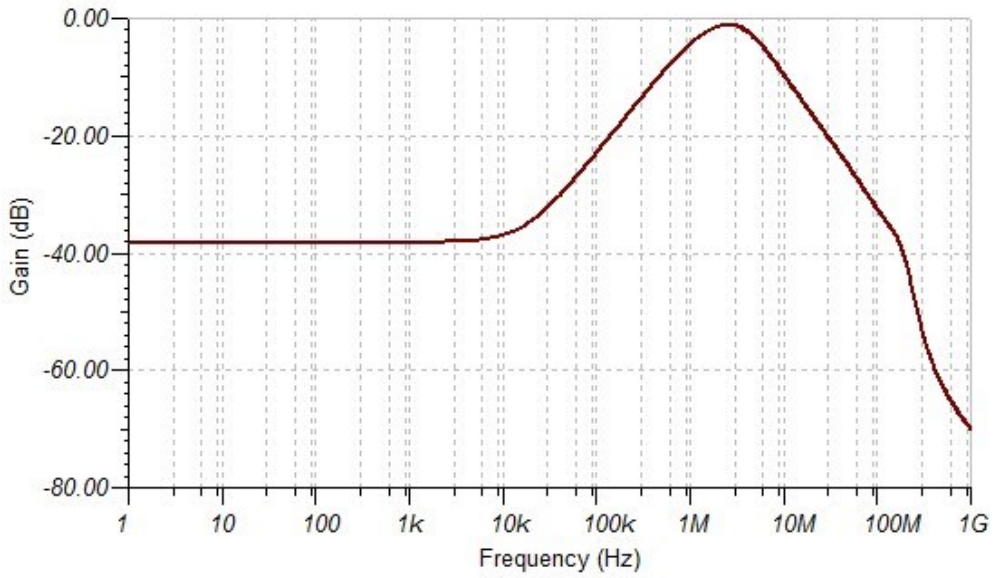






SADC Analog-Filter (PANDA)



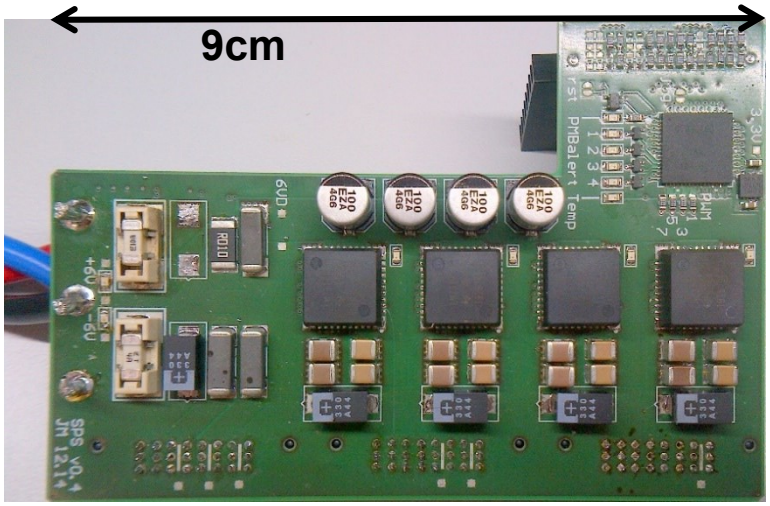


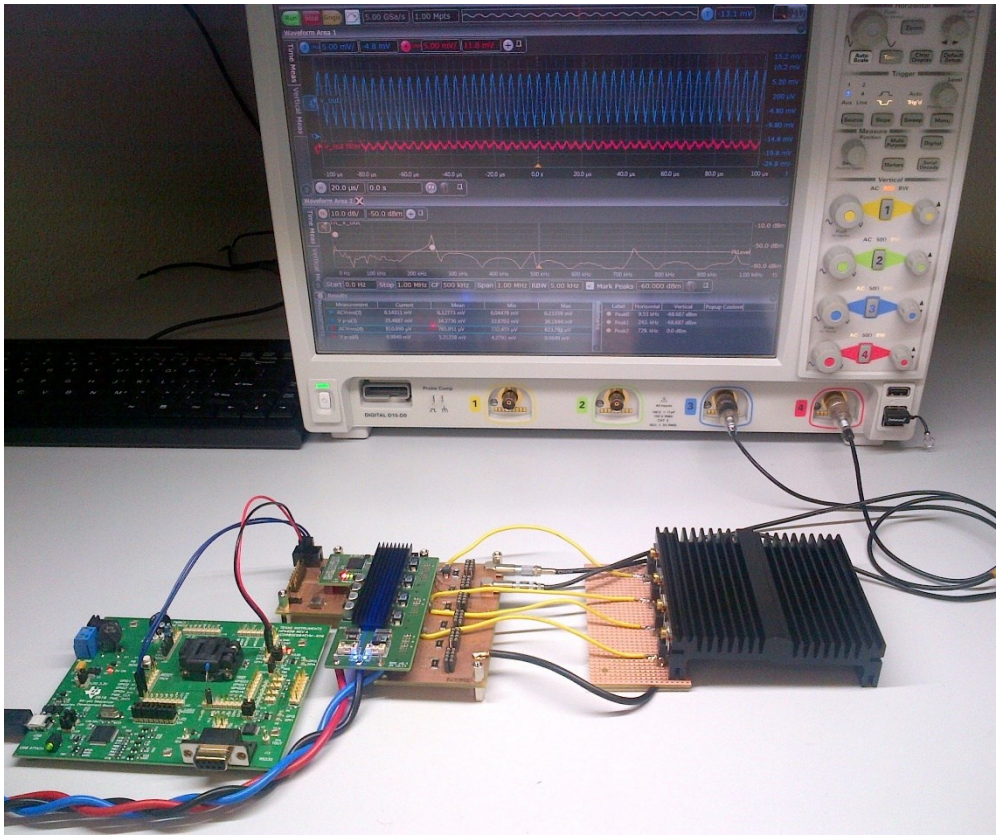
Low noise switching power supply

→ SADC power consumption
~ 30 Watts
→ 1.0V_D FPGA core voltage (10A)
→ 2.2/3.0V_A ADC voltage (3A)
→ …

→ Input voltage: 6V/12V NIM
→ crucial: residual ripple/noise of analog voltages (impact on σ_E / σ_t)

Power supply tested with 4x5A load
→ 50% of designed load
→ 200% of required load
→ below 3mV_{PP} residual ripple



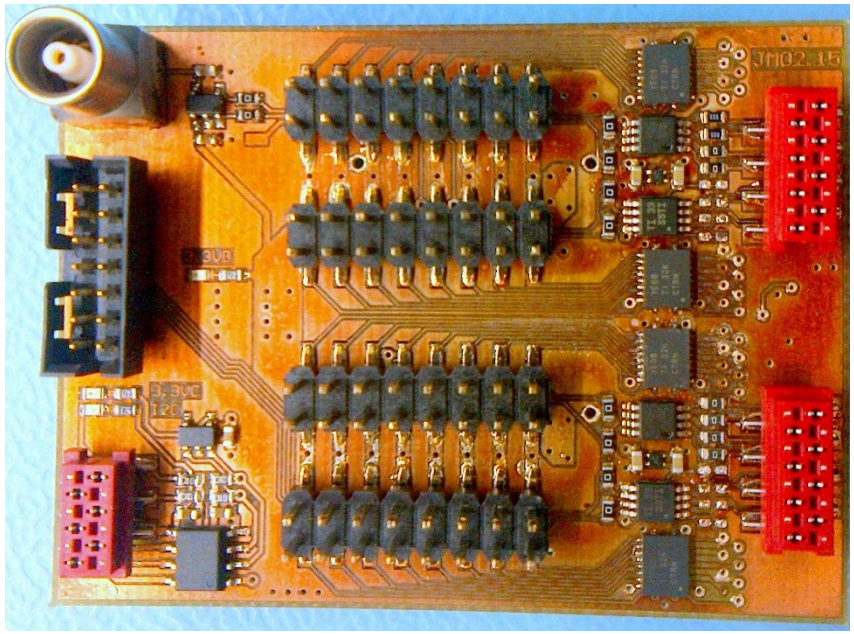


Trigger / Clock / Debug / Slowcontrol

LVTTL clock input
→ all SADCs will be phase-locked for best time reconstruction

Debugging ports for accelerated development

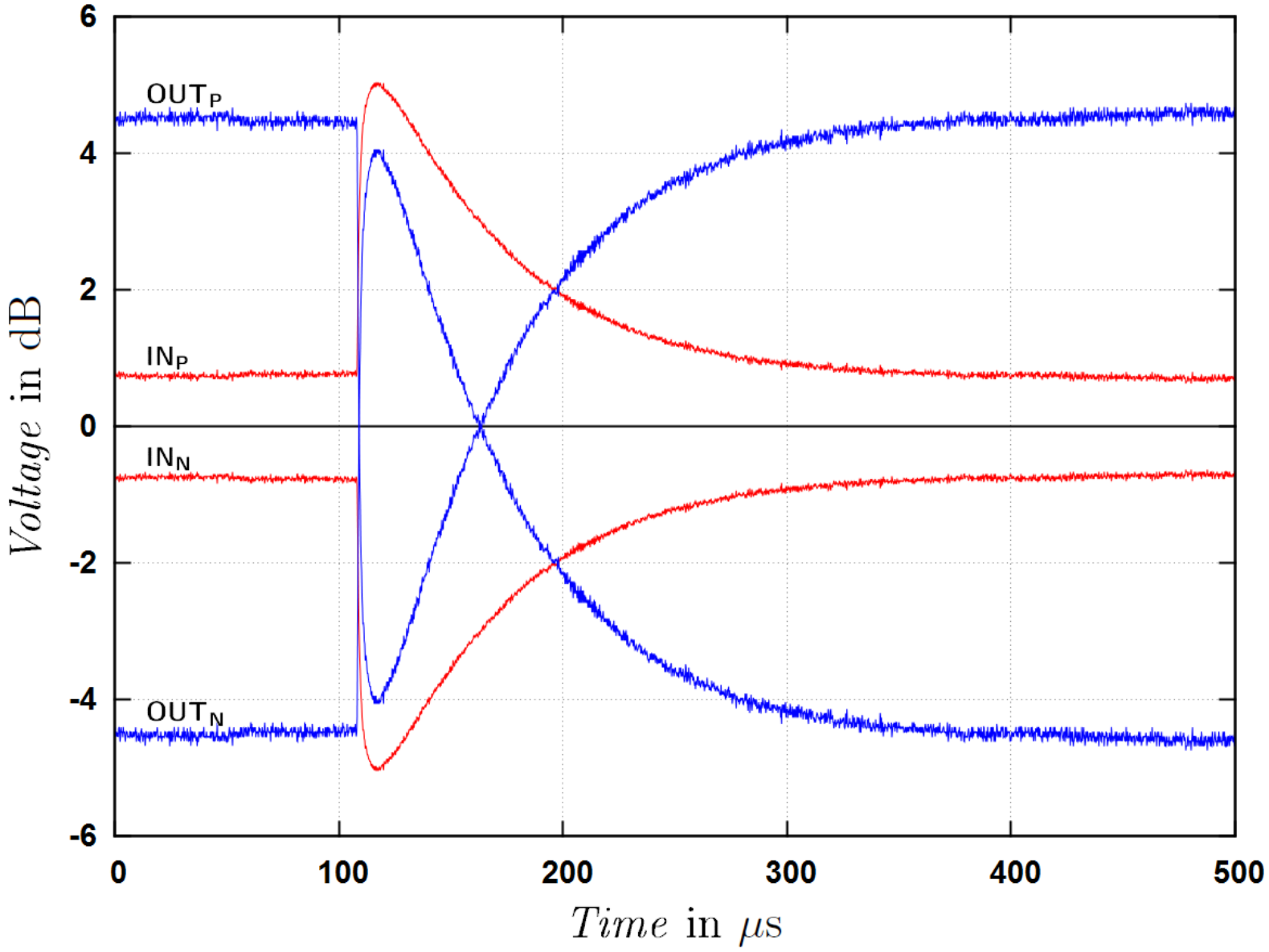
JTAG for FPGA configuration



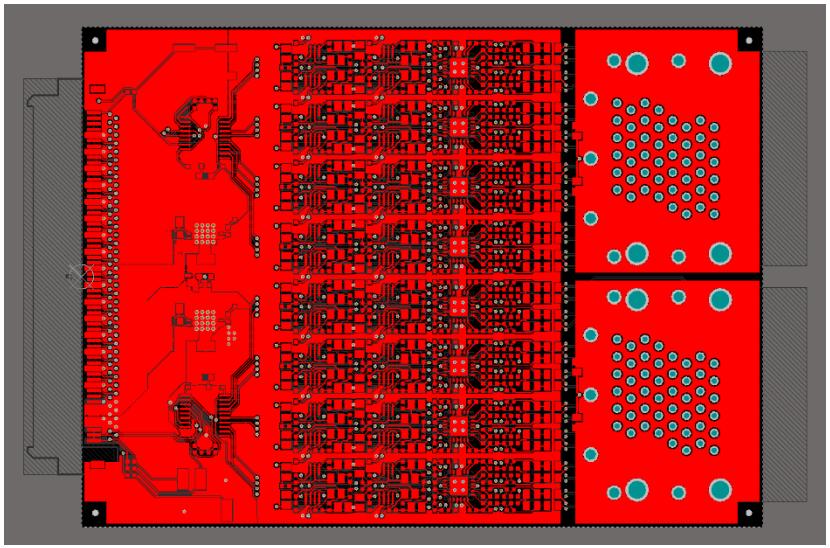
Slowcontrol (I^2C) connection (control & monitoring interface)

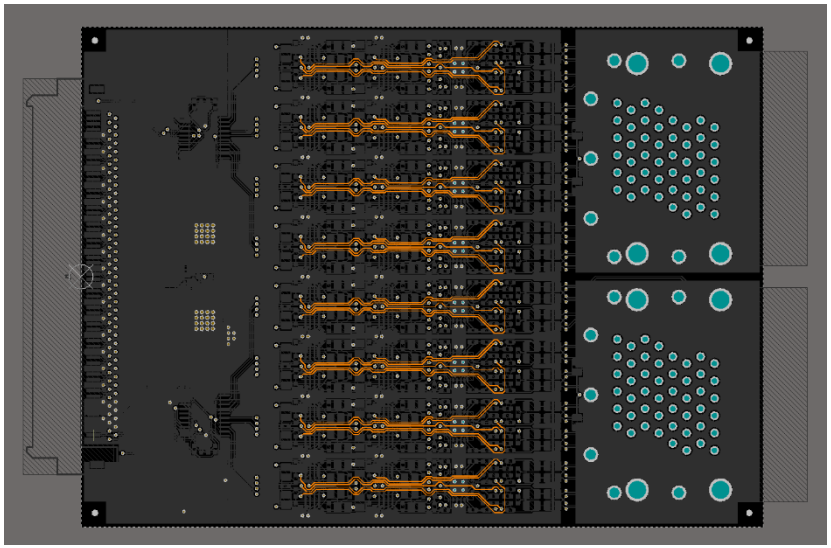
LVPECL I/O for DAQ sync system (Trigger)

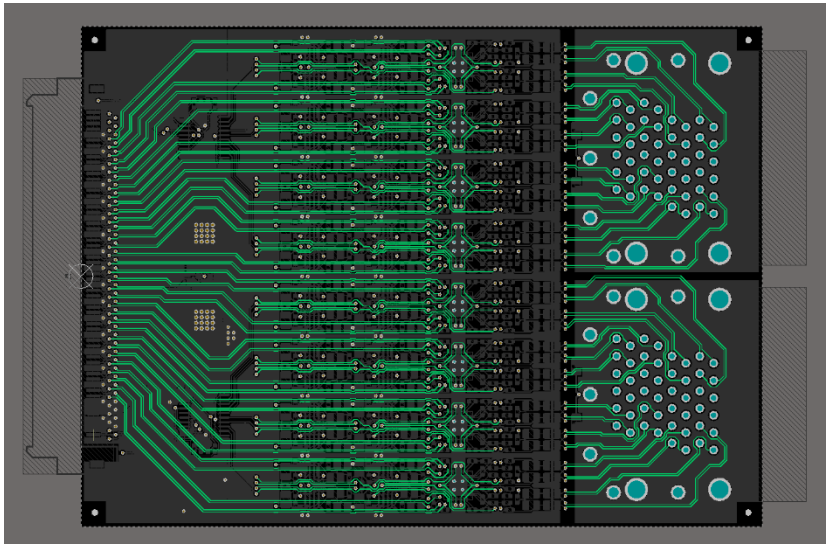
Baseline Shifter

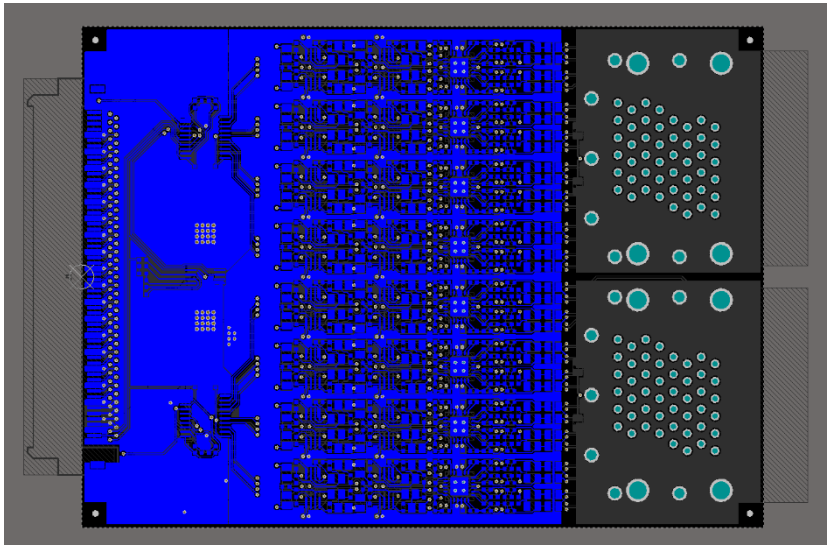


Baseline Shifter

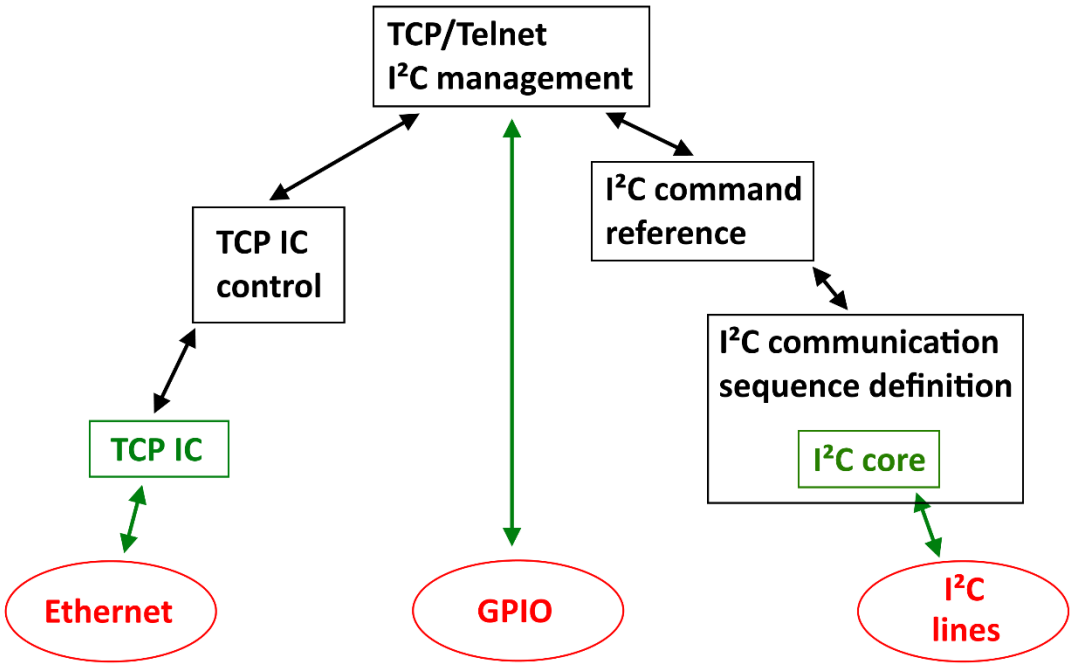




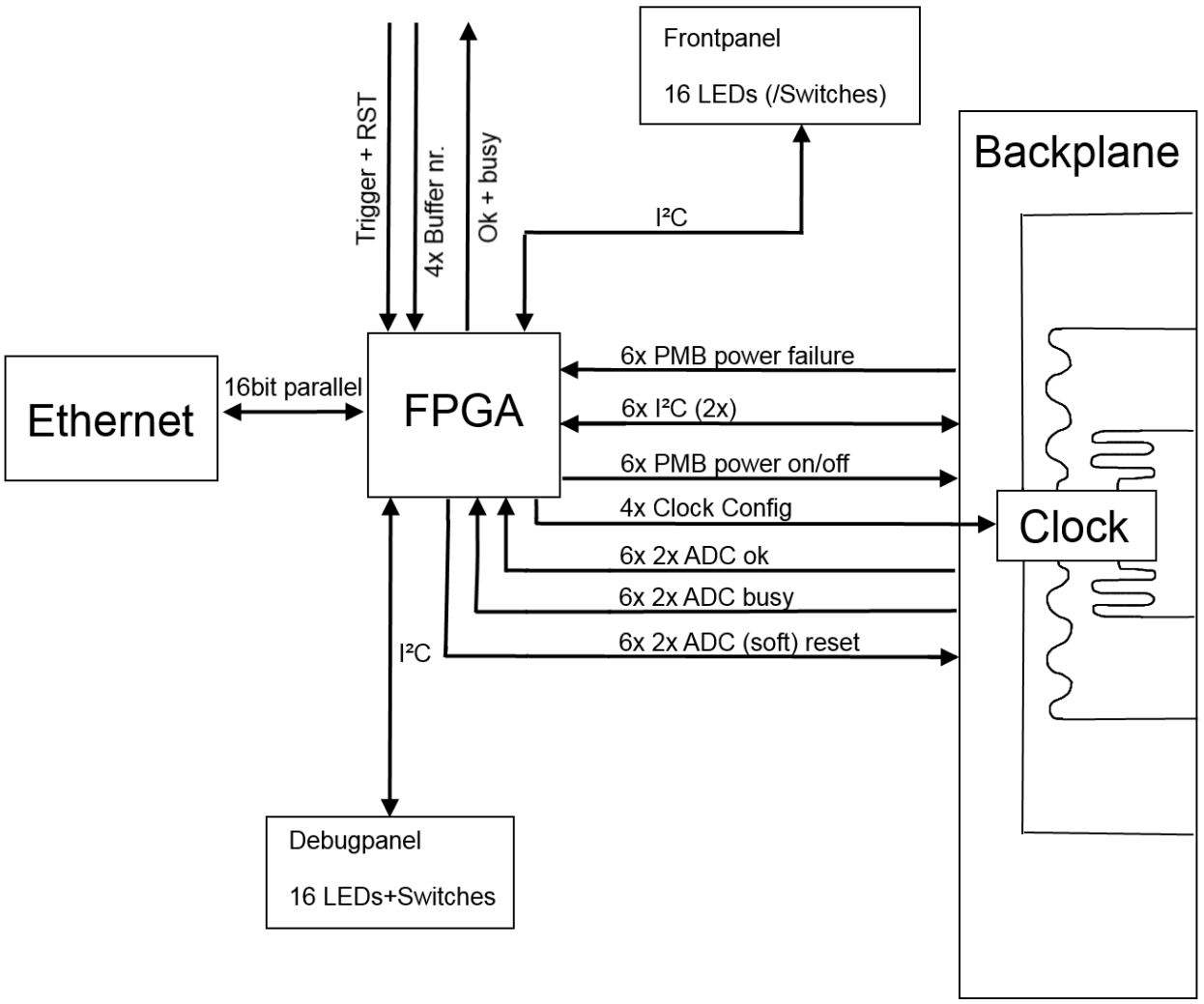




Slowcontrol VHDL

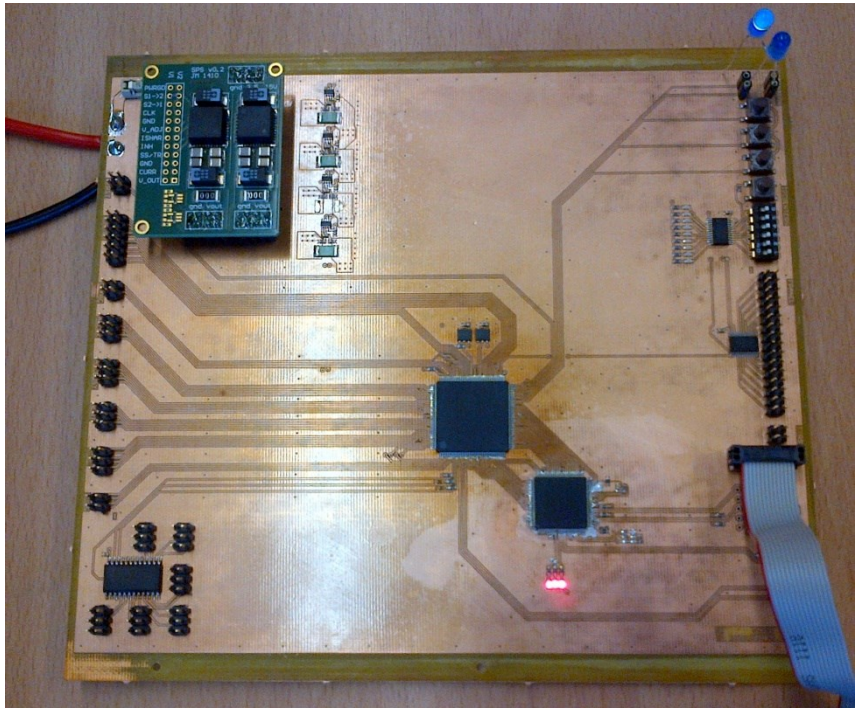


Slowcontrol



Slowcontrol

→ **Master student Georg Urff**



Purpose:

→ **Programming of FPGAs**

→ **Clock (phase) distribution**

→ **Slowcontrol of SADC**
- **monitoring of U, I, T**
- **voltage adjustment**
- **baseline adjustment**