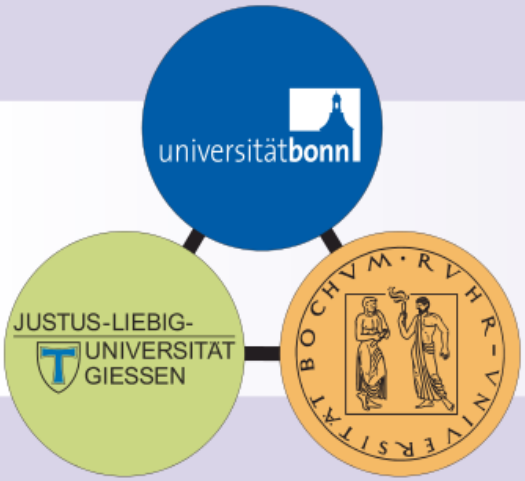
universitätbonn

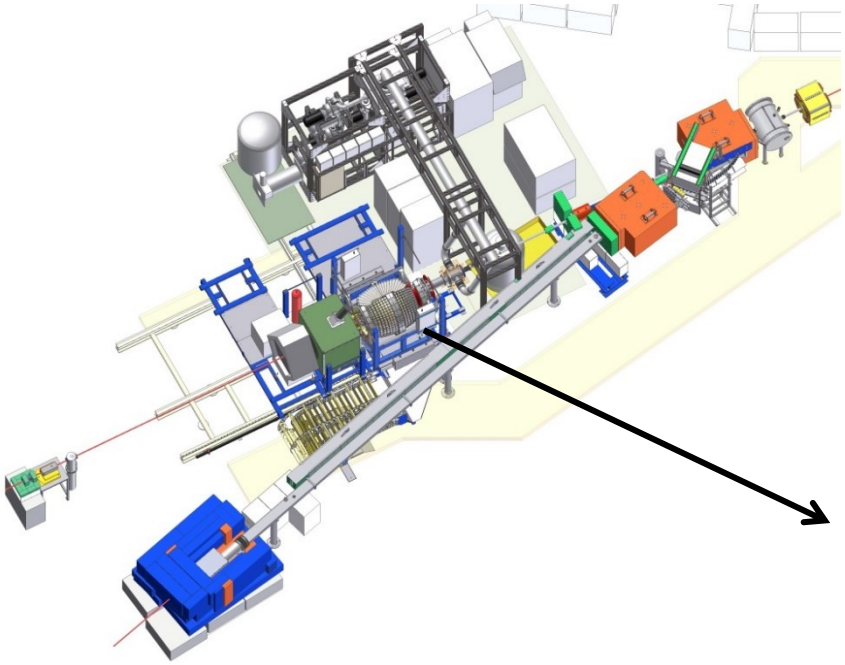
FPGA based Sampling ADC for Crystal Barrel

Johannes Müllers
for the CBELSA/TAPS collaboration



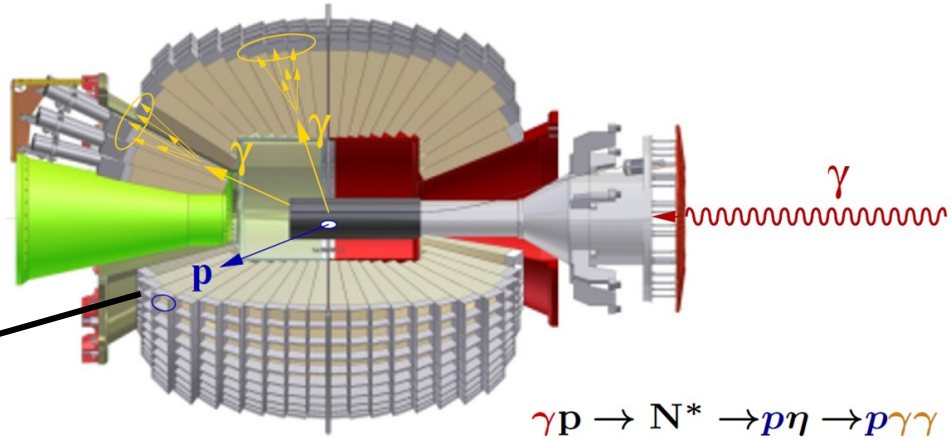
Rheinische Friedrich-Wilhelms-Universität Bonn

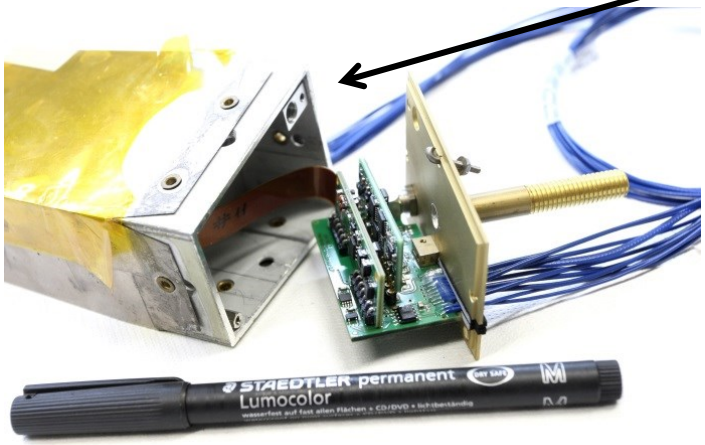
CBELSA/TAPS Experiment (Bonn)



- Investigation of the baryon excitation spectrum in meson photoproduction
- 3.2 GeV e- on Bremsstrahlung radiator
- (Un-)polarized target

→ Measurement of double pol.observables





- CBELSA/TAPS is being upgraded to achieve trigger and timing capability for the electromagnetic Calorimeter
- PIN Diode → APD
- QDC → SADC

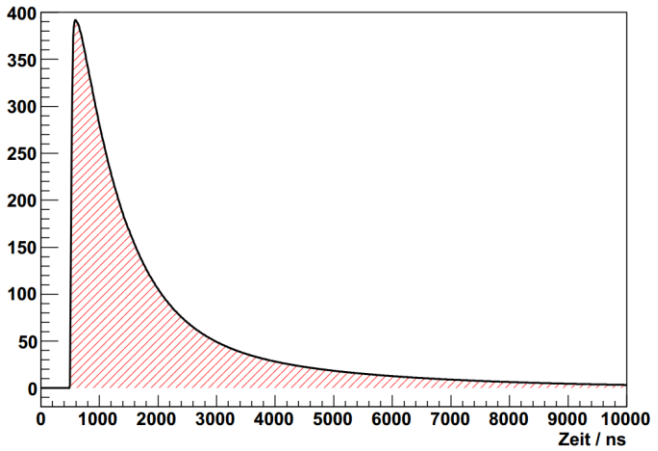
Talk CB: HK 62.1

Poster CB Upgrade: HK 22.4

Advantages of SADC over QDC

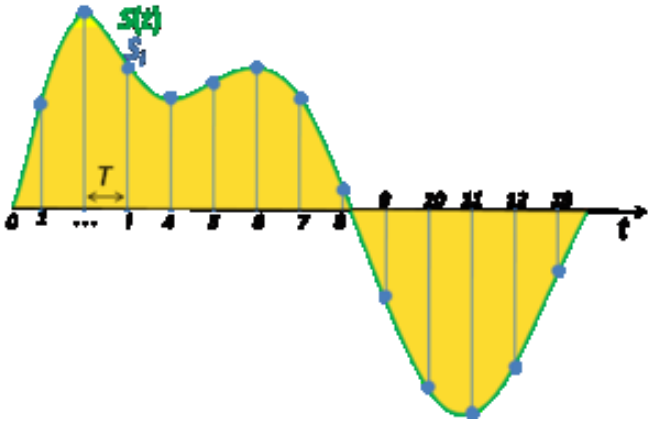
QDC

- Charge to digital converter
- Integral → proportional to E
- 6 µs window, fixed to trigger
- Fixed pedestal per run
- No pile-up handling
- Readout rate limitation ~2 kHz



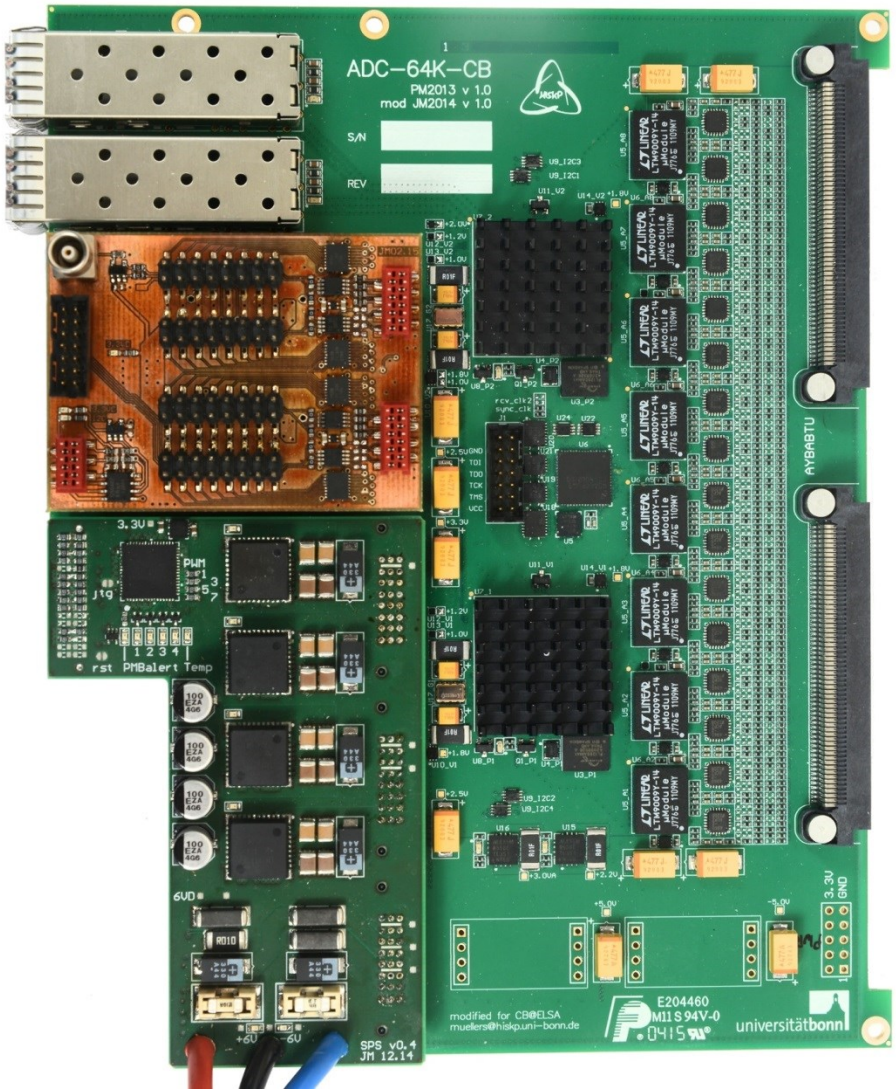
SADC

- Sampling Analog-to-Digital-Converter
- Access to DSP through FPGA
- Integral / Maximum / Rise Time / …
- Event-based pedestal subtraction
- Pile-up recovery



SADC Prototype

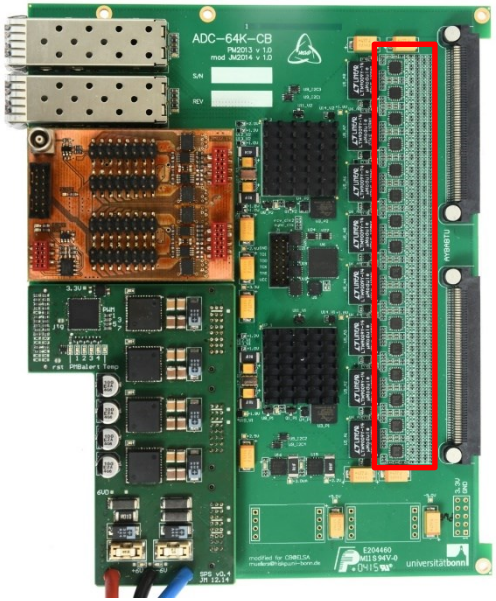
- **Adapted from prototype for PANDA (Design: Pawel Marciniewski)**
- **Optimized for low power, low cost, high channel density**
- **Changes for our project:**
  - **NIM form factor**
  - **Custom power supply**
  - **Custom interfaces**

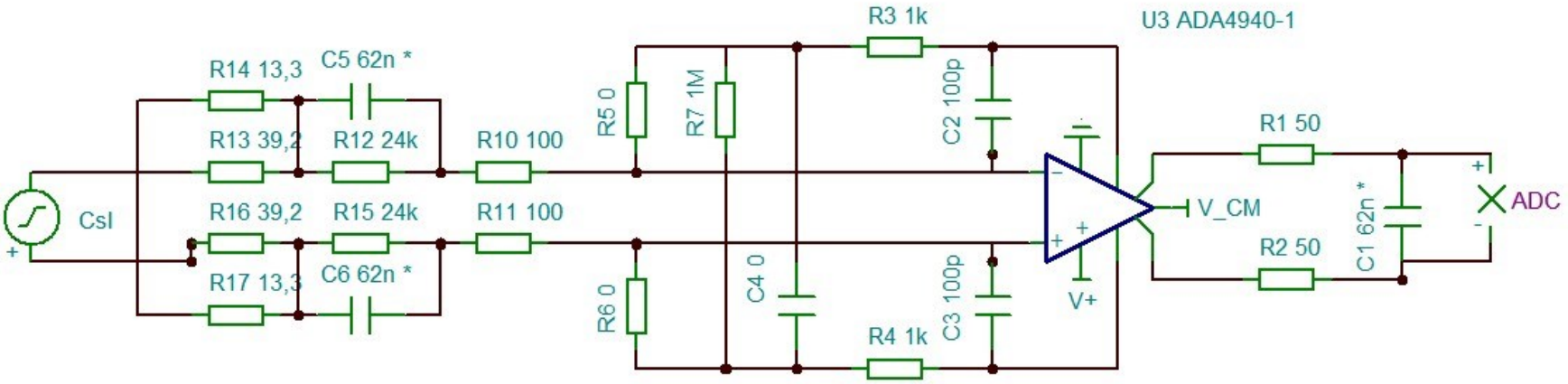


SADC Prototype

Analog stage

- 64 differential inputs
- OpAmp: Analog Devices ADA4940-2
- Signal attenuation
- AC-coupling with pole zero compensation
- 2-pole active lowpass
- Anti-aliasing filter (high pass)

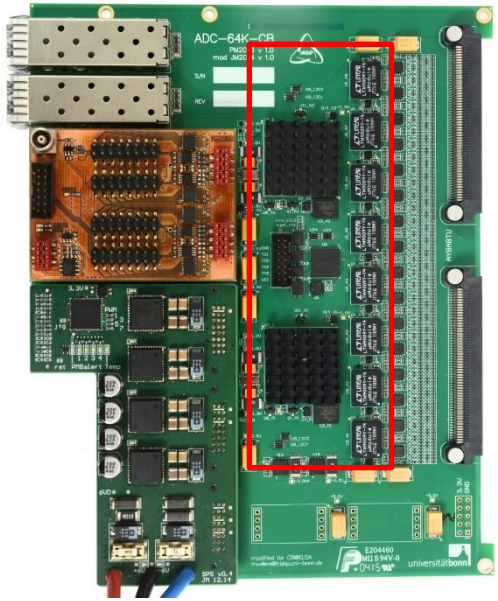




SADC Prototype

Digital stage

- ADC: Linear Technologies LTM9009-14
  14 bit, 80 MHz, 8 channels
- FPGA: 2x Xilinx Kintex 7
- Clock: Texas Instruments LMK04806
  (Clock distribution + phase lock)



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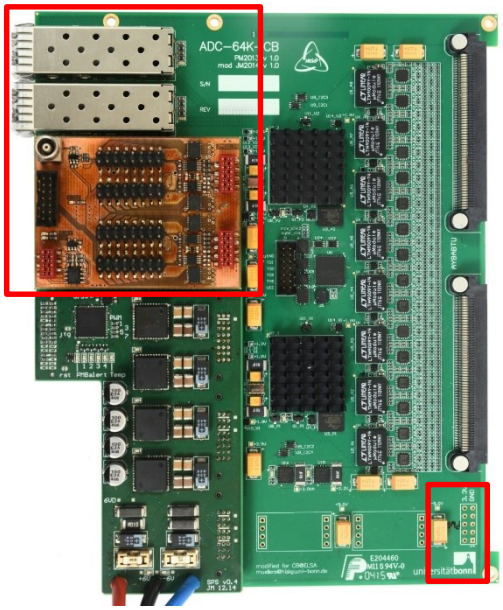
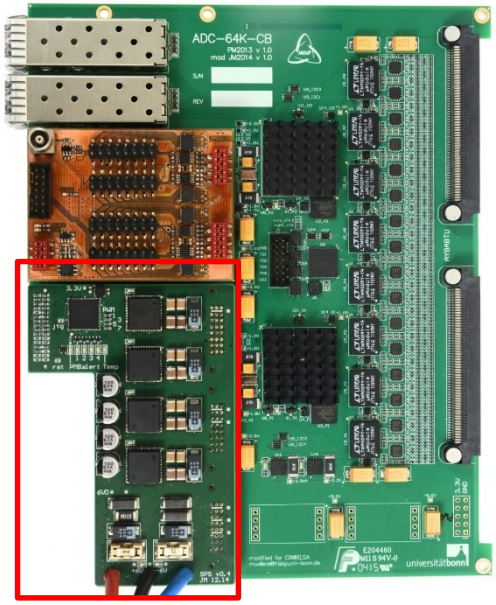
Interconnect stage

- 2x SFP
- JTAG
- I²C
- Trigger, Reset, …



SADC Prototype



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Interconnect stage

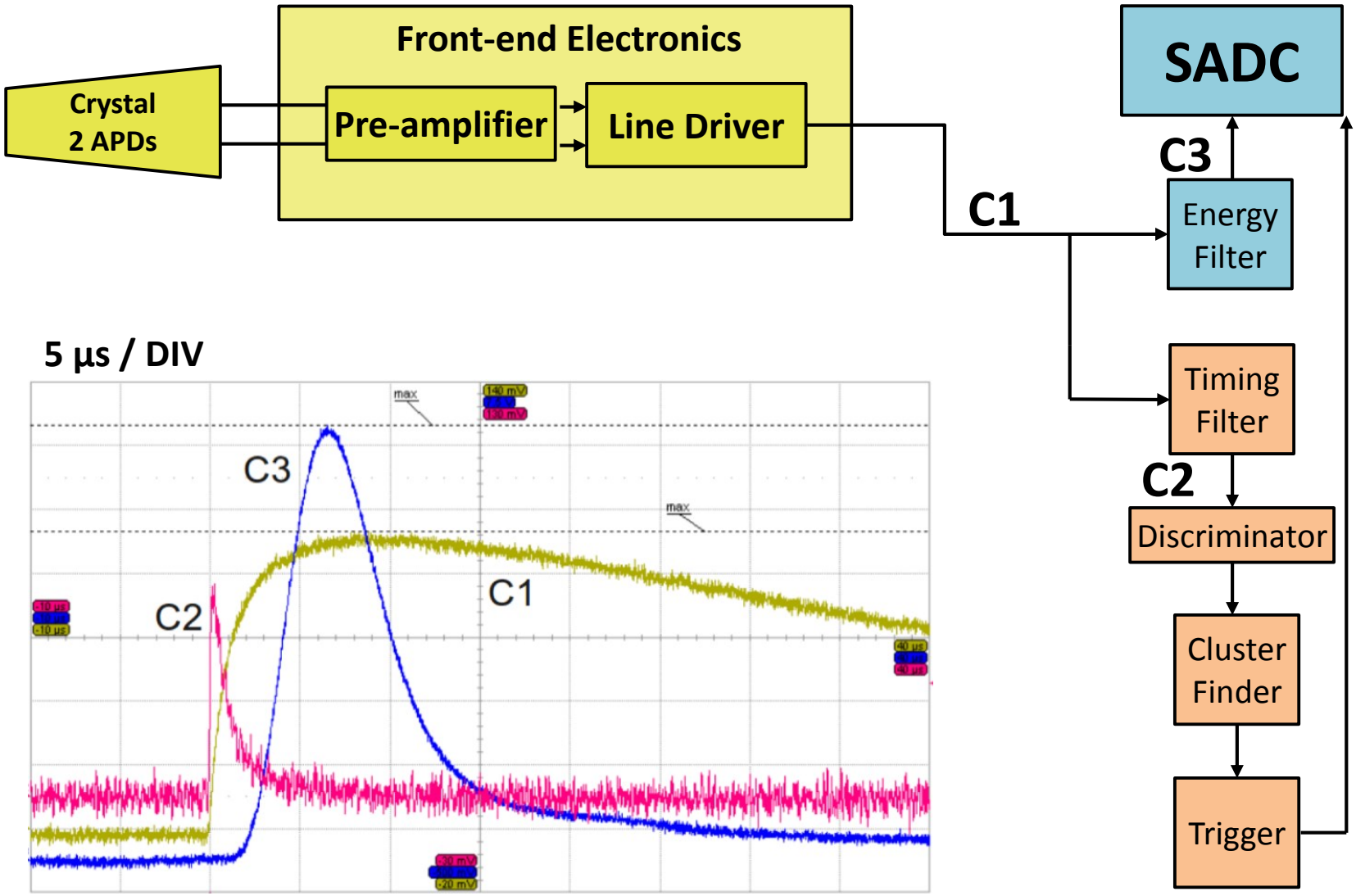
- 2x SFP
- JTAG
- I²C
- Trigger, Reset, …

Power supply

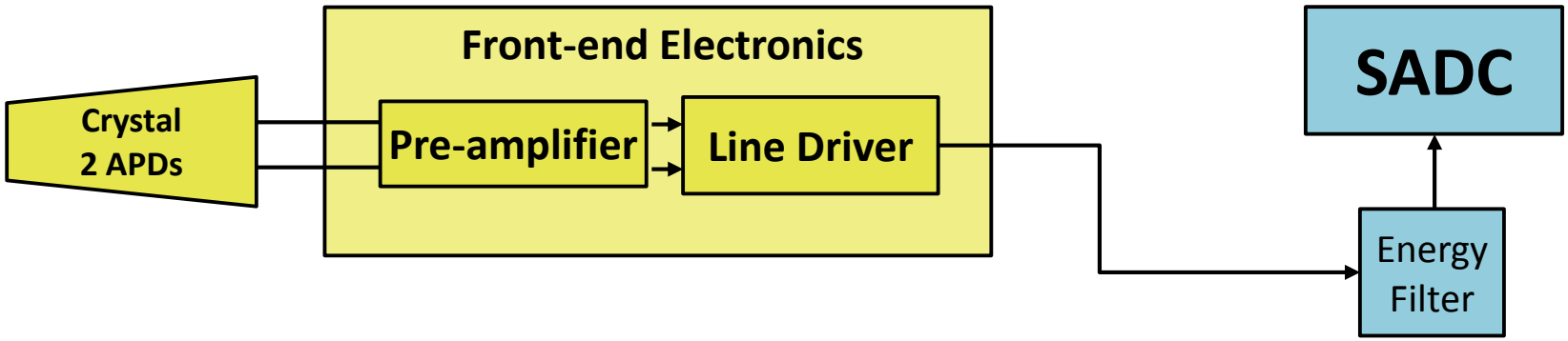
- Input 6 V (NIM supply)
- 4x TI LMZ31710
  10 A @ 1.0 / 2.5 / 2.5 / 3.3 V
- TI UCD90160 16 channel monitor/sequencer

→ Power consumption ~25 W

Signal Transfer

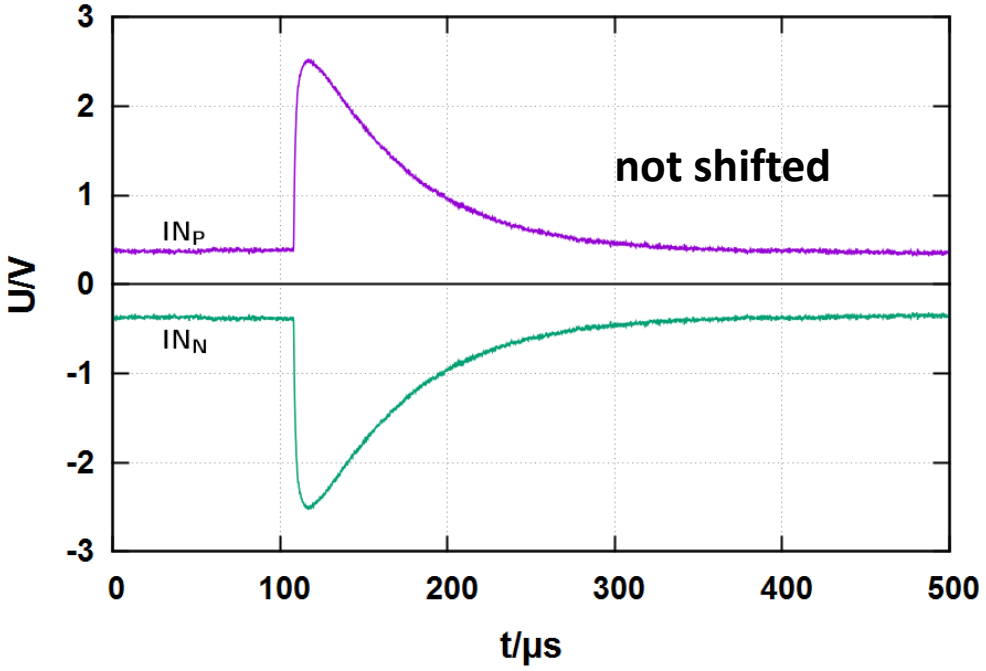


Signal Transfer

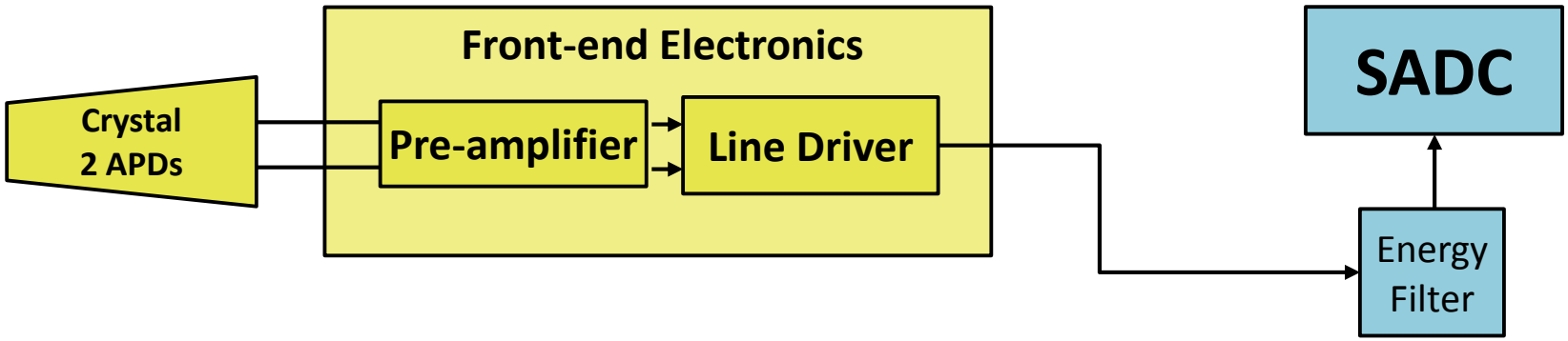


- Differential signal transfer
- <u>Unipolar difference</u>

- Low losses in parallel termination
- Half scale of SADC (13 bit)

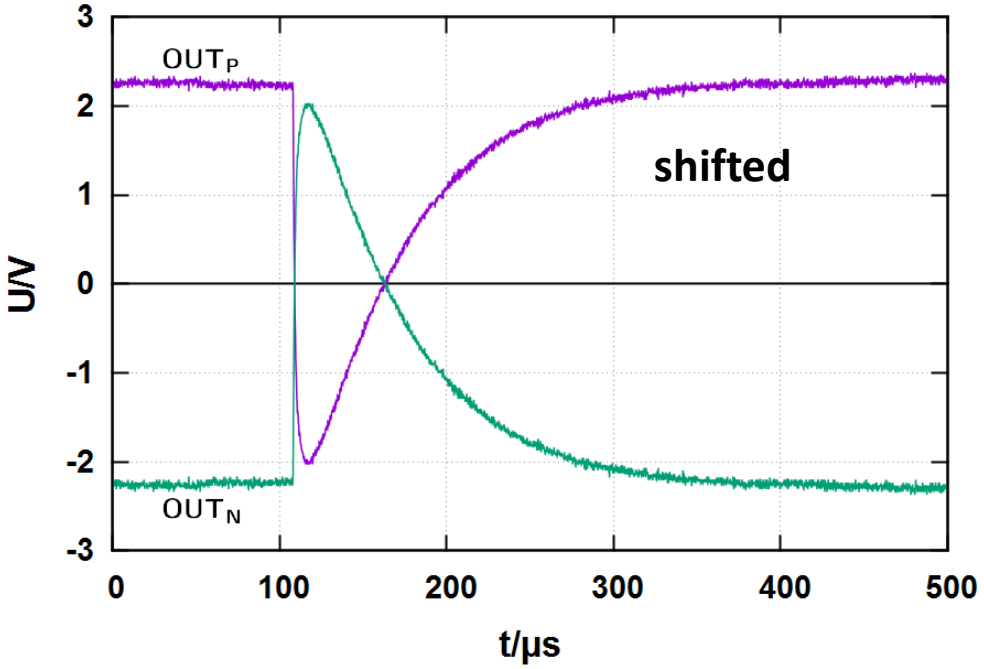


Signal Transfer



- Differential signal transfer
- Bipolar difference

- Use series termination
- Full scale of SADC (14 bit)

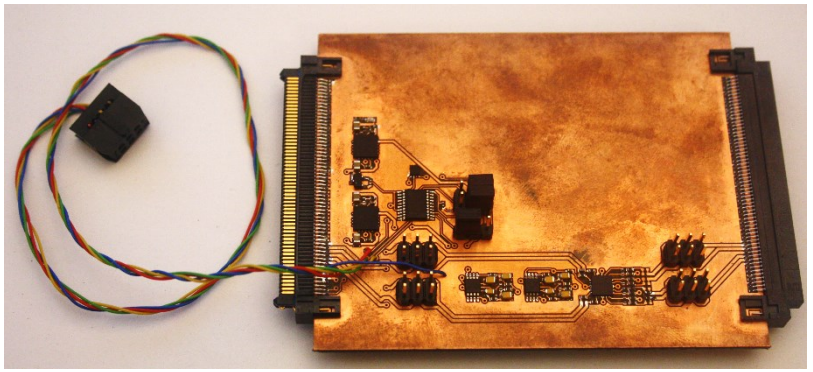


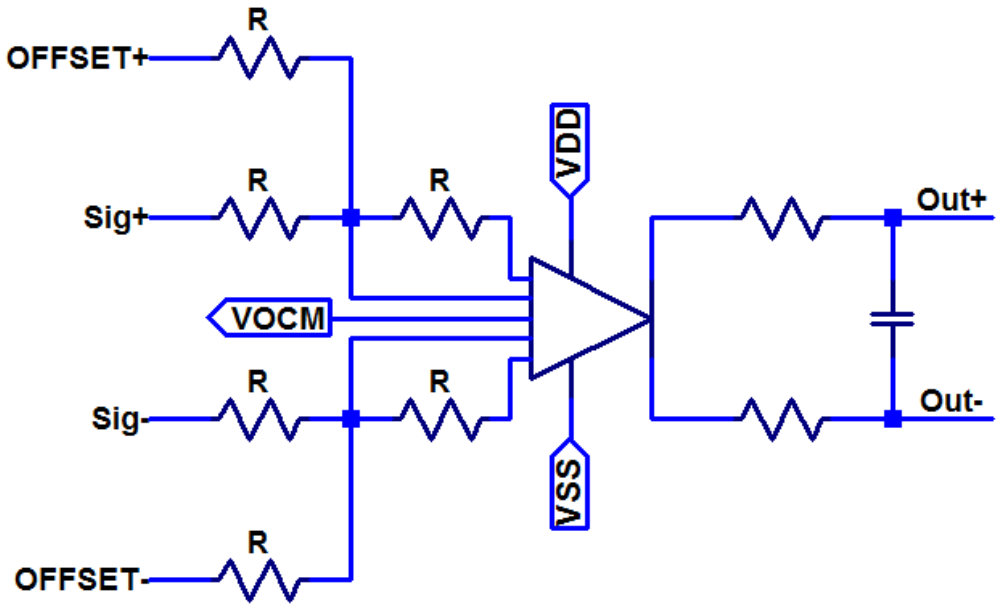
Baseline Shifter

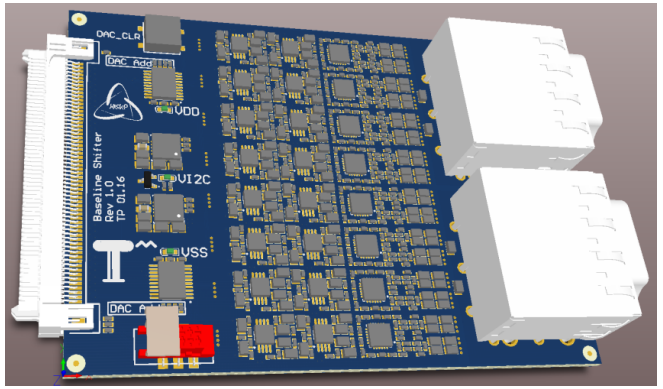
(Timo Poller, Poster HK45.72)

- **Use DAC and differential adder-circuit**
- **Challenge: Noise must be less than ADC quantization noise**

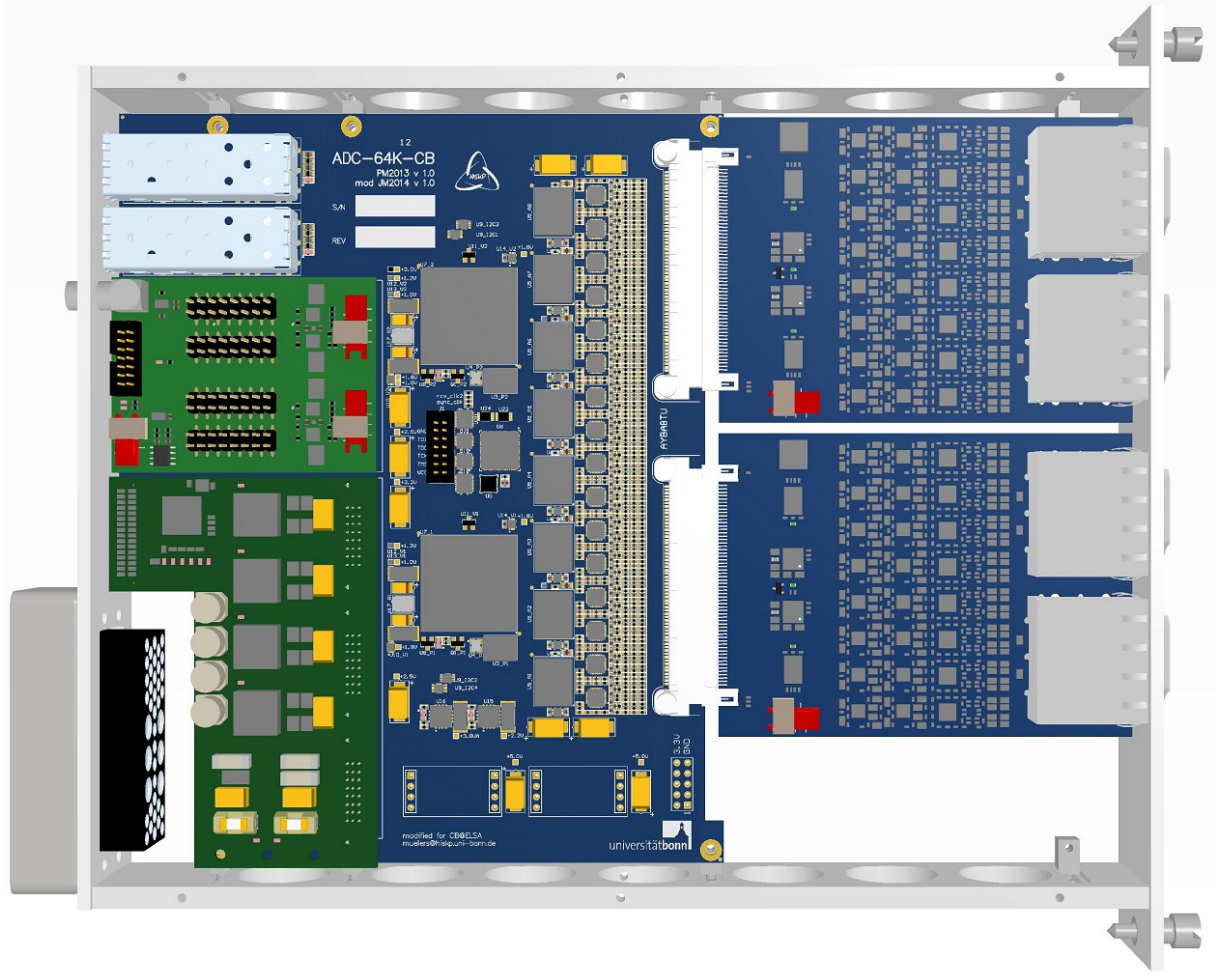
- **Has been achieved**
  42 µV vs. 146 µV



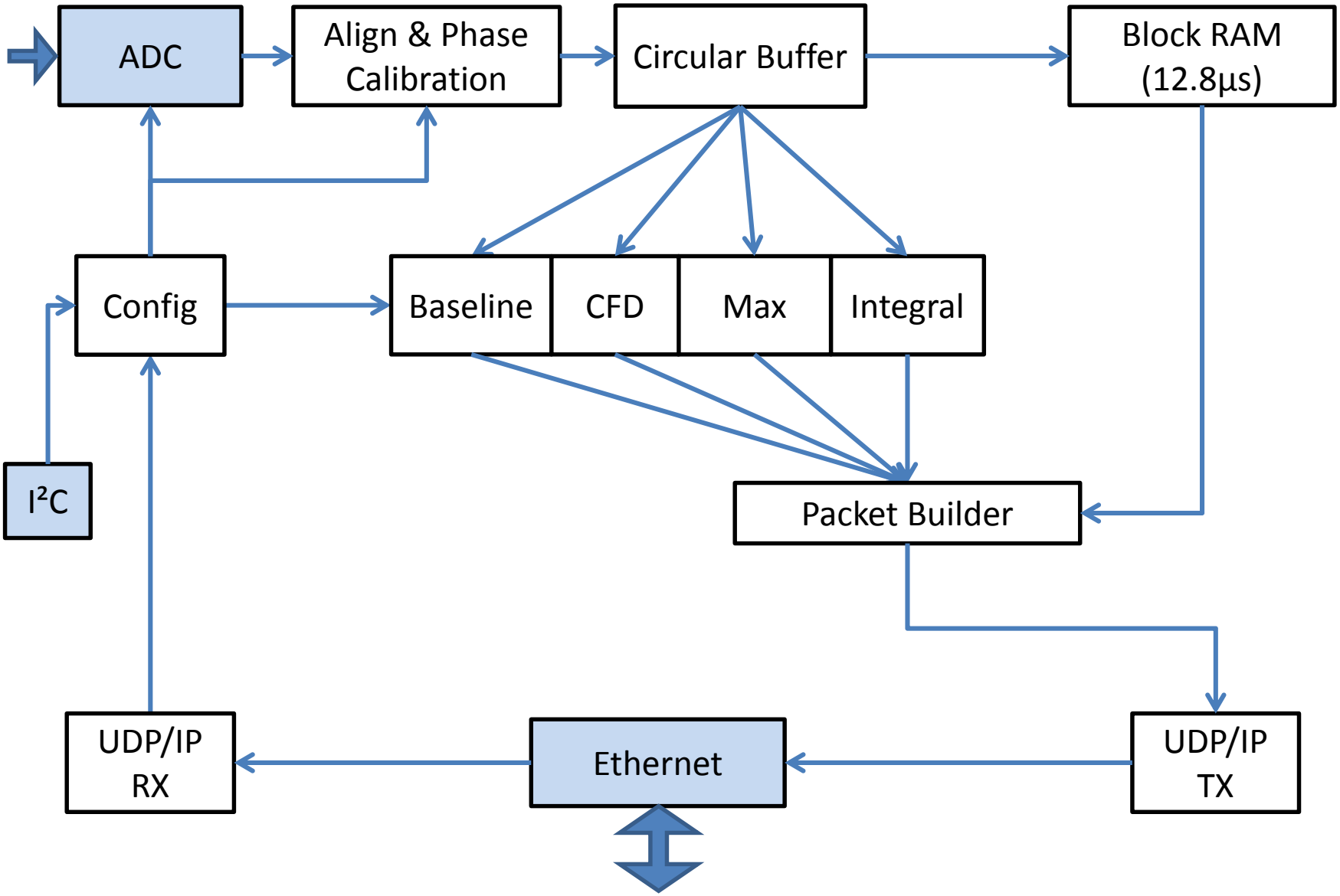




SADC with Baseline Shifter



VHDL (FPGA) Design



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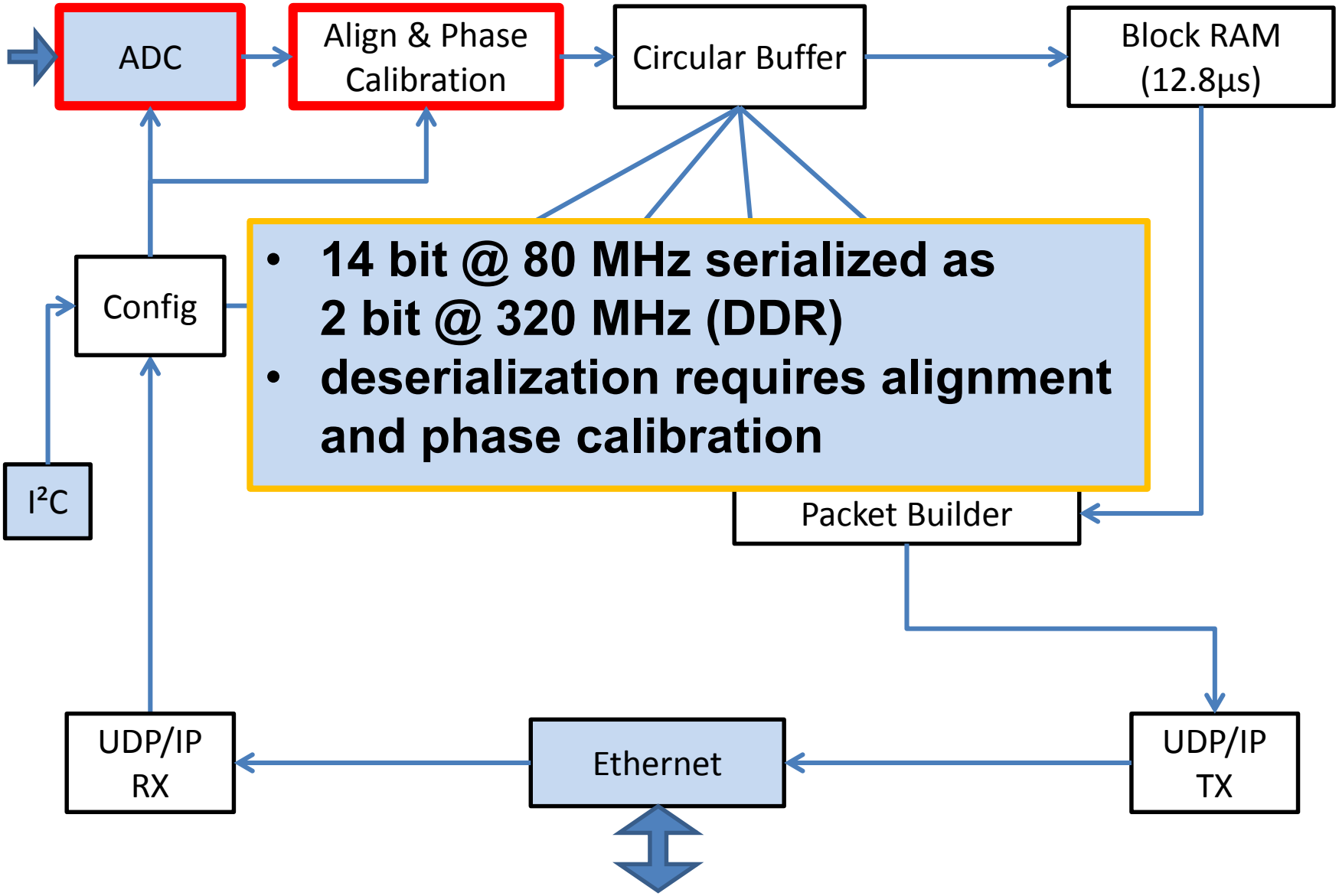
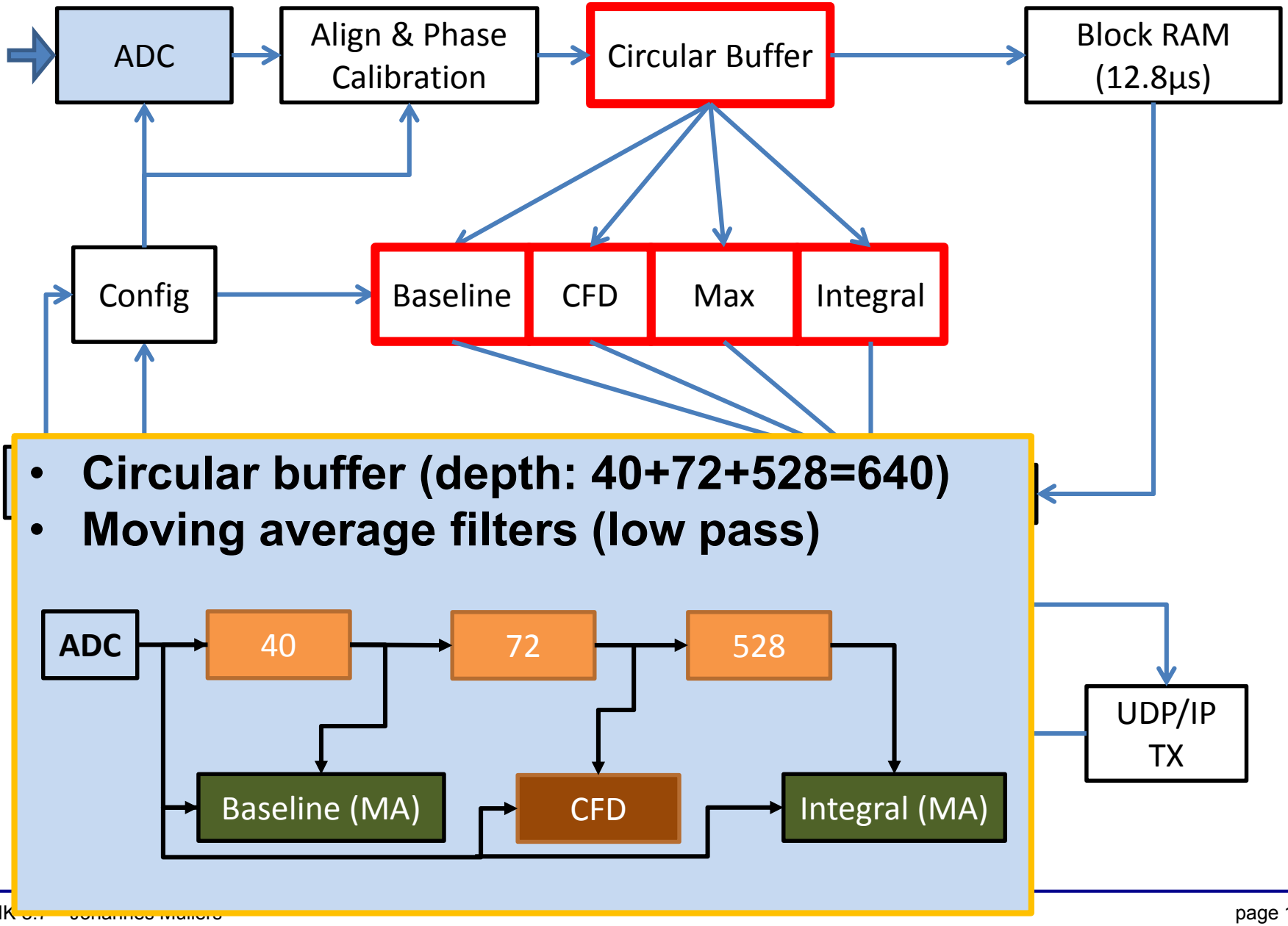
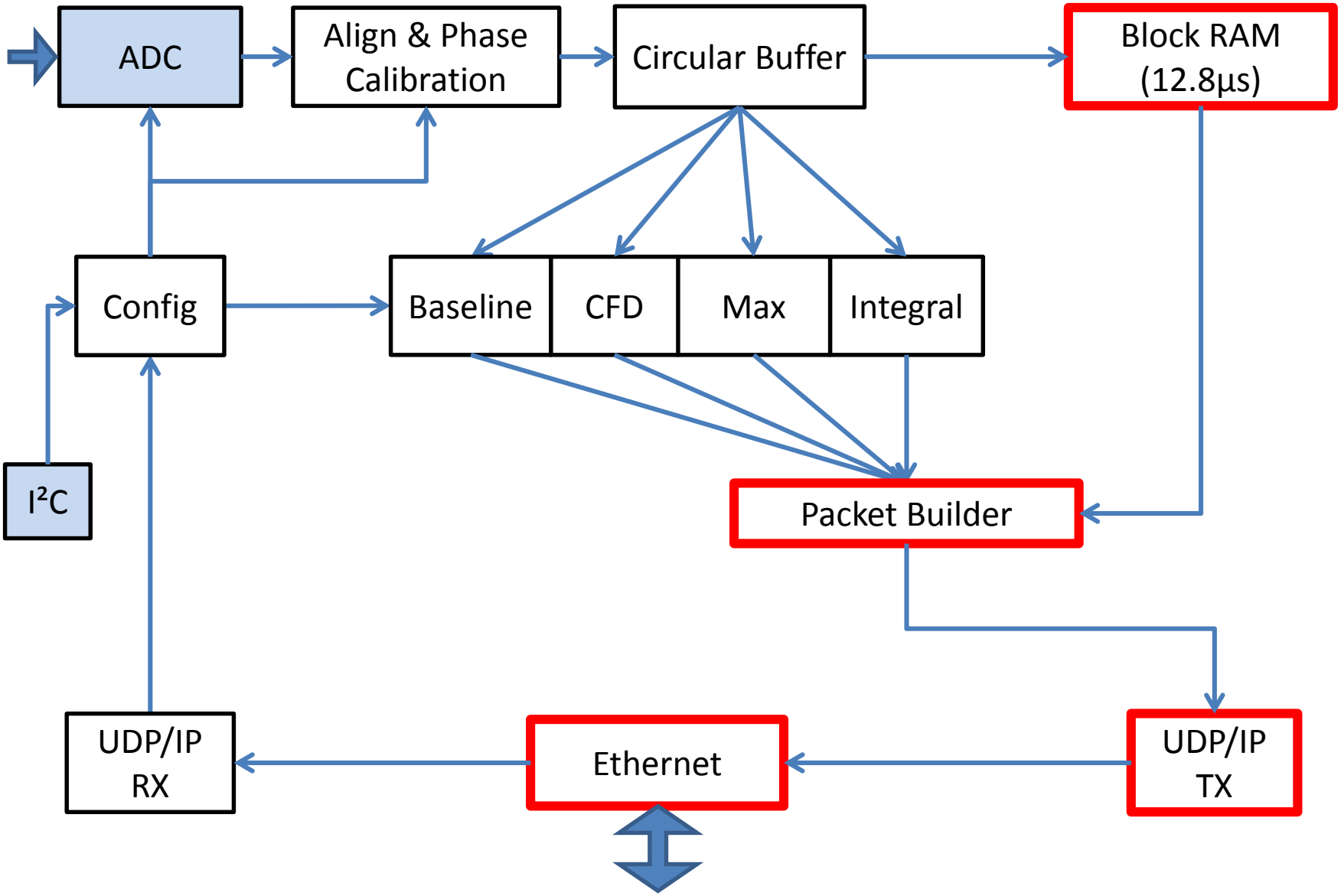


VHDL (FPGA) Design



VHDL (FPGA) Design



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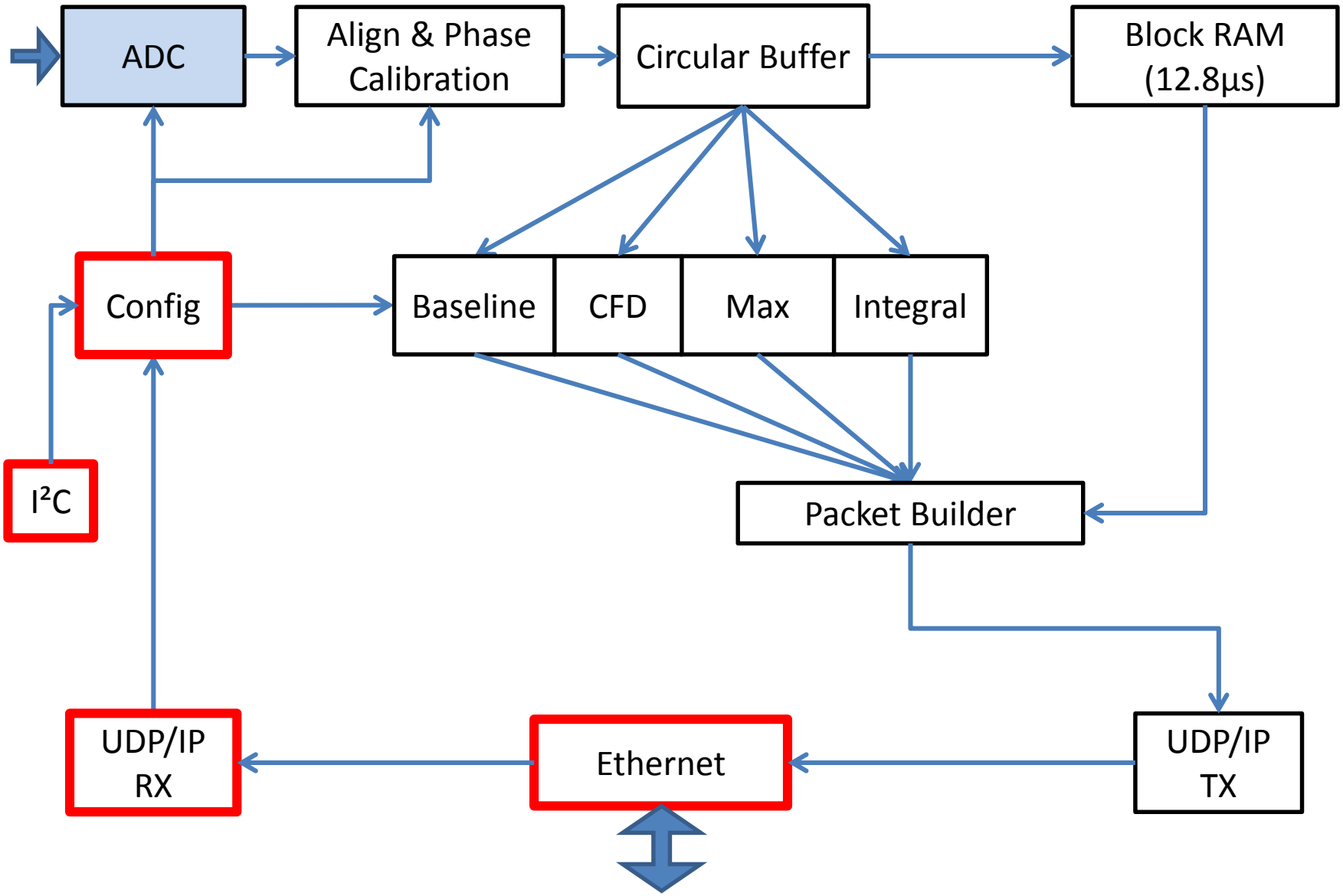
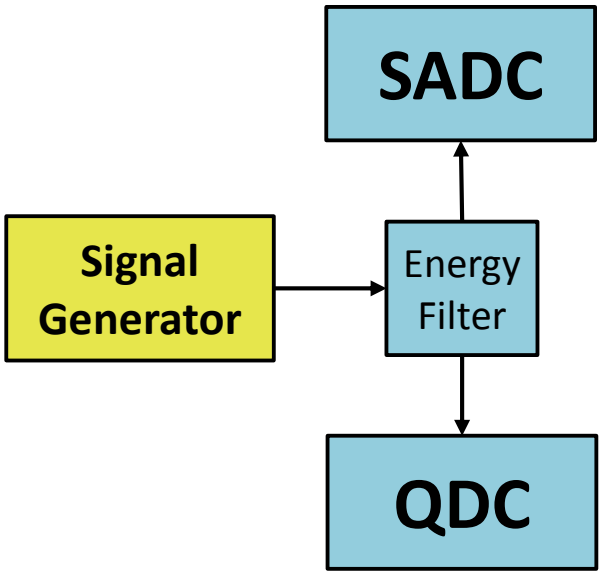


Studies on Energy Resolution

(Jan Schultes, Poster HK45.70)

- **Comparison of QDC and SADC: Measurement of energy resolution (σ_E/E)**



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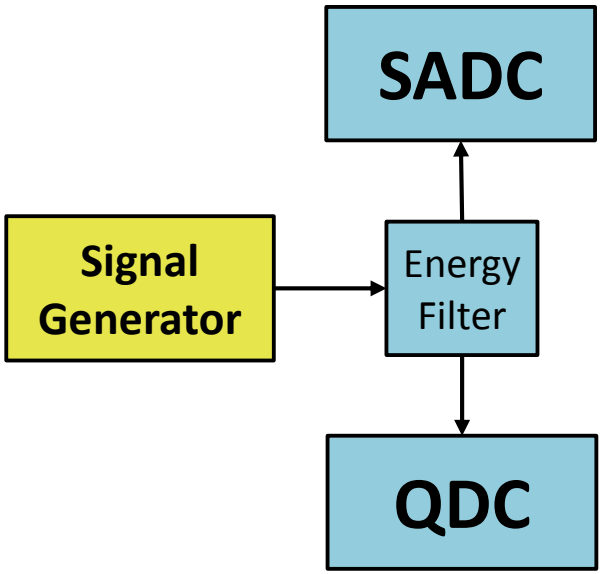
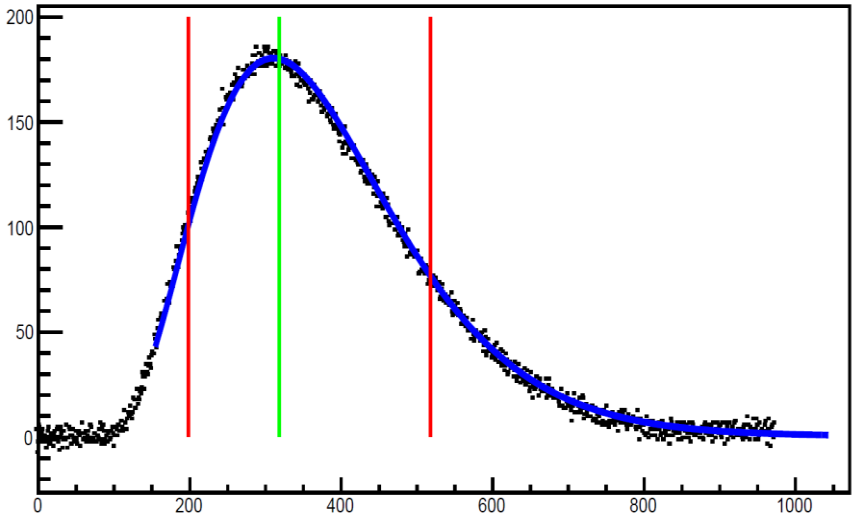


- **Options to obtain deposited energy:**
  - **Integral (SADC, FPGA)**
  - **Integral (SADC, offline)**
  - **Maximum (SADC, offline)**
  - **Integral (QDC)**



Studies on Energy Resolution

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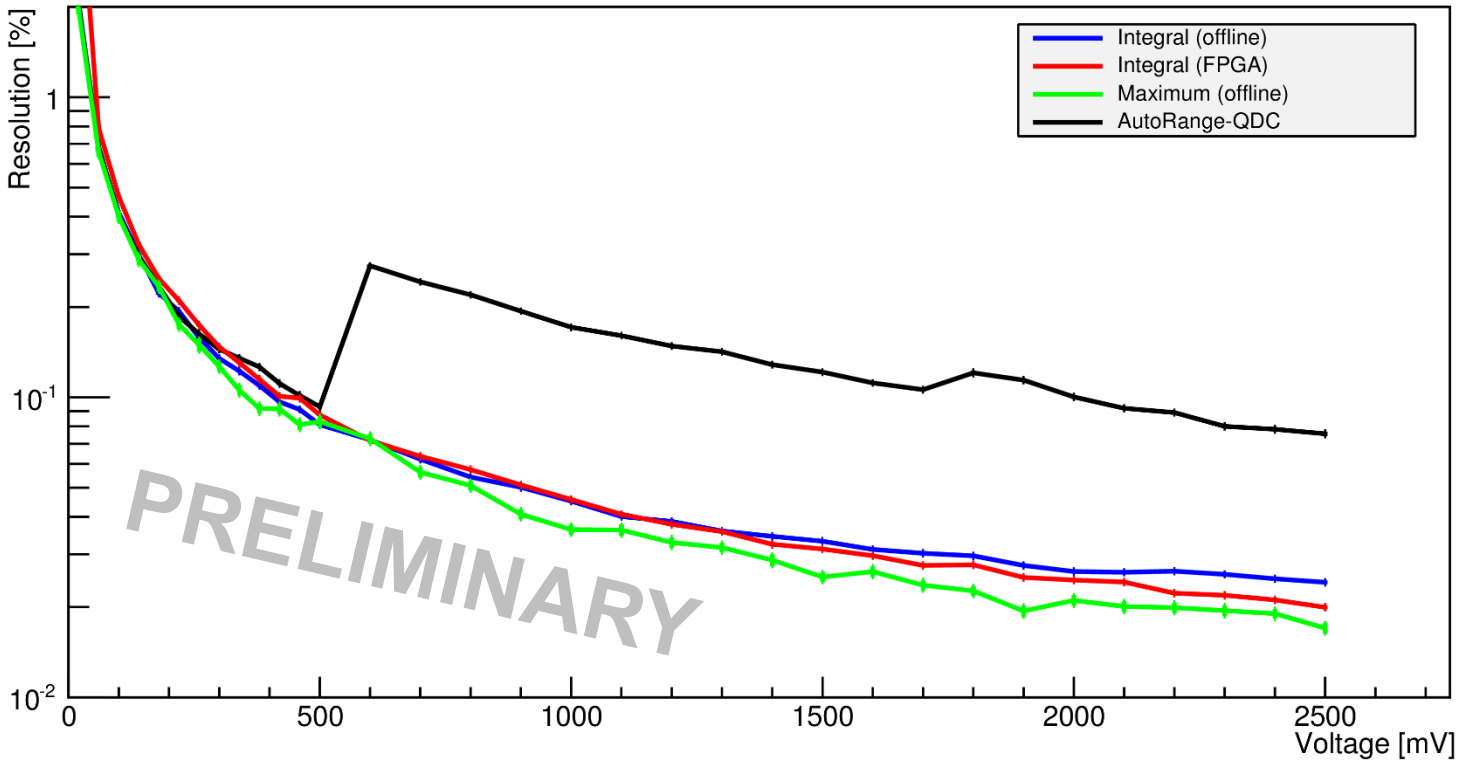
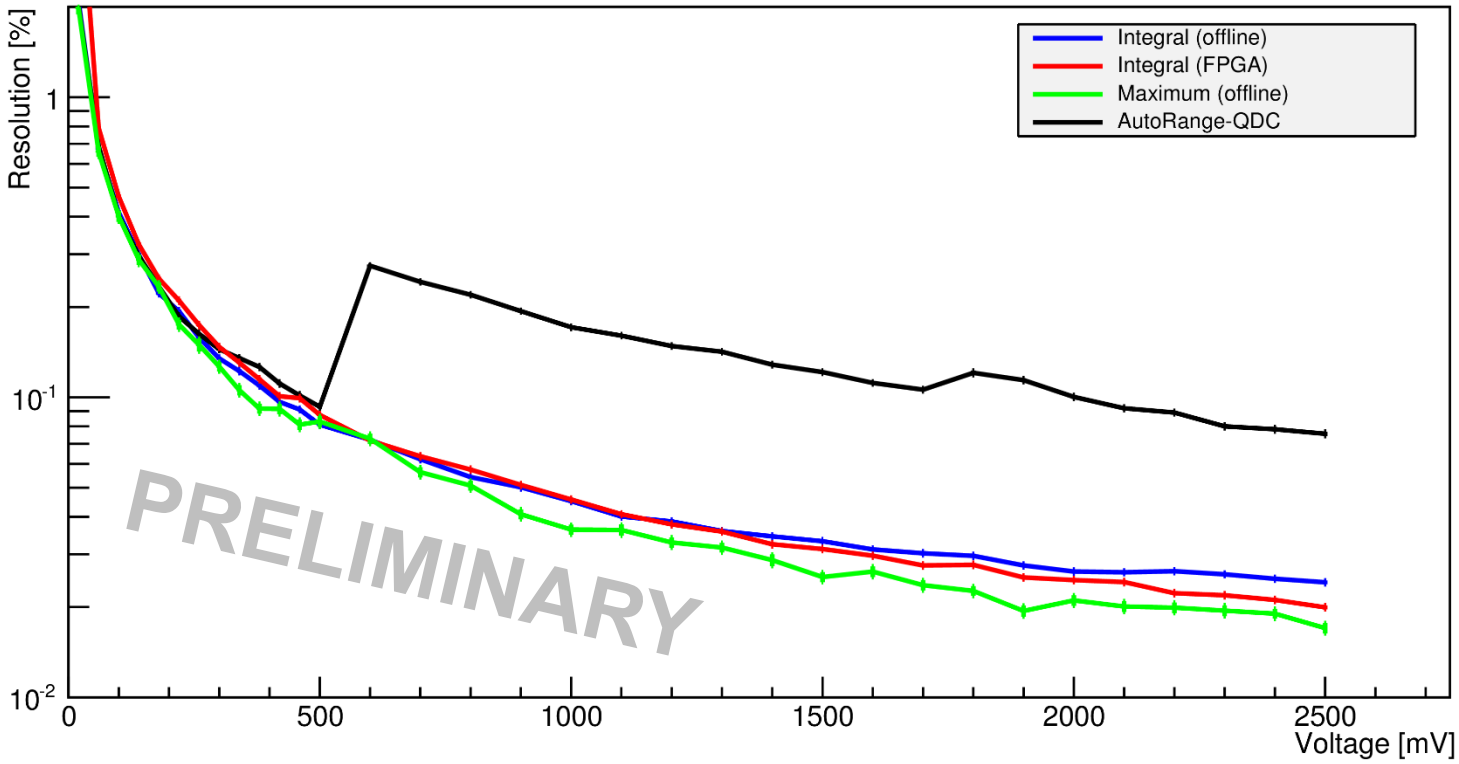


Observations:

- **High range: SADC outperforms QDC**
- **Low range: Most probably resolution is limited by signal noise**
  → Further investigations with less noisy signals

Studies on Energy Resolution

(Jan Schultes, Poster HK45.70)



Tasks:

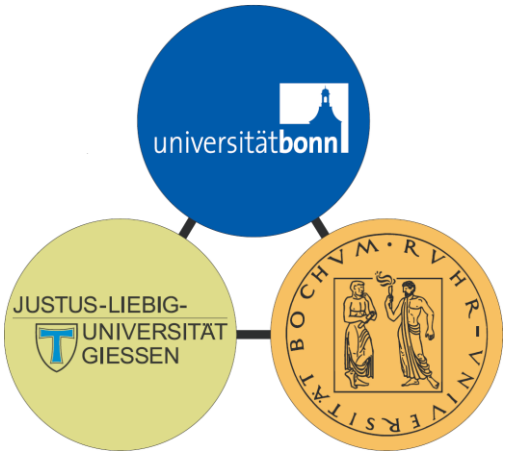
- **Find optimal method to extract energy information in offline analysis**
- **Implement algorithm in FPGA**
- **Challenge: Limited resources (memory, DSP)**

Summary

- **PANDA SADC was adapted for the CB experiment**
- **Investigations for analog & digital filters are ongoing**
- **First studies on the energy resolution are promising**

Funded by the DFG

Contributions to the project:
P. Marciniewski, T. Poller, C. Schmidt, J. Schultes, U. Thoma, G. Urff

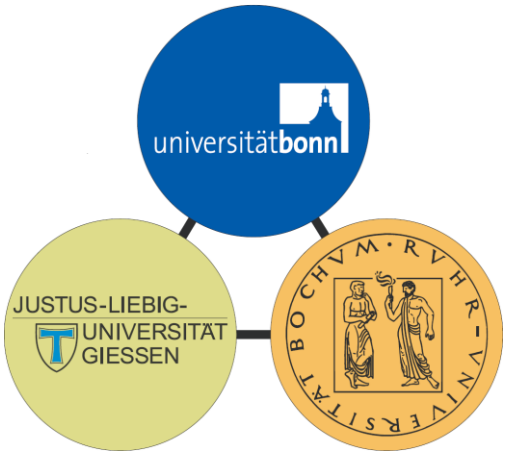


SFB/TR16

Summary

Thank you!

Questions?

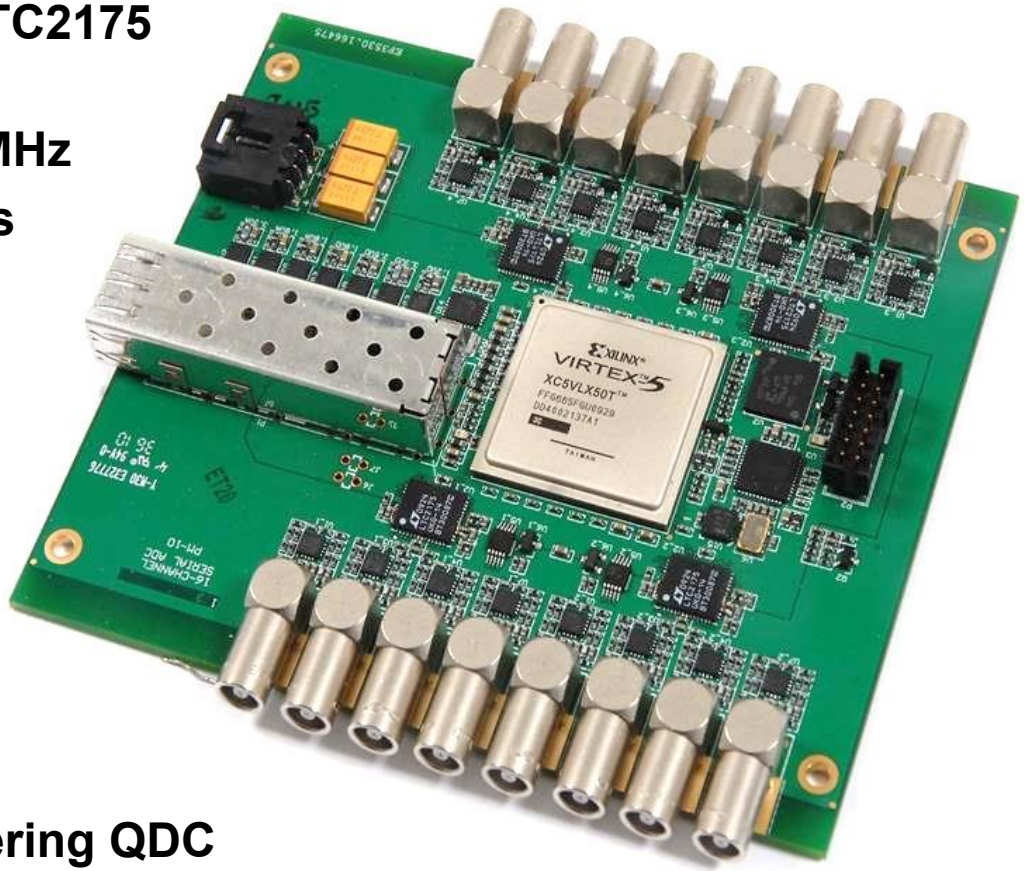


Funded by the DFG

SFB/TR16

First prototype (16 channels)

- Developed as prototype for PANDA (P. Marciniewski)
- ADC: Linear Technologies LTC2175
  14bit, 125MHz, 4 channels
- Xilinx Virtex-5 LX50T @ 125MHz
- 16 single ended LEMO inputs
- SFP Interface



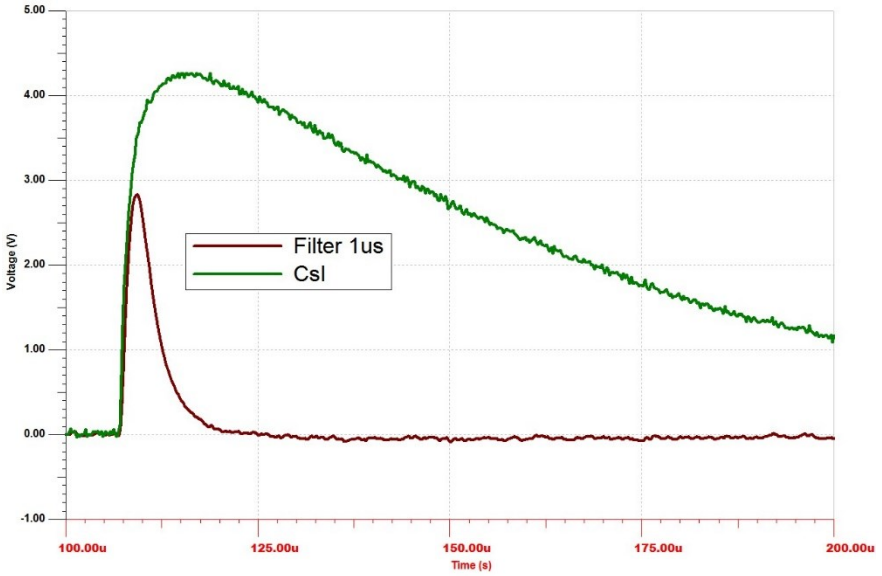
- Overall satisfying results
- Implementation of self-triggering QDC
  with Gigabit Ethernet
- but: needed higher channel density

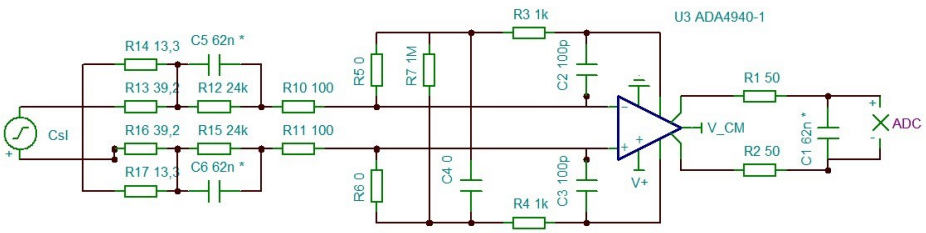
Onboard analog shaping

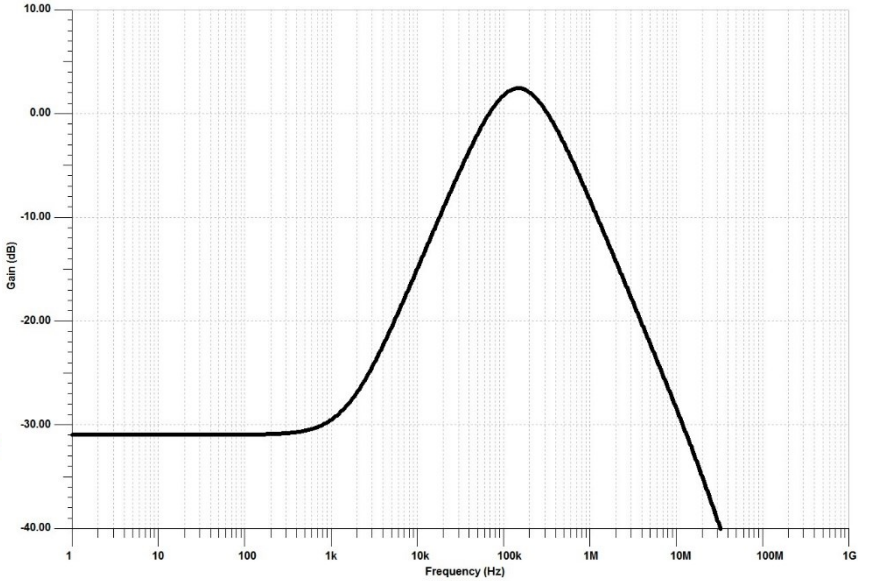
Analog input stage of SADC:
- → **passive highpass (with PZ cancellation)**
- → **quasi-3pole lowpass**

Will be used for
- → **CRRC shaping**
- → **Aliasing-filter for ADC (LP)**

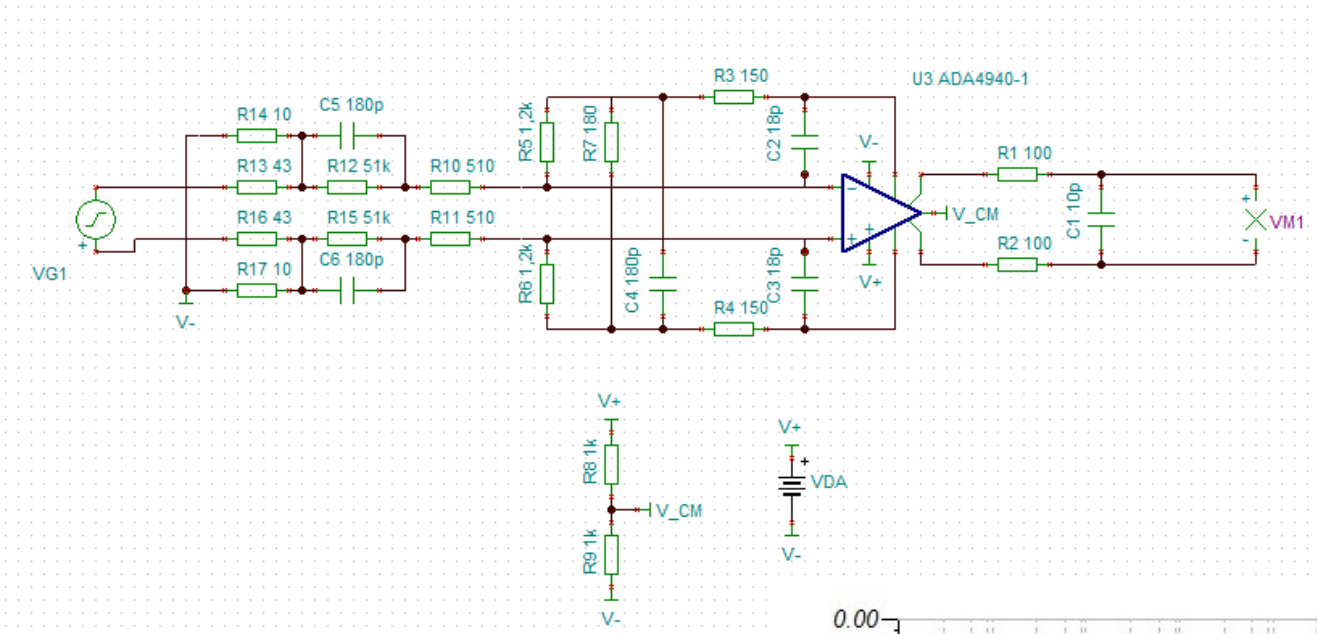
In prototype:
- → **Attenuating input buffer with aliasing filter**
- → **reconfiguration possible**

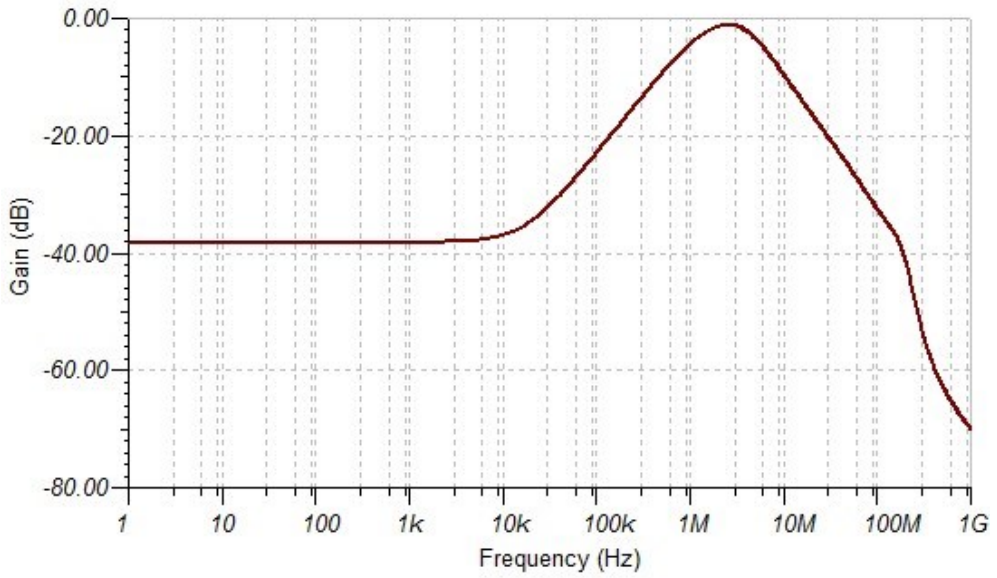






SADC Analog-Filter (PANDA)



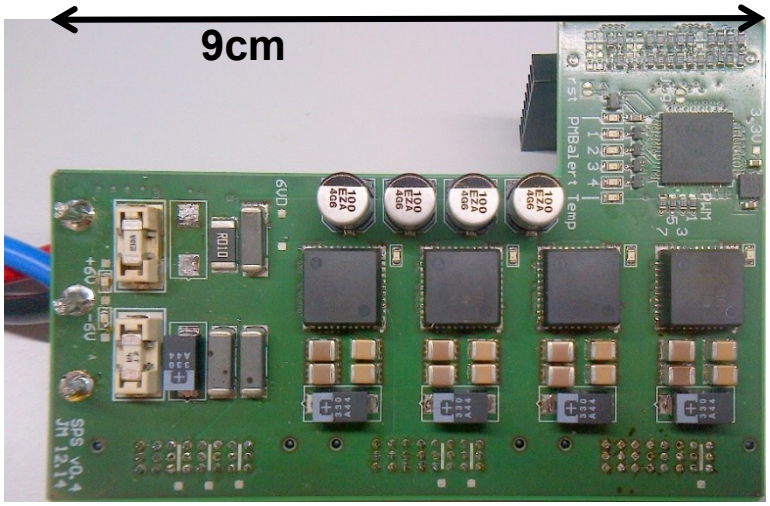


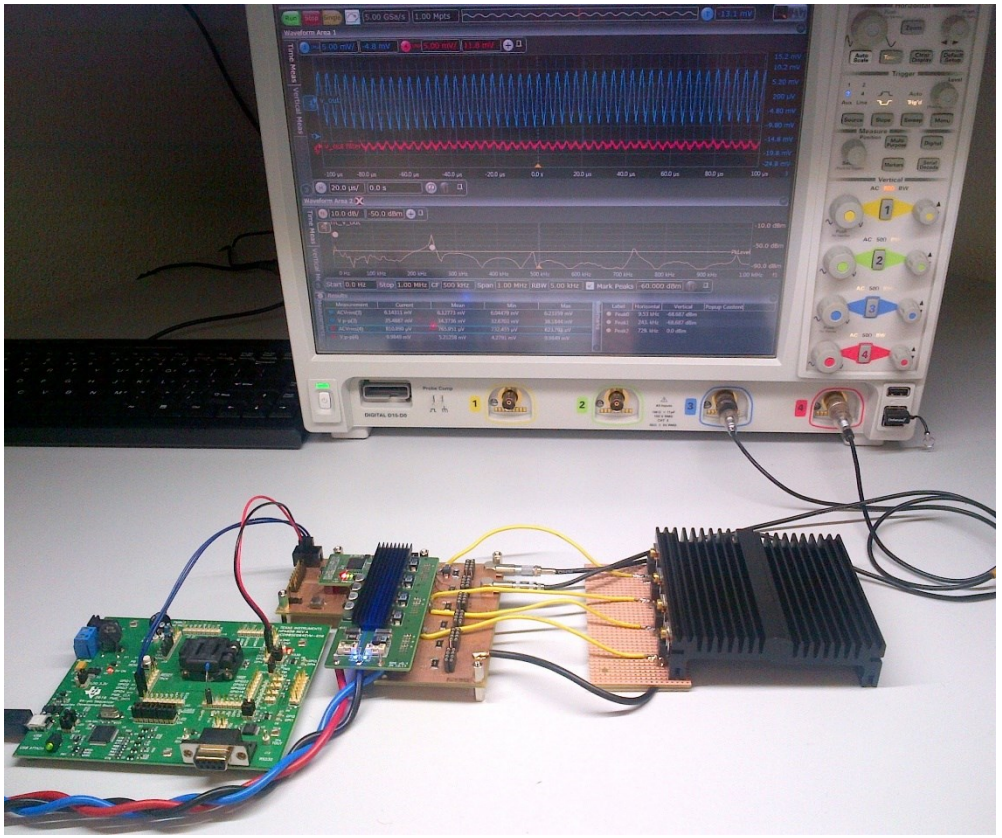
Low noise switching power supply

→ SADC power consumption
~ 30 Watts
→ 1.0V_D FPGA core voltage (10A)
→ 2.2/3.0V_A ADC voltage (3A)
→ …

→ Input voltage: 6V/12V NIM
→ crucial: residual ripple/noise of analog voltages (impact on σ_E / σ_t)

Power supply tested with 4x5A load
→ 50% of designed load
→ 200% of required load
→ below 3mV_{PP} residual ripple



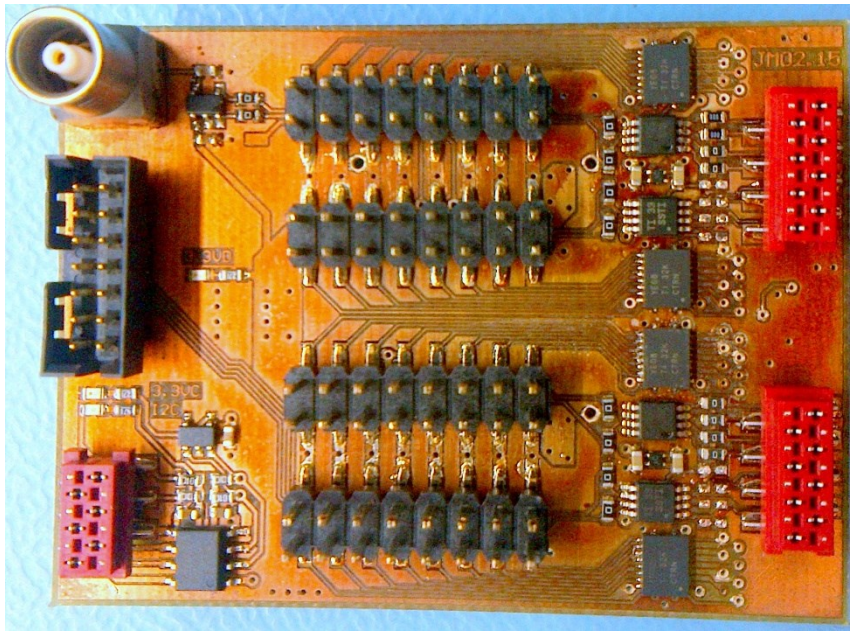


Trigger / Clock / Debug / Slowcontrol

LVTTL clock input
→ all SADCs will be phase-locked for best time reconstruction

Debugging ports for accelerated development

JTAG for FPGA configuration

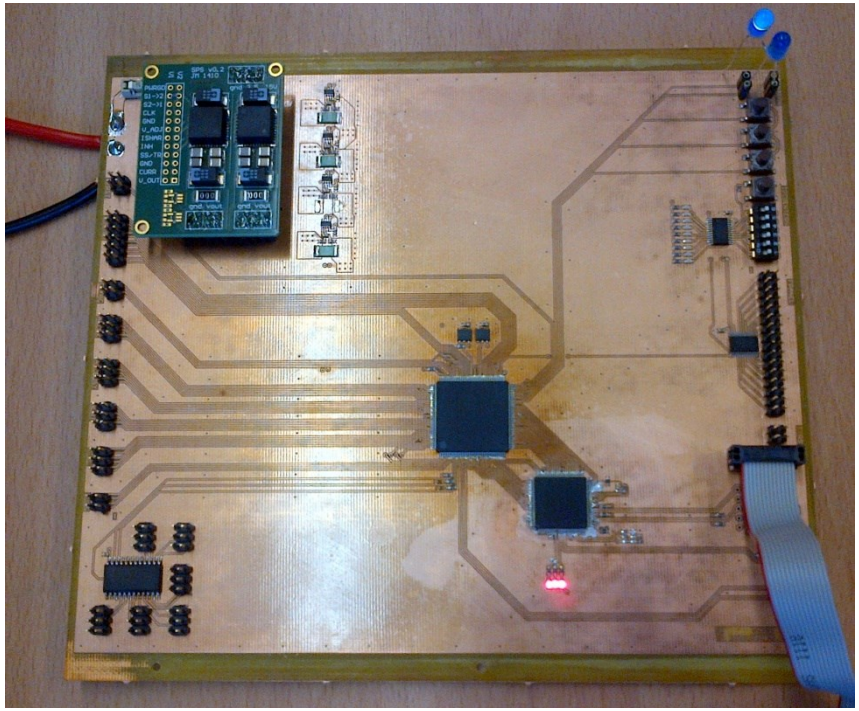


Slowcontrol (I^2C) connection (control & monitoring interface)

LVPECL I/O for DAQ sync system (Trigger)

Control Modul

- → Master student Georg Urff
- → One Control Module for 6 SADCs (384 channels)
- → Status: first prototype is produced and being programmed



Purpose:

- → Programming of FPGAs
- → Clock (phase) distribution
- → Slowcontrol of SADC
  - monitoring of U, I, T
  - voltage adjustment
  - baseline adjustment

Control Module