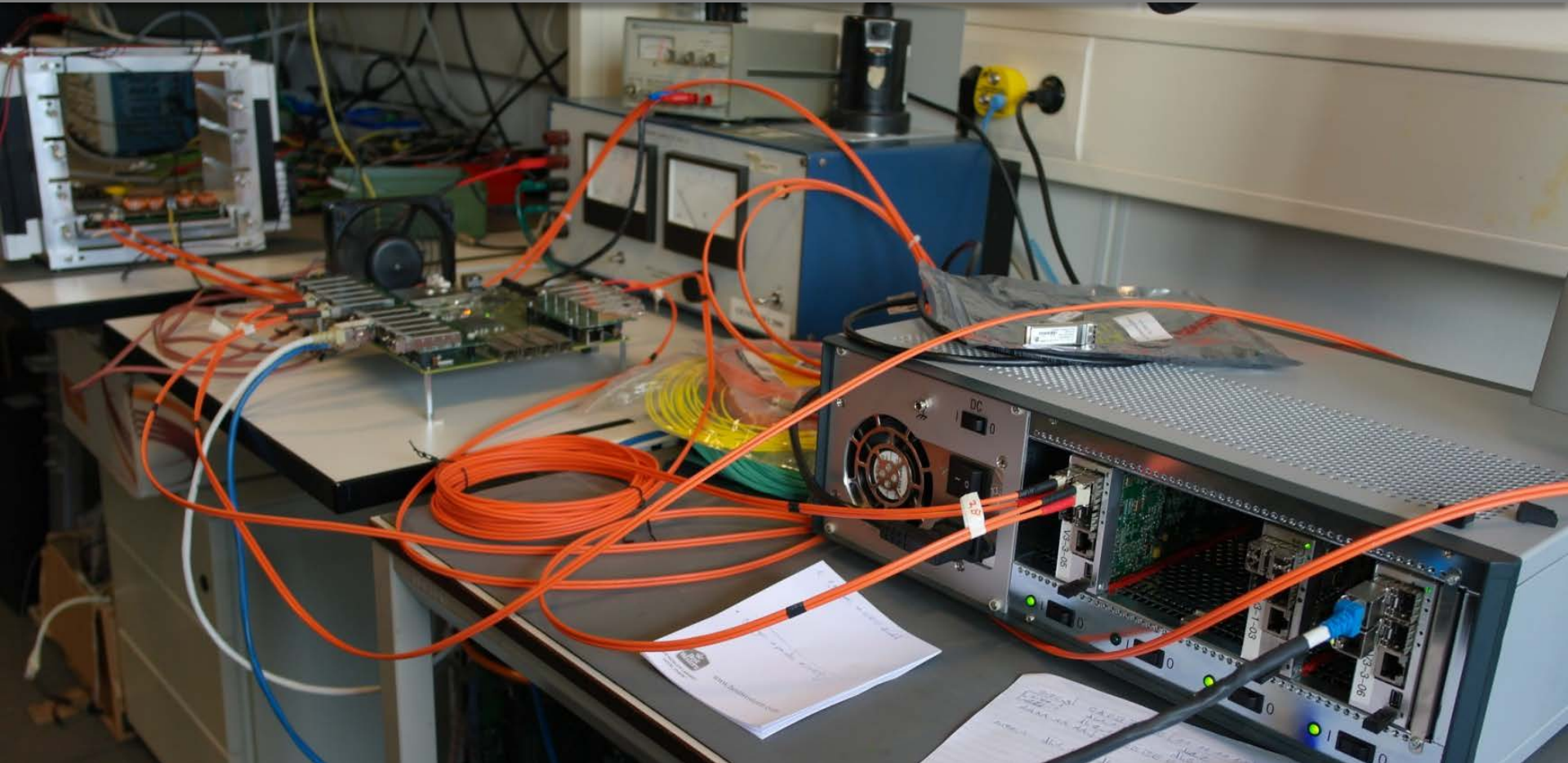
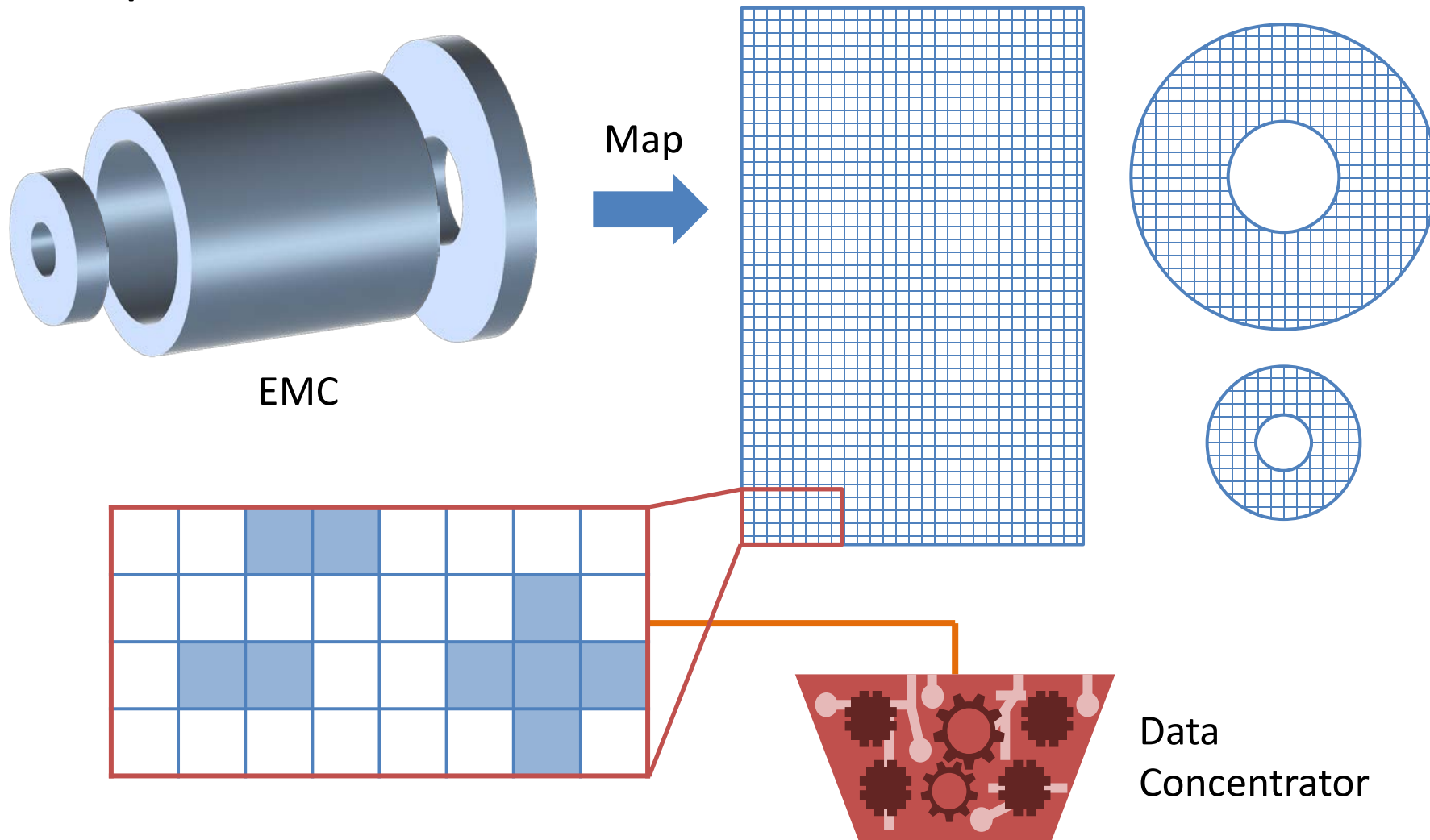




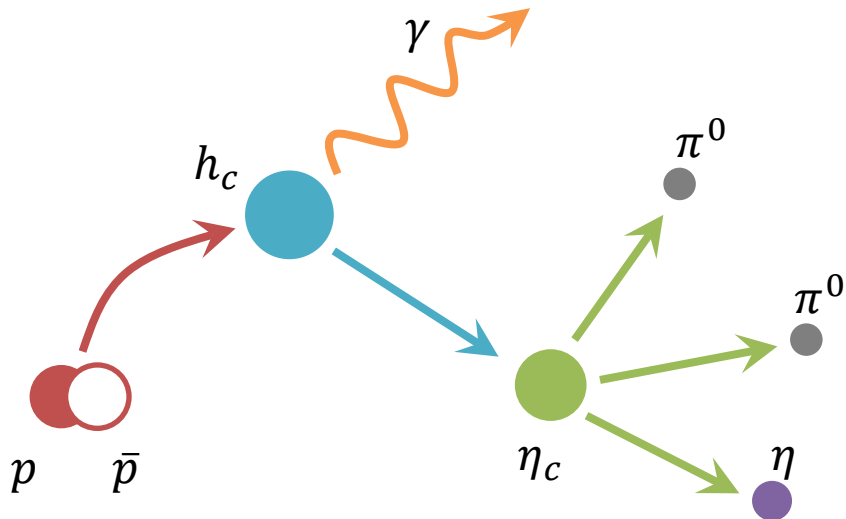
# The hardware implementation of the cluster finding algorithm and the Burst Building Network



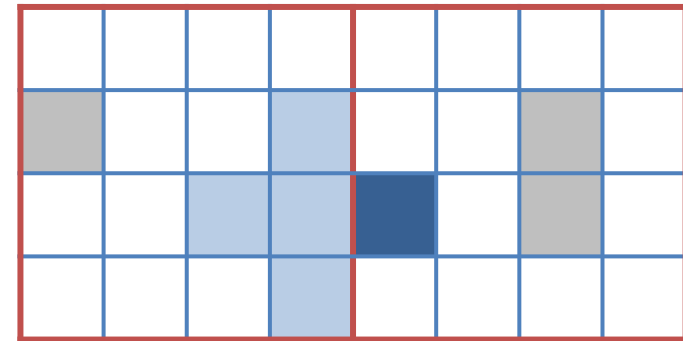
# Recap



# Distributed Cluster Finding

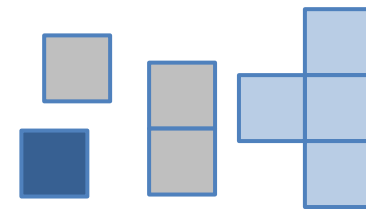


5000 events @200 kHz



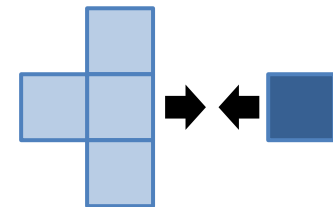
1

Form preclusters:



2

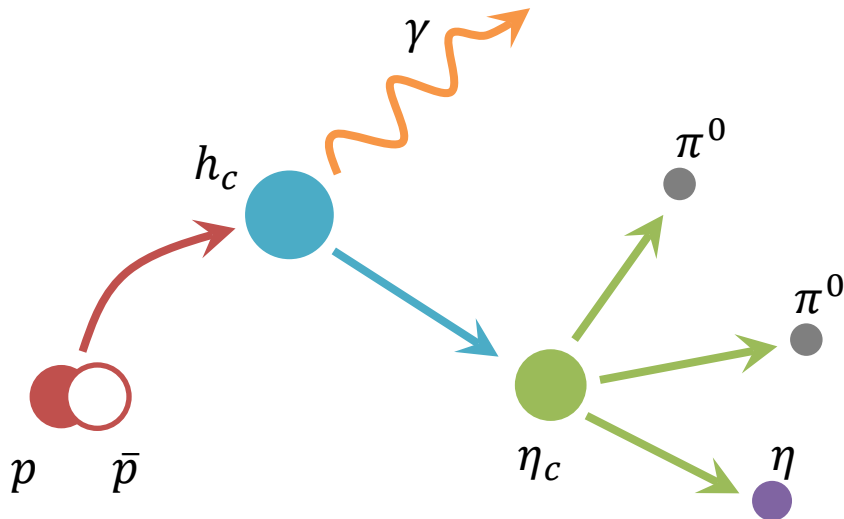
Merge preclusters:  
(if needed)



3

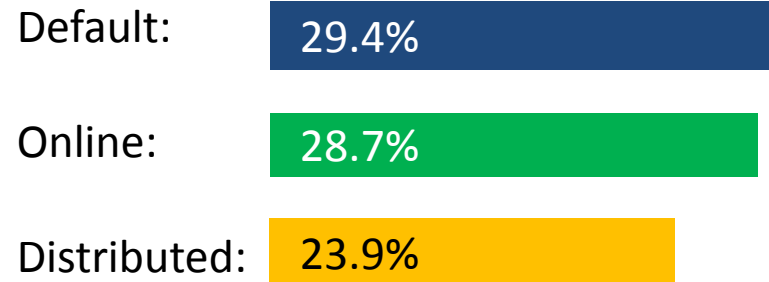
(Set properties of completed  
 clusters)

# Distributed Cluster Finding

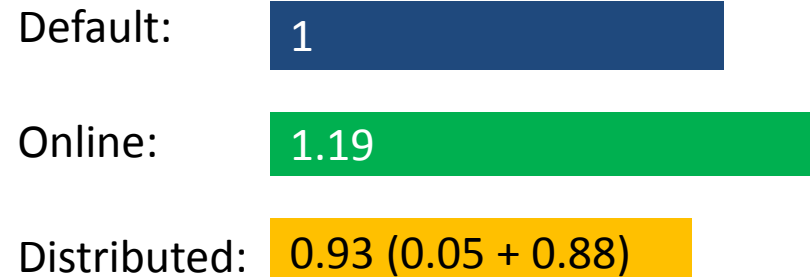


5000 events @200 kHz

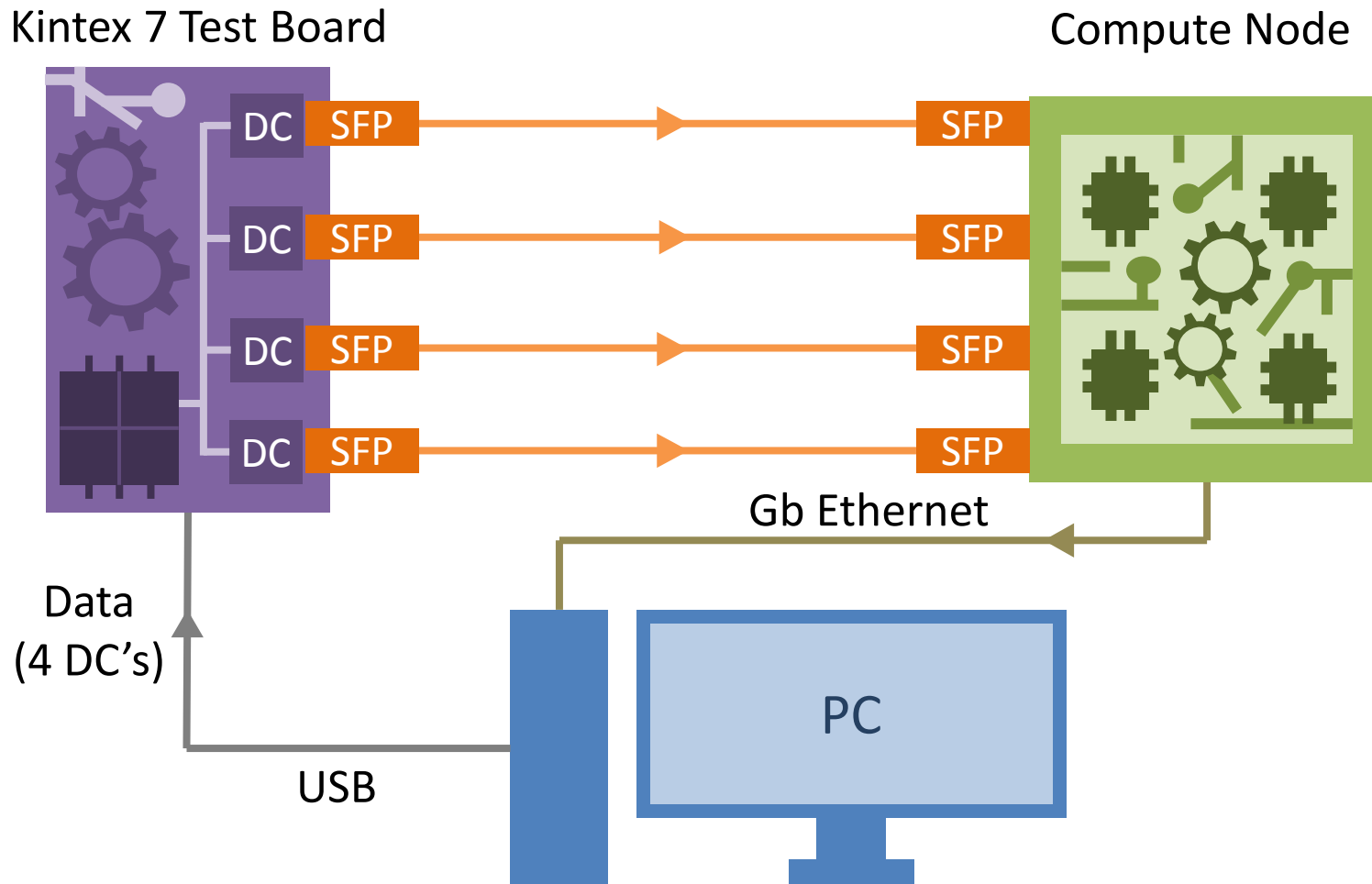
Relative nr of events reconstructed:



CPU processing time (relative to Default):

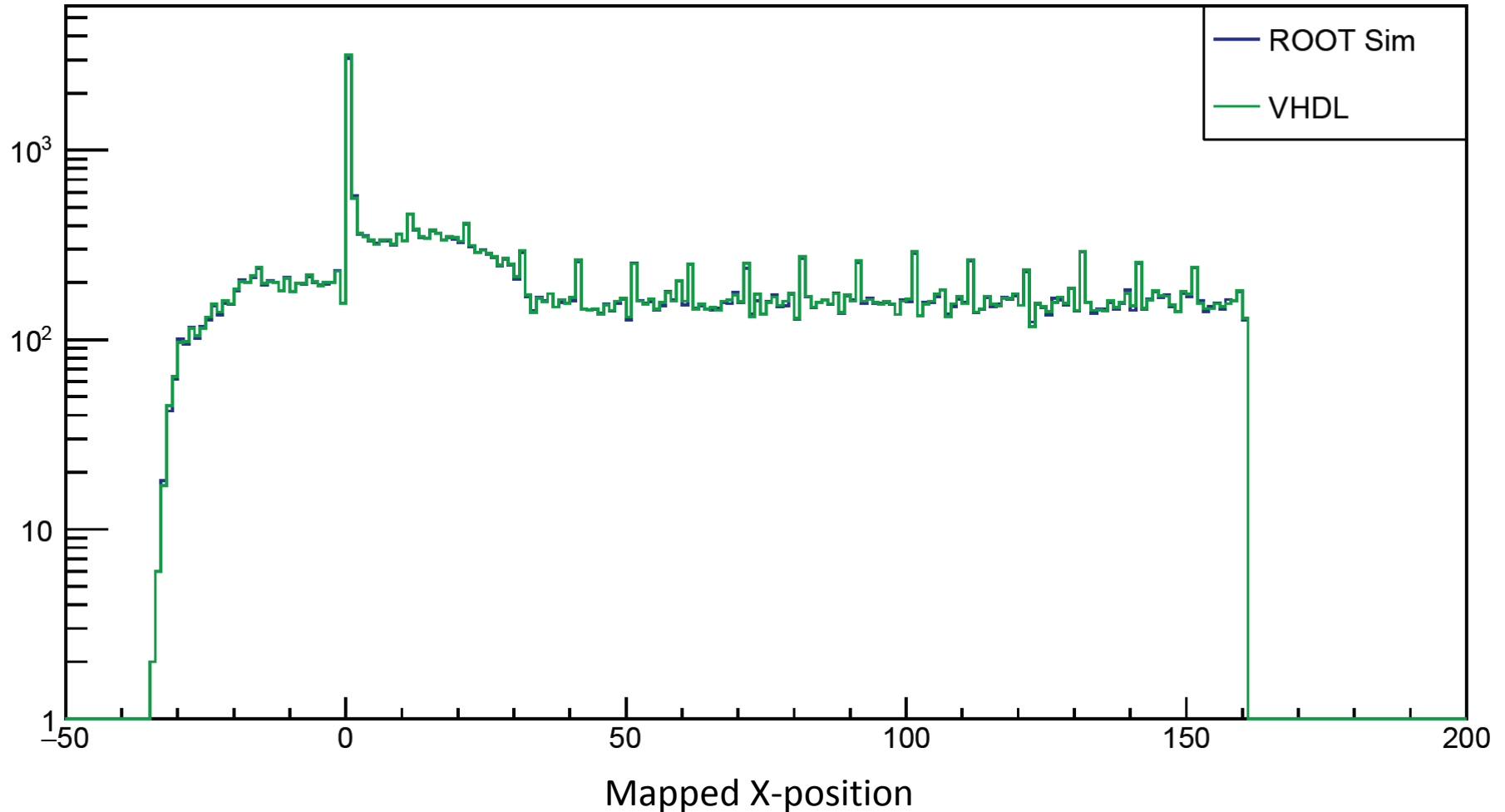


# VHDL Implementation Test Setup






# Comparison Between PandaRoot and VHDL Simulation



## Data Structure

 64-bit words

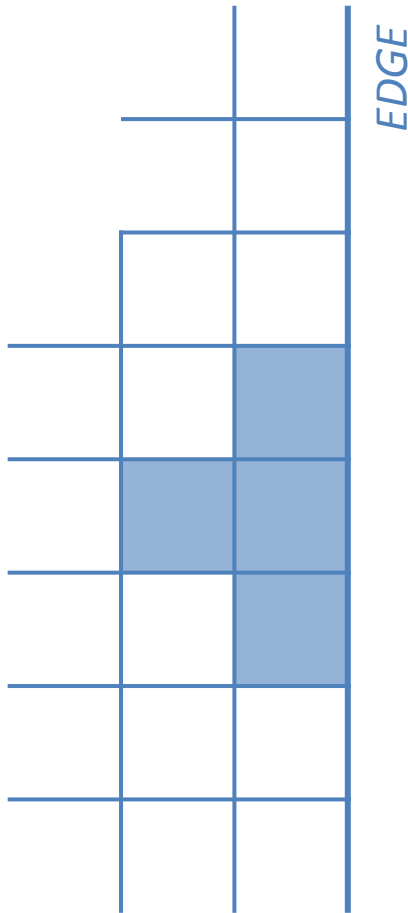
PRECLUSTER1	X	Y	D	t	NR_OF_HITS
HIT1	t	E	ch. nr		
HIT2	t	E	ch. nr		
...					



CLUSTER1	x	y	z	t	E	NR_OF_HITS
HIT1	t	E	ch. nr			
HIT2	t	E	ch. nr			
...						

X, Y: Position in 2D Map  
D : Diameter of Precluster  
t : Time  
E : Energy

## What if a Photon Hits the Edge?



### Detection:

Energy-weighted position is close to edge of map

### Options:

- 1 Discard these clusters
- 2 Apply correction factor to E
- 3 Use complicated neighbour relation to edge of other map

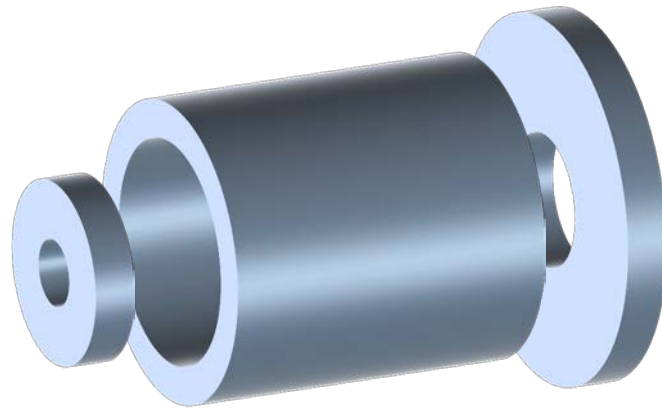




All right, so what does this all mean for the data flow, and the processing thereof?



# Data Collection

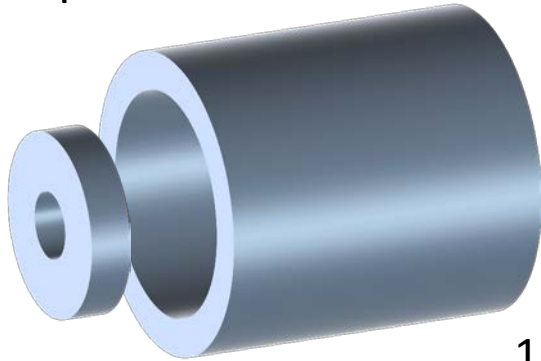


EMC

BwEndcap + Barrel	#	Rate /device (Gbps)	Total rate (Gbps)	FwEndcap	#	Rate/device (Gbps)	Total rate (Gbps)
SADCs <10 kHz	572	0.05	28.6	SADCs 300 kHz	217	1.2	260.4
SADCs >10, <50 kHz	512	0.27	138.24				
SADCs >50 kHz	112	0.6	67.2				
Total	1196		234.04		217		260.4

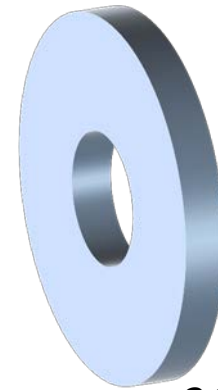
BwEndcap

Barrel



1196 digitisers  
 Total rate: 234 Gbps

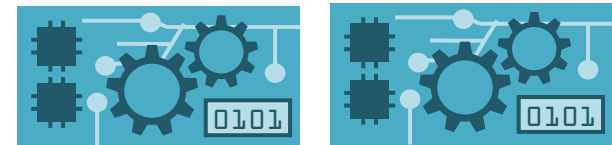
FwEndcap



217 digitisers  
 Total rate: 260 Gbps



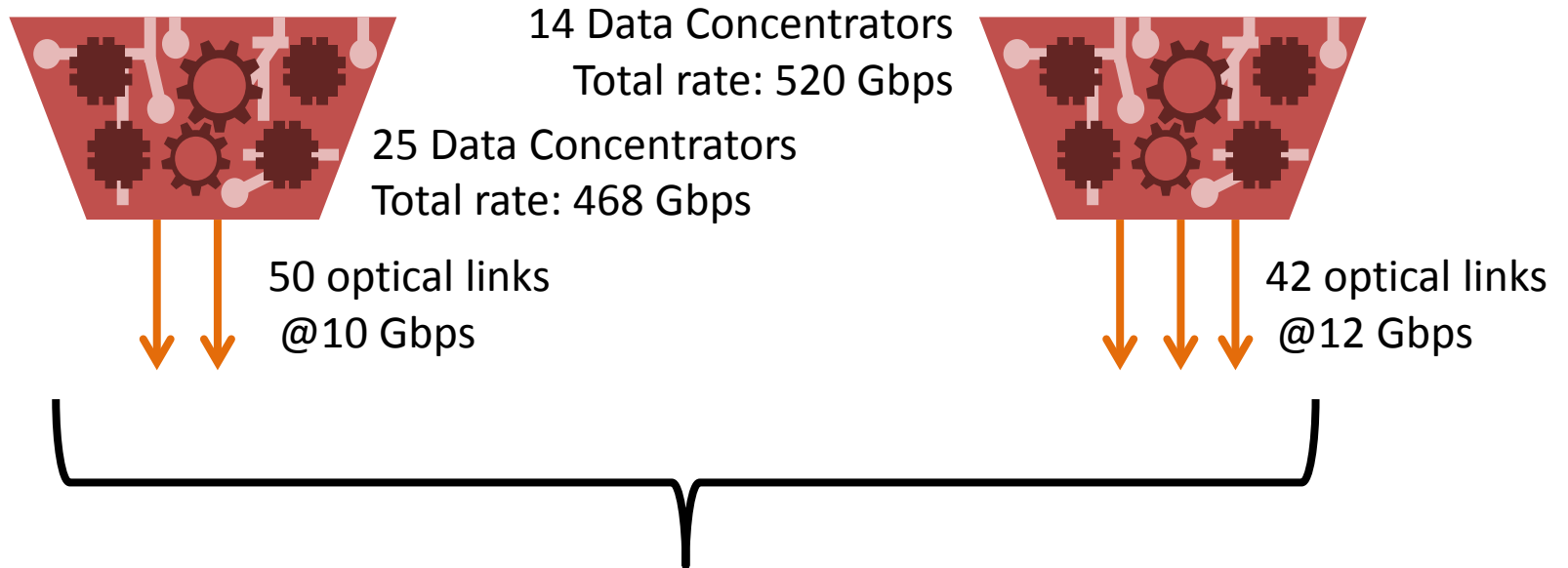
25 Data Concentrators  
 Total rate: 468 Gbps



14 Data Concentrators  
 Total rate: 520 Gbps

Assuming worst  
 case where each hit  
 becomes a cluster

## Output Produced by Data Concentrators (DCs)





## Processing the DC Output

### 3 Options for the BBN\*:

1

Throw everything into one big data collection network, which may or may not do more advanced processing (at least collect and sort data).

2

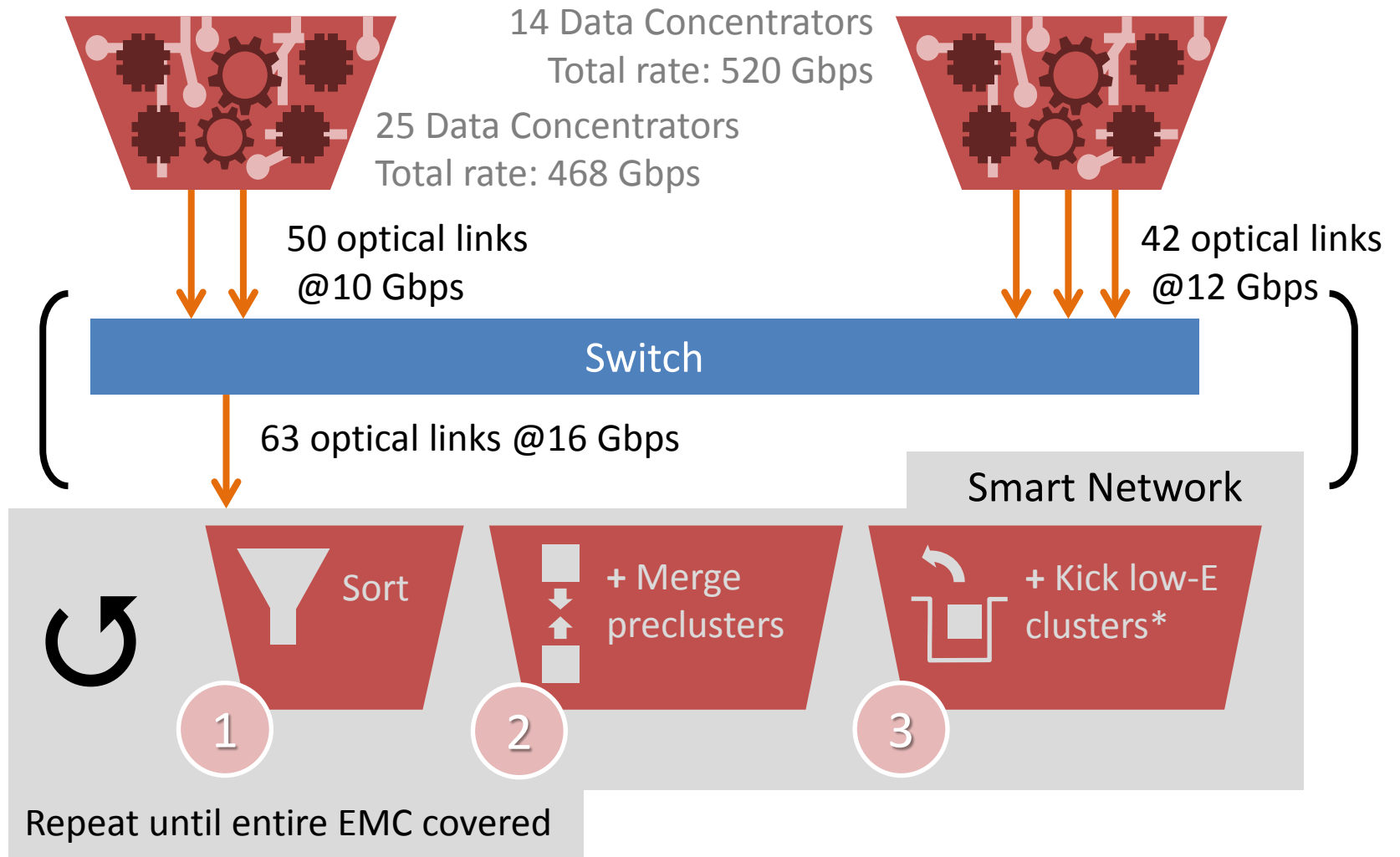
Do some data merging, then do 1.

3

Collect everything in a switch, and let one big FPGA board do the rest.

\*Burst Building Network, PANDA's data collection and processing network

# Processing the DC Output



Repeat until entire EMC covered

# Topology of the Network

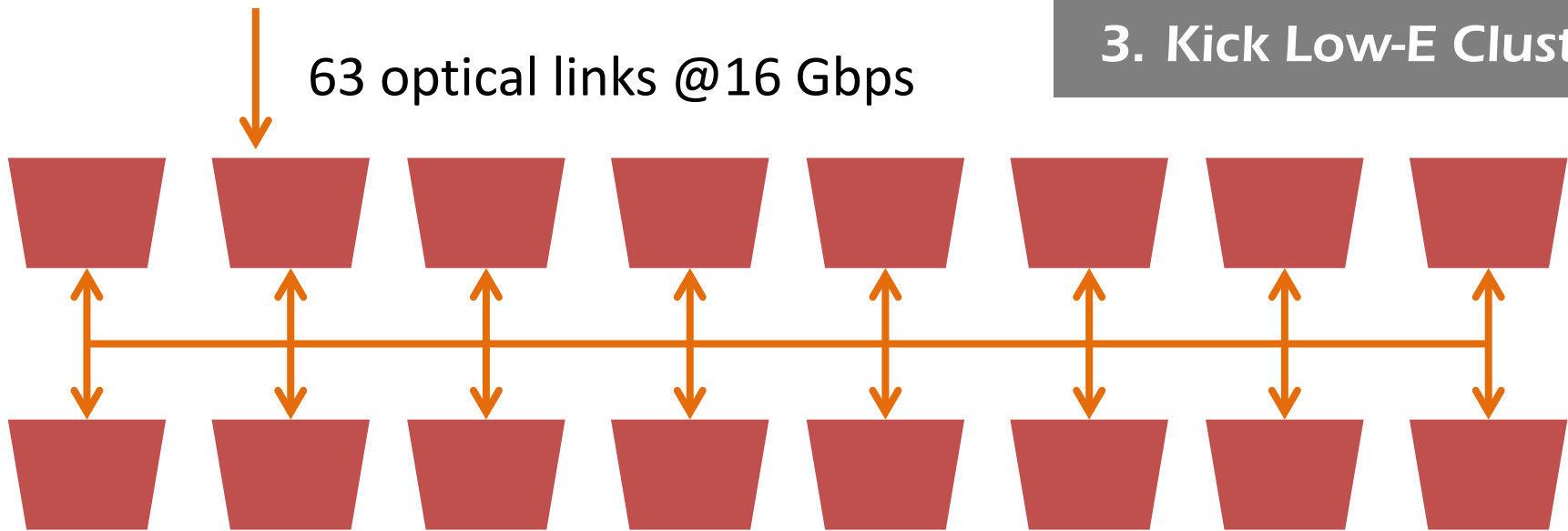
1. Sort

1

2. Merge Preclusters

3. Kick Low-E Clusters\*

63 optical links @16 Gbps



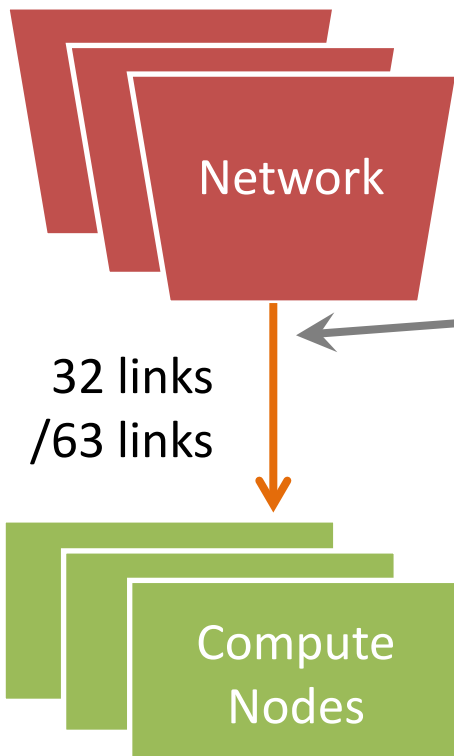
508 Gbps (if 1+2+3)  
1 Tbps (if 0 or 1)

32 Optical links (if 1+2+3)  
63 Optical links (if 0 or 1)




# Topology of the Network

1



## Procedure (after sorting):

1. Make timebunches: 
2. Send 1<sup>st</sup>  $n$  timebunches to  $n$  FPGAs on 1<sup>st</sup> CN
3. Send 2<sup>nd</sup>  $n$  timebunches to  $n$  FPGAs on 2<sup>nd</sup> CN
4. Etc until  $m$ th CN, then send to 1<sup>st</sup> CN again and repeat from 2.





## Processing the DC Output

### 3 Options for the BBN:

1

Throw everything into one big data collection network, which may or may not do more advanced processing (at least collect and sort data).

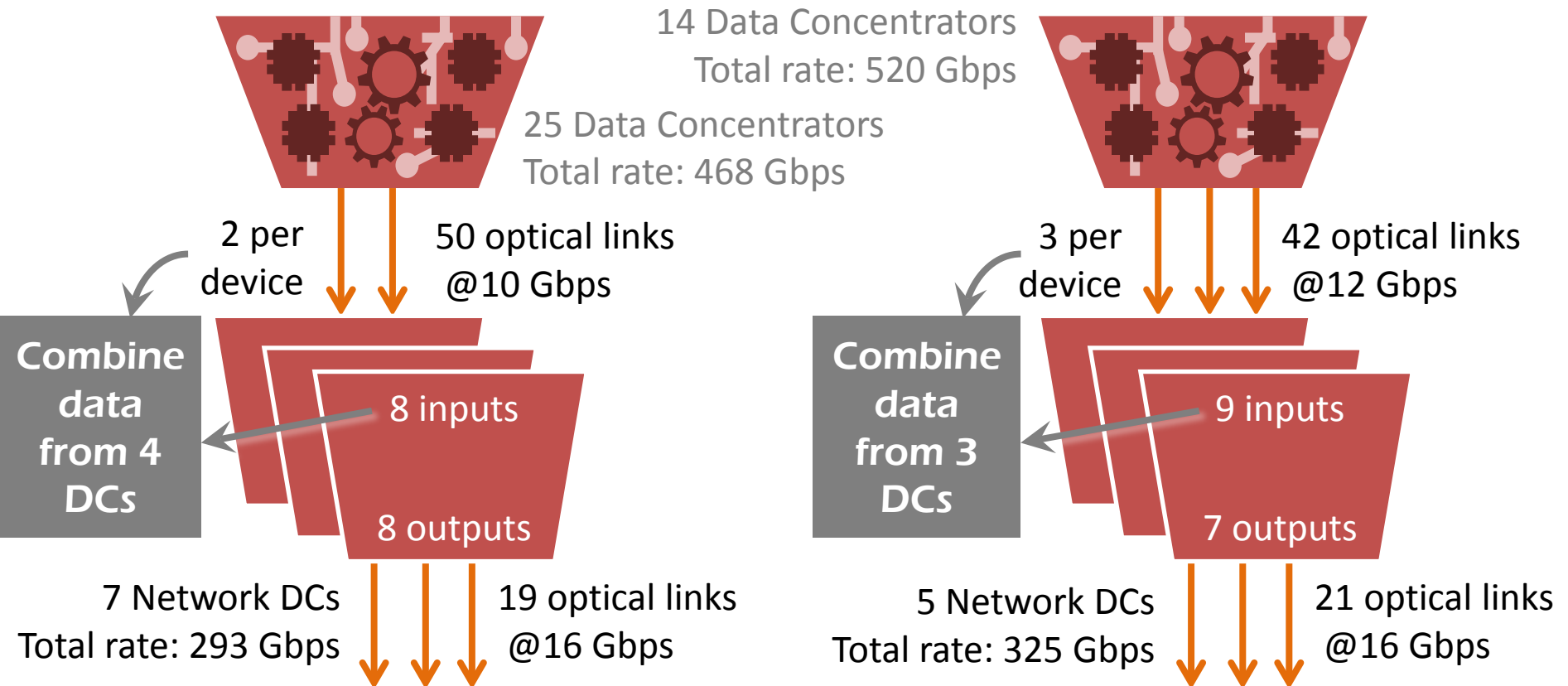
2

Do some data merging, then do 1.

3

Collect everything in a switch, and let one big FPGA board do the rest.

# Processing the DC Output



---> (Uncombined: 63 links @988 Gbps)



# Processing the DC Output

## 3 Options for the BBN:

1

Throw everything into one big data collection network, which may or may not do more advanced processing (at least collect and sort data).

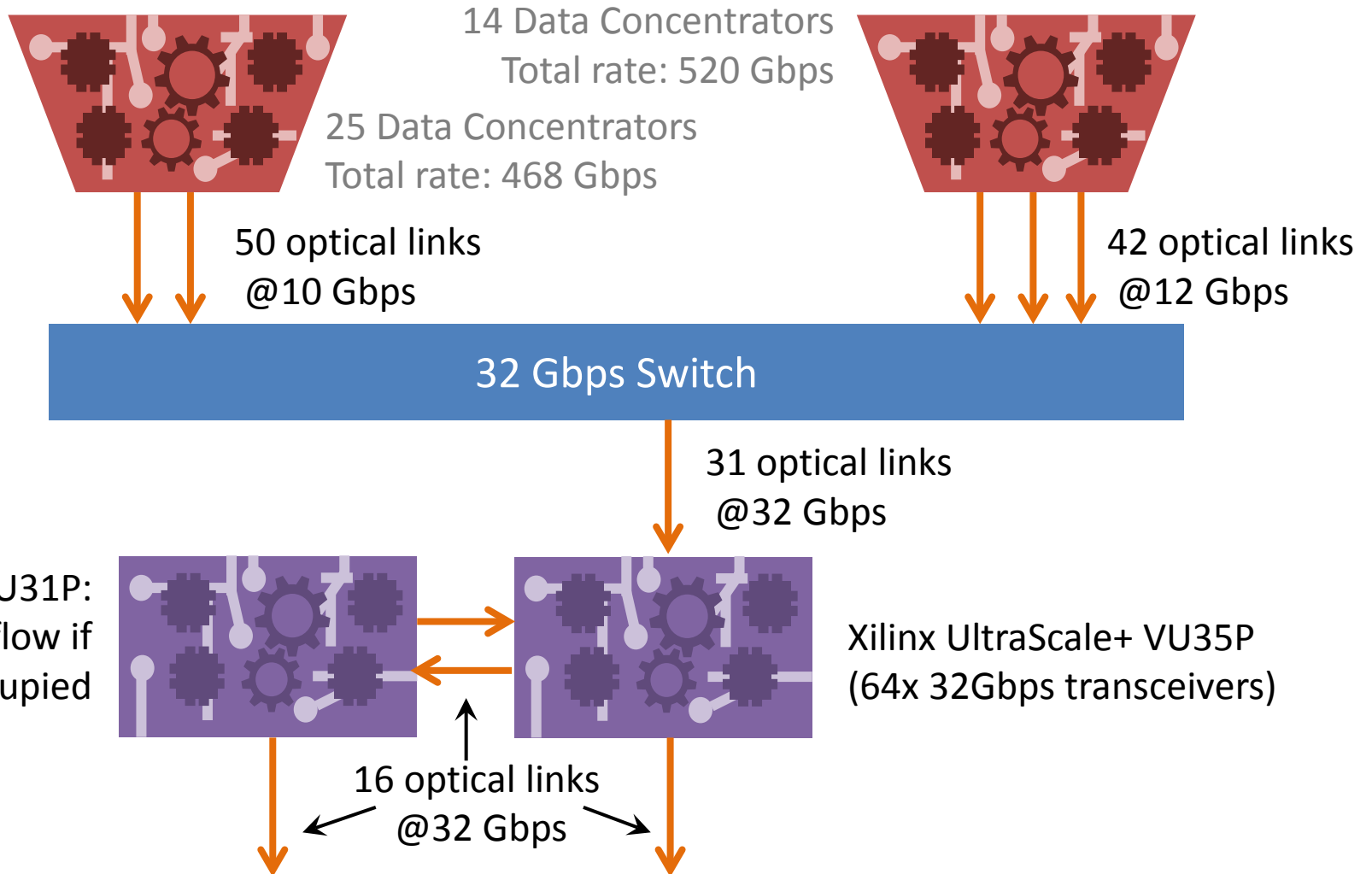
2

Do some data merging, then do 1.

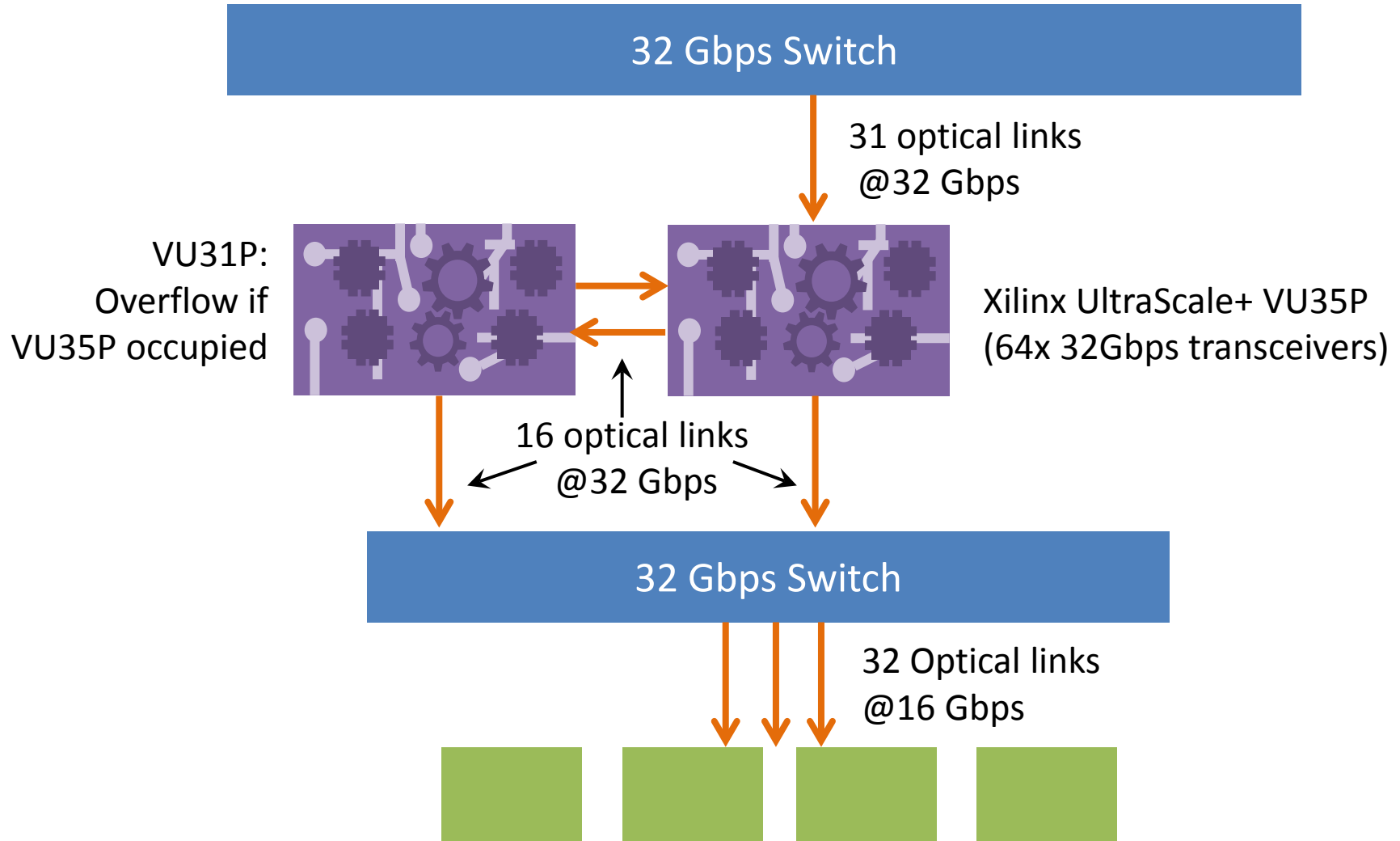
3

Collect everything in a switch, and let one big FPGA board do the rest.

# Processing the DC Output



# Processing the DC Output



## Summary and Outlook

1 Hardware implementation of clustering has been made:

a Results agree with PandaRoot sim.

b → Check with FPGA specifications to explore possibilities.

2 Several options for the BBN are being explored.

### Recommendation:

1 Use Option 3 (big FPGA board).

2 If not possible (see 1b), use Option 2 (do data merging, then feed to BBN).



*Open Question to Collaboration:*

What do other subsystems require of the BBN?

