Workshop on fast Cherenkov detectors

Giessen , 11-13 May 2009

Microelectronics
for
Silicon-PM readout

Christophe de La Taille , LAL Orsay, France

Presented by Joël Pouthas , IPN Orsay

IN2P3 CSNSM LAL LPN IPN rsay

Omega

Orsay Micro-Electronics

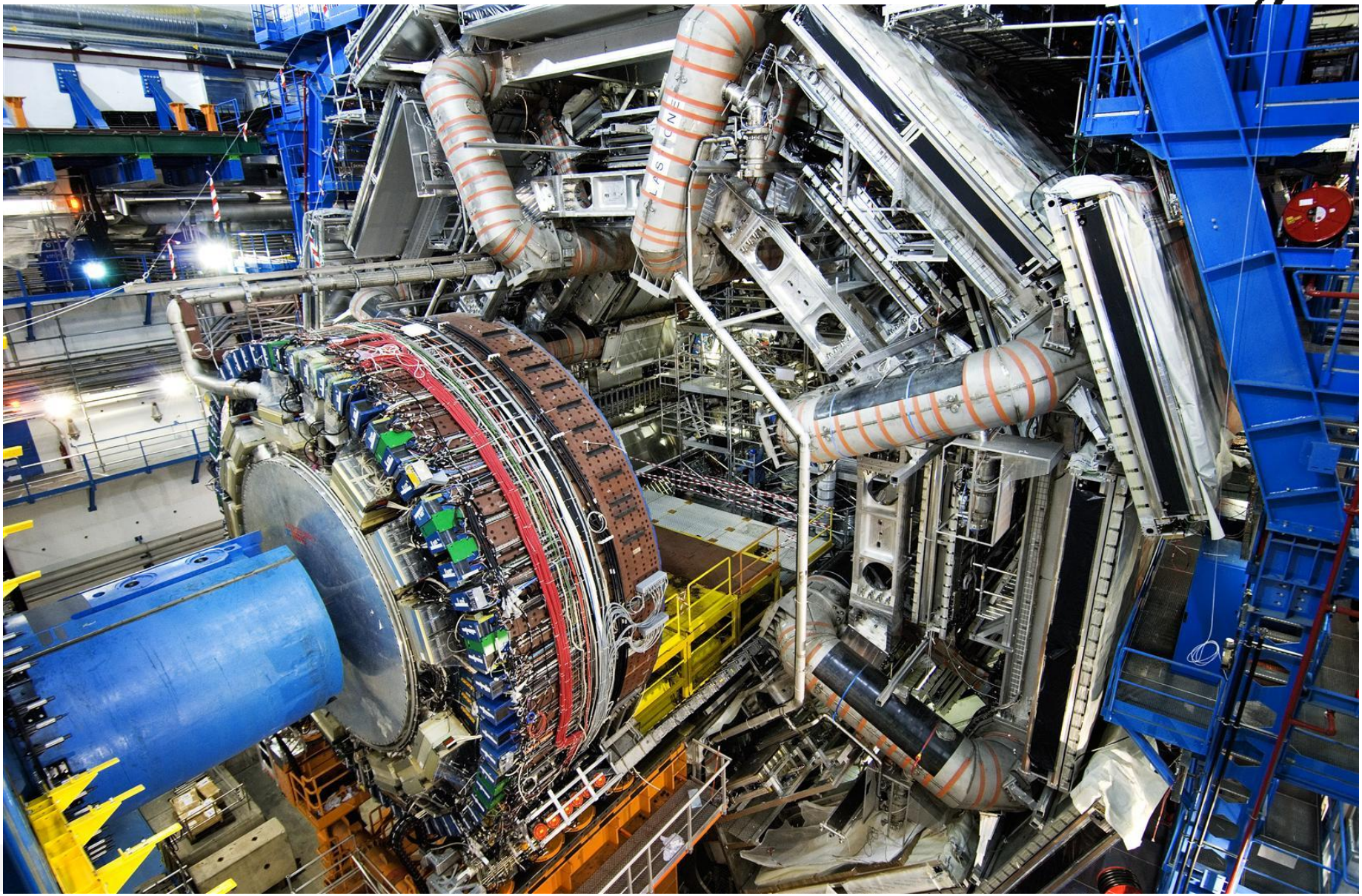
Groups Associated

P. Barrillon, S. Blin, S. Callier, S. Conforti, F. Dulucq, J. Fleury, C. de La Taille, G. Martin-Chassard, L. Raux, N. Seguin-Moreau

+ Wei Wei from IHEP Beijing

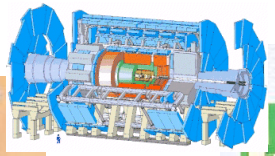
Orsay MicroElectronic Group Associated

ATLAS at LHC

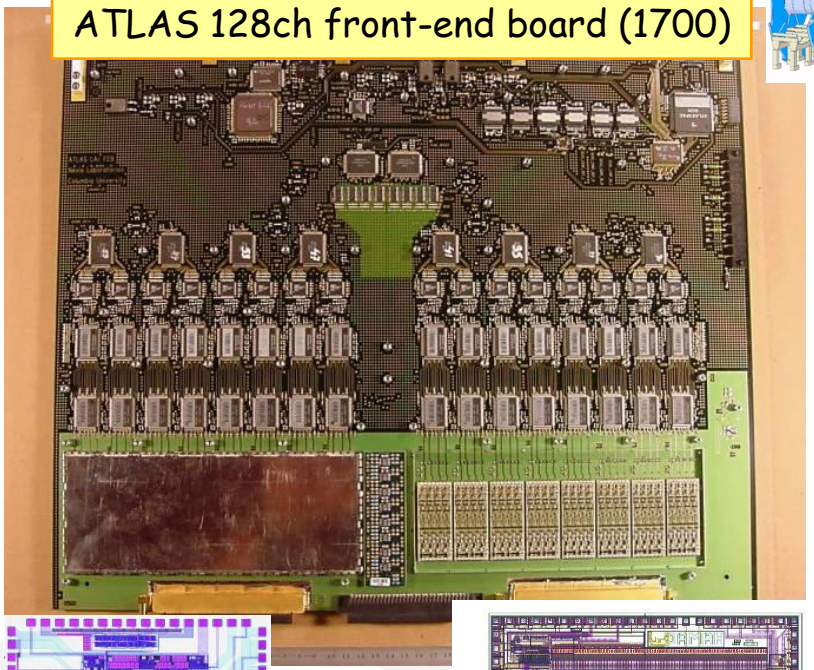


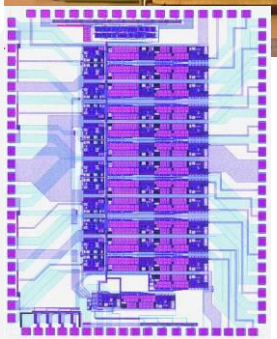
ASIC production for ATLAS LAr calorimeter

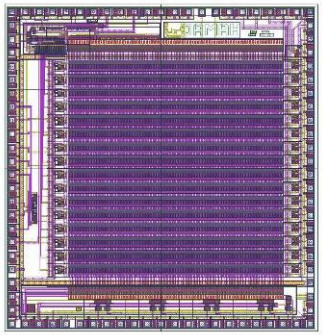
ATLAS 128ch front-end board (1700)

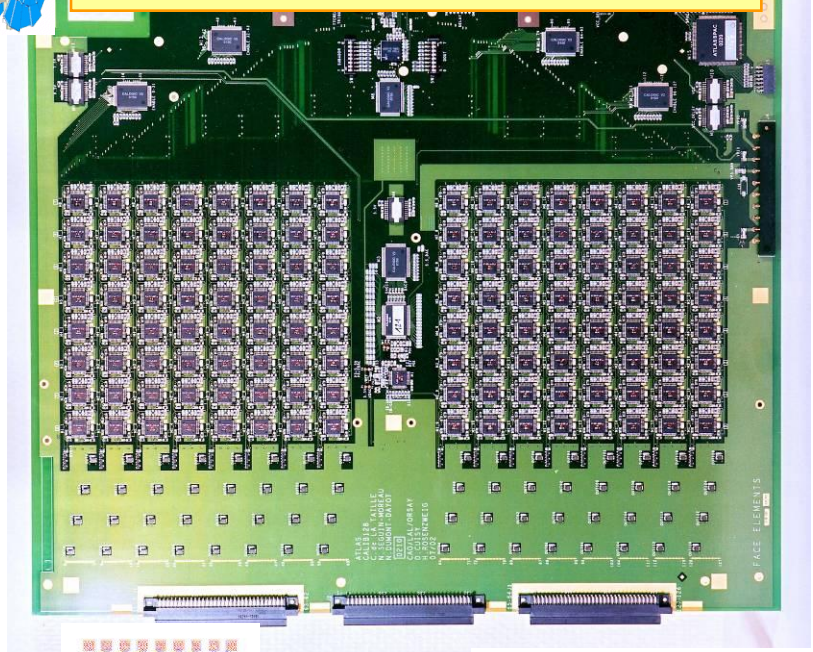


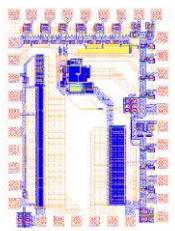
ATLAS 128ch calibration board (135)

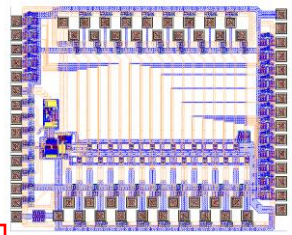












SHAPER_V3 (1999)
4 ch. tri-gain (1,10,100)
fast-shaper (30ns)
BiCMOS 1.2µm
70 000 chips

HAMAC (2000)
16 ch 12 bits analog memory
Ecriture/lecture : 40/5Mhz
DMILL 0.8µ
84 000 chips

LOANA (2002)
Low offset opamp (<10 µV) +
switch HF (50µV →5V à 1‰)
DMILL 0.8µ
40 000 chips

DAC (2003)
R/2R 16 bits
DMILL 0.8µ
8 000 chips

Microelectronics at IN2P3 (Fr)

- Large force of microelectronics experienced engineers (~50)
- Expertise in detectors, chip design and test
- Common Cadence tools

- Continuous increase of chip complexity

- Actions :
  - Building blocks
  - Networking
  - Poles:
    - OMEGA at Orsay
    - Strasbourg
    - Dipole Lyon-Clermont

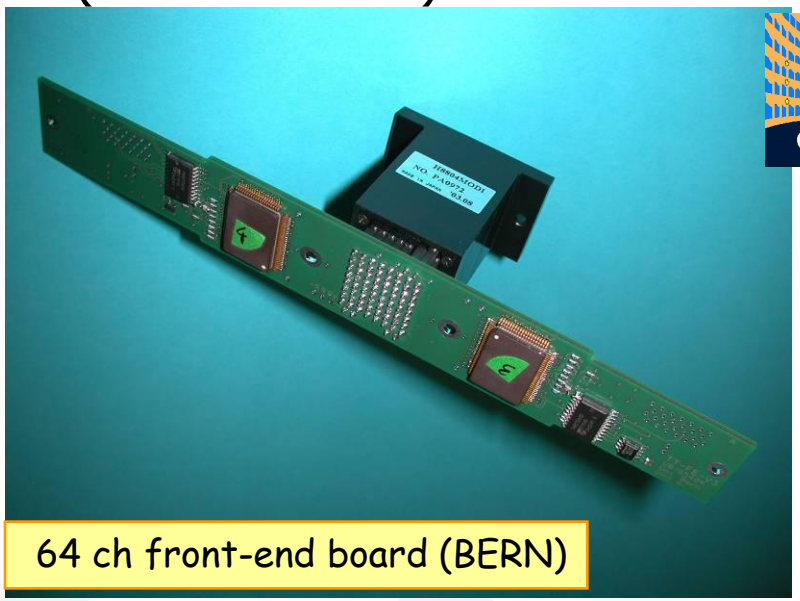
OMEGA
is a microelectronics design center
created in October 2007

The pole is hosted by LAL
and gathers 4 laboratories:

LAL, IPNO, LLR and CSNSM

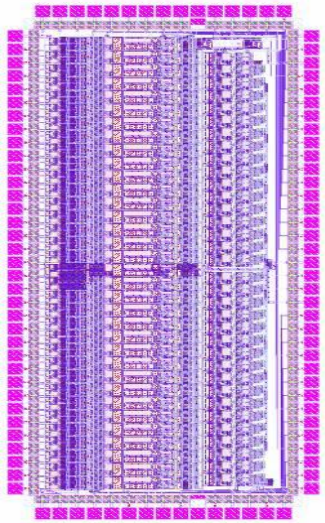
ASIC production for OPERA target tracker

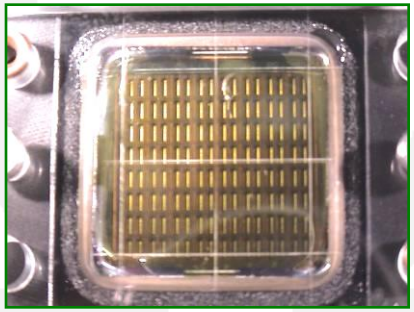
- Readout ASIC for multi-anode Photomultiplier (Hamamatsu)

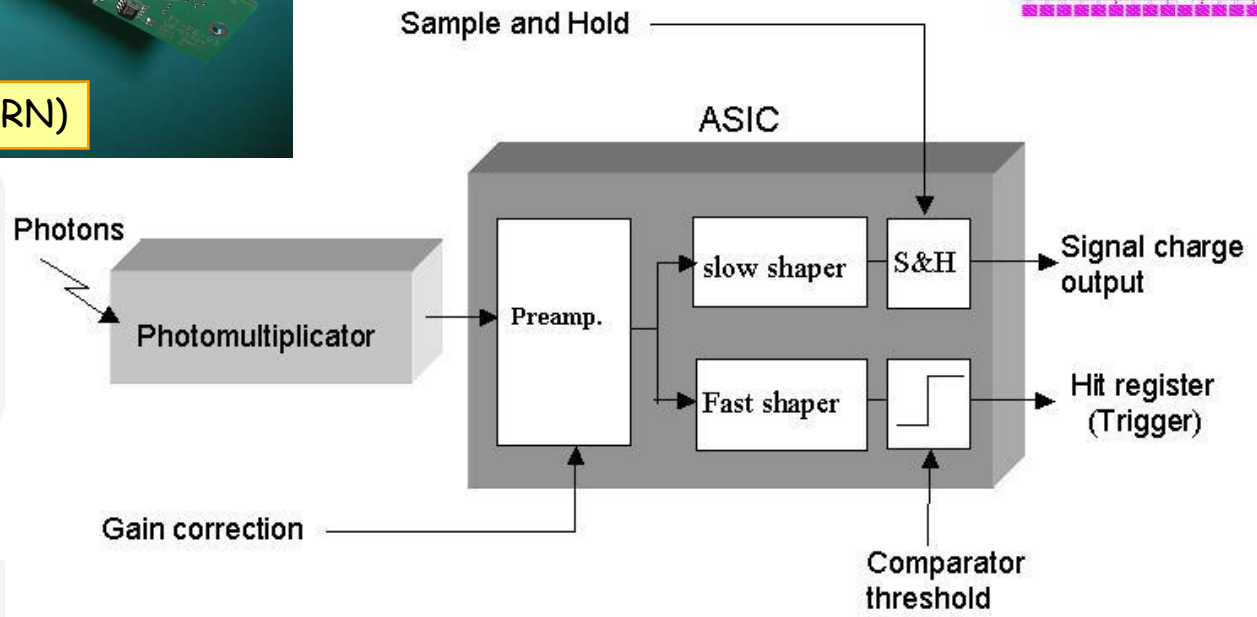


64 ch front-end board (BERN)

OPERA_ROC (2002)
32 channels
Variable gain preamp
Autotrigger on ¼ p.e.
BiCMOS 0.8µ
3 000 chips



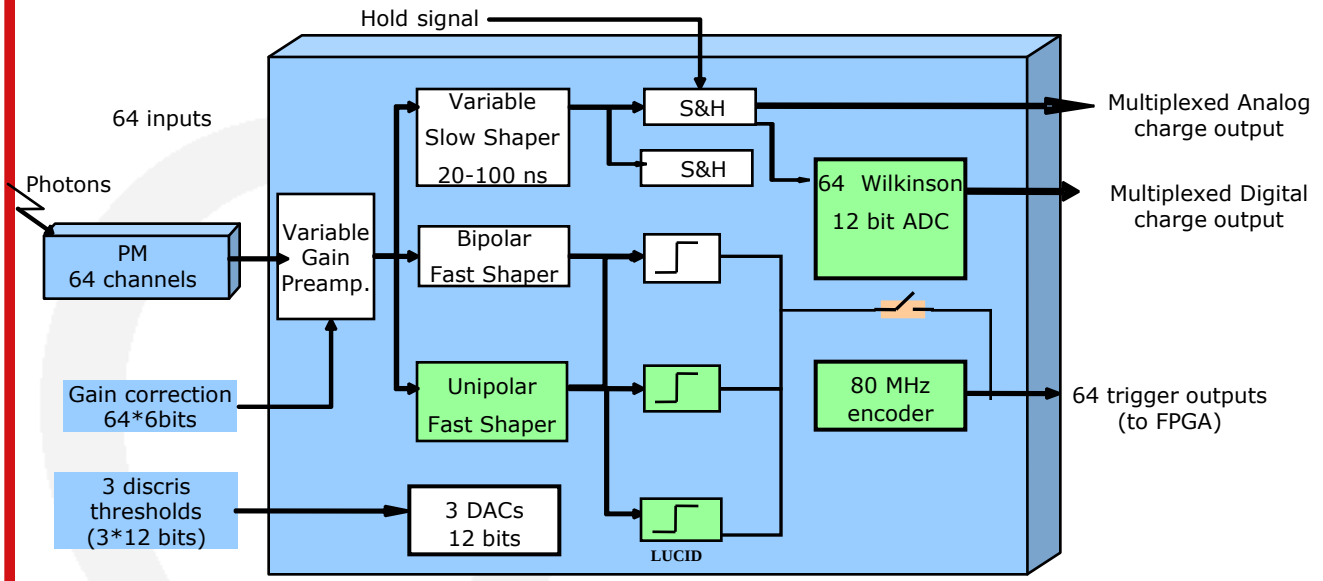


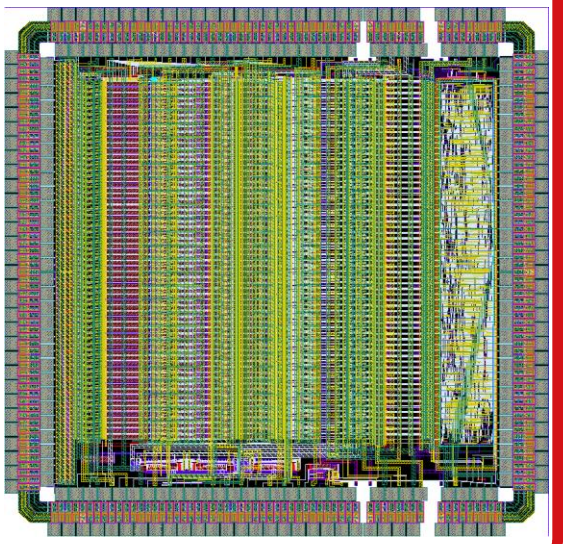


MAROC : 64 ch MAPMT chip for ATLAS lumi

Complete front-end chip for 64 channels multi-anode photomultipliers

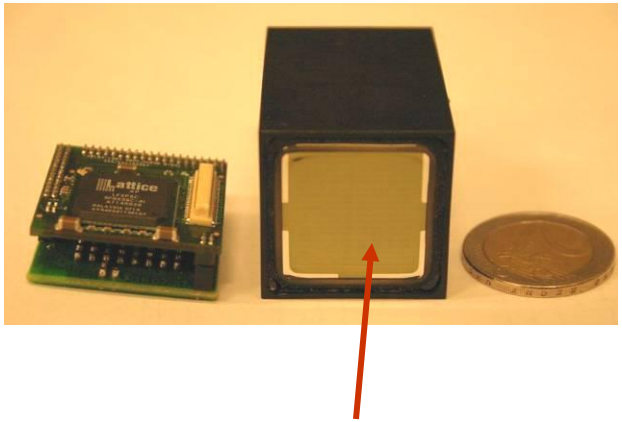
- Auto-trigger on 1/3 p.e. at 10 MHz, 12 bit charge output
- SiGe 0.35 µm, 12 mm2, Pd = 350mW



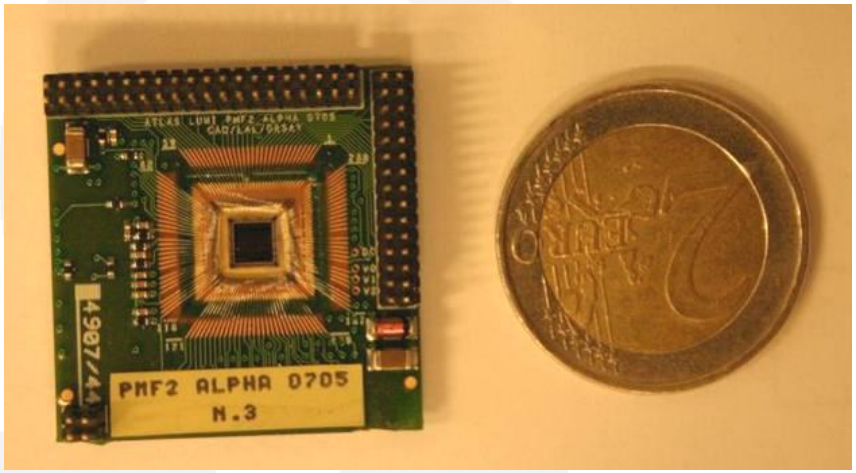


Active board pictures

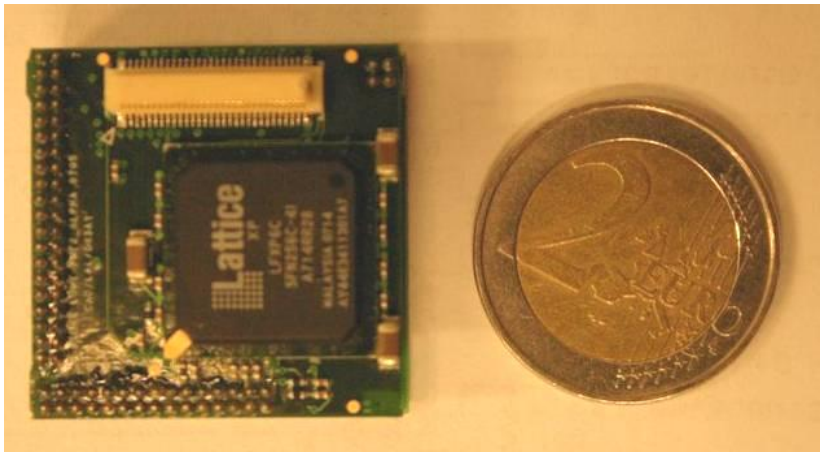
MAROC2 chip bounded at CERN



64 ch PMT



MAROC side

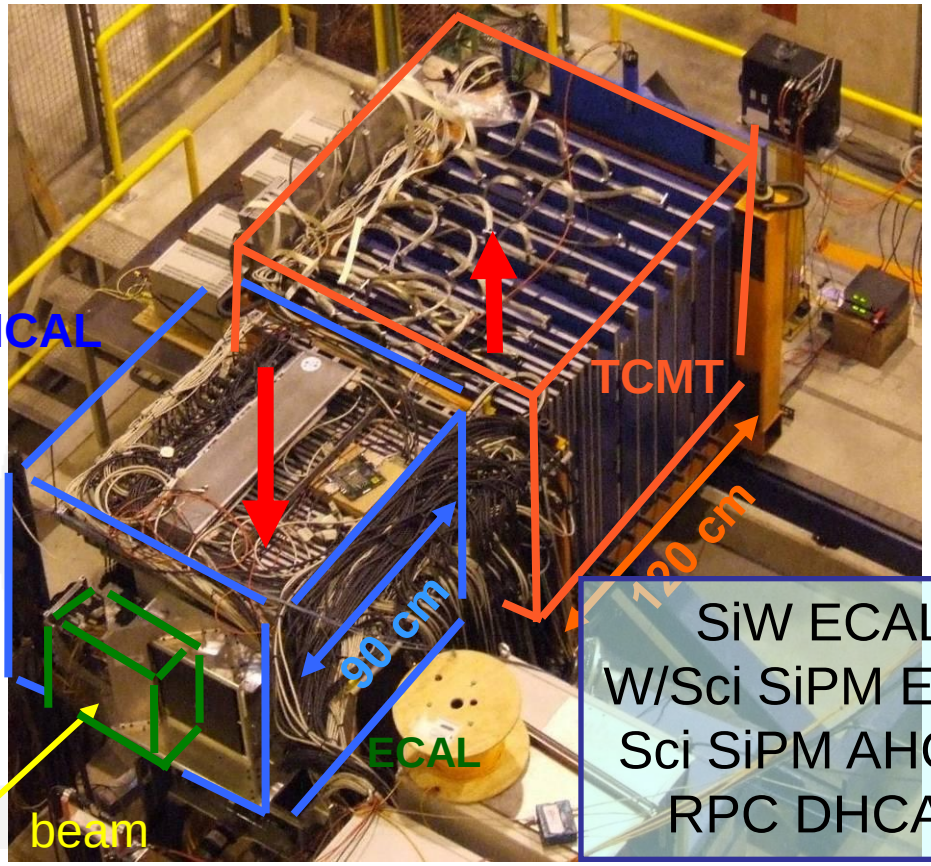


Lattice side

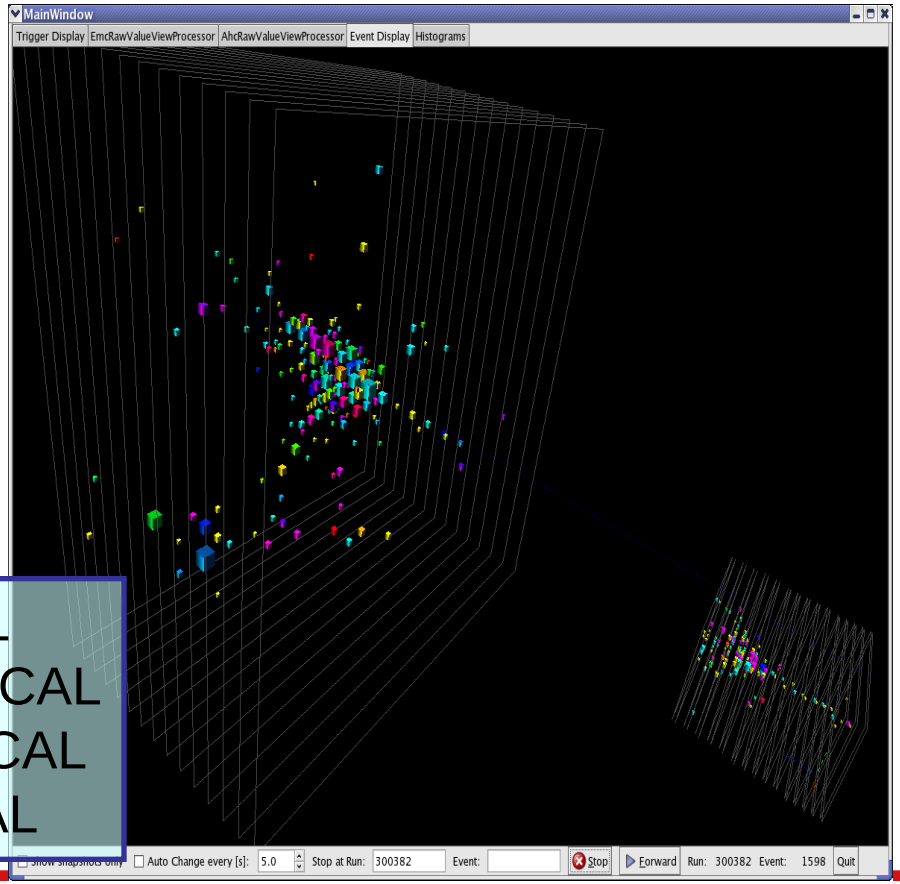
CALICE : imaging caorimetry

- After LHC : New imaging calorimetry…at the ILC
- Improve jets measurement by Particle flow algorithm
- CALICE : 281 phys., 47 labs, 12 countries.

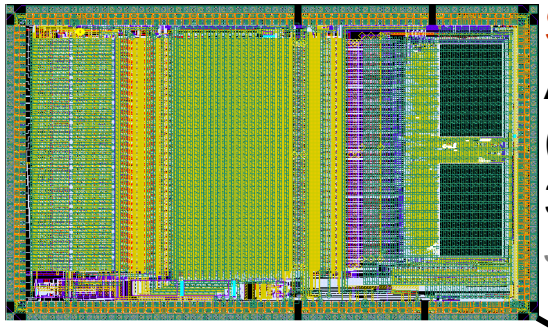
Chairperson : JC Brient http://llr.in2p3.fr/activites/physique/flc/calice.htm



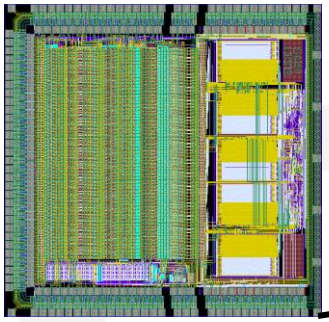
SiW ECAL
W/Sci SiPM ECAL
Sci SiPM AHCAL
RPC DHCAL



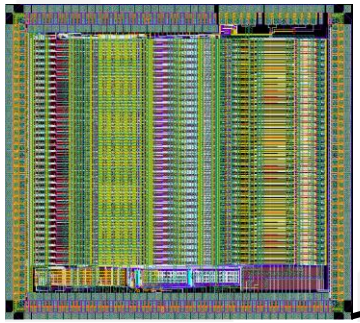
The front-end ASICs : the ROC chips



SPIROC
Analog HCAL
(SiPM)
36 ch. 32mm²
June 07

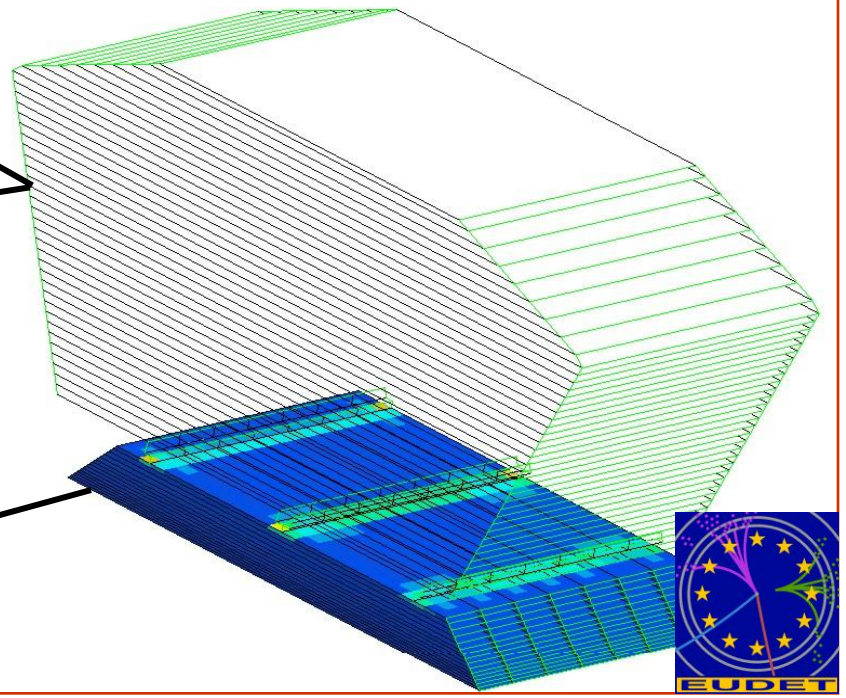


HARDROC
Digital HCAL
(RPC, µmegas or GEMs)
64 ch. 16mm²
Sept 06



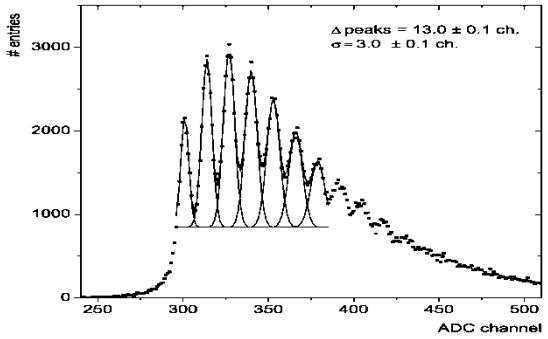
SKIROC
ECAL
(Si PIN diode)
36 ch. 20mm²
Nov 06

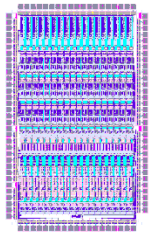
- Technological prototypes : full scale modules (~2m)
- EUDET EU funding (06-09)
- ECAL, AHCAL, DHCAL
- B=5T



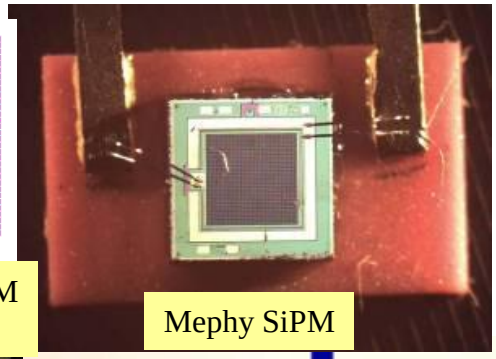
CALICE AHCAL testbeam prototype

- Hadronic calorimeter prototype for the ILC : 1 cubic metre, 38 layers, 2cm steel plates
- 8000 tiles with SiPMs fabricated by MePHY group

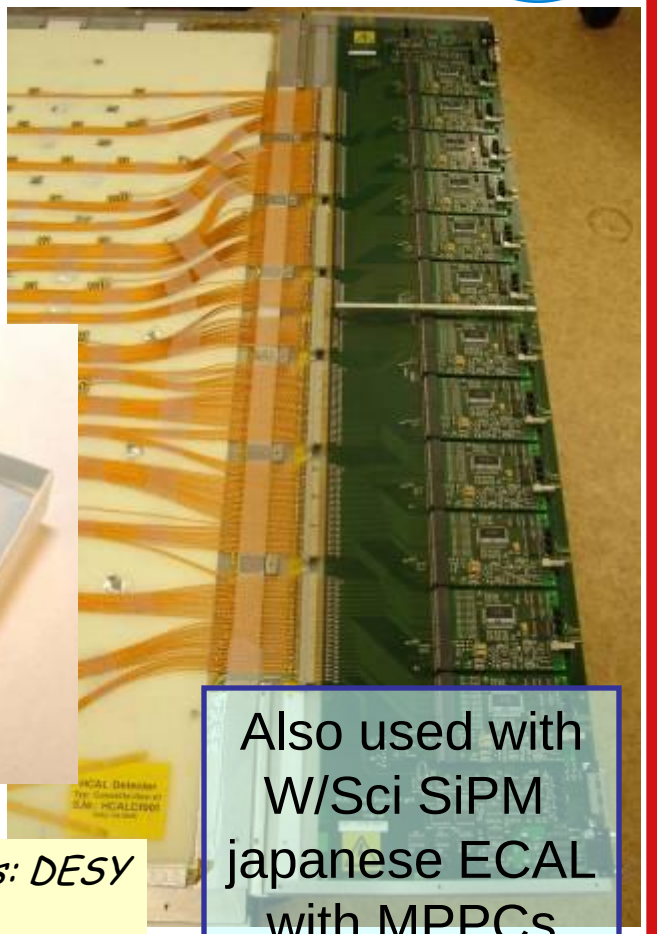


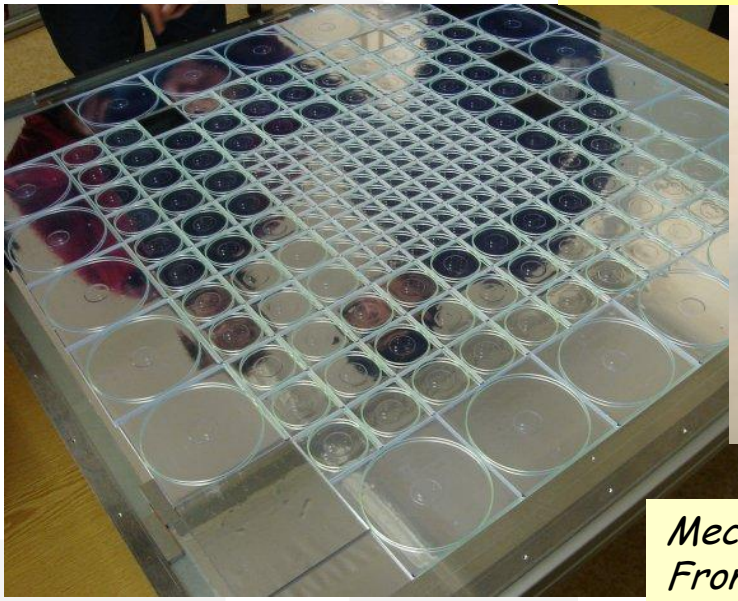


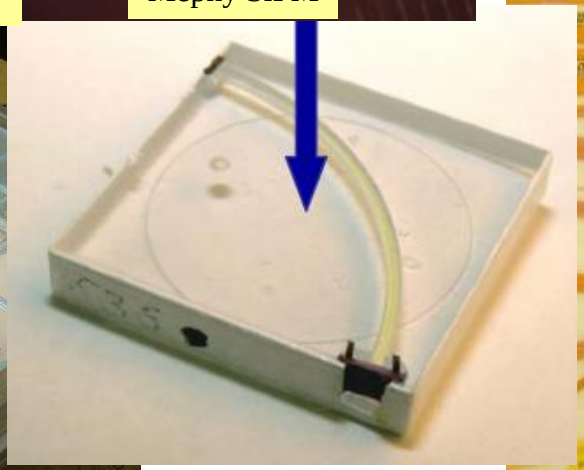
FLC_SiPM ASIC



Mephy SiPM





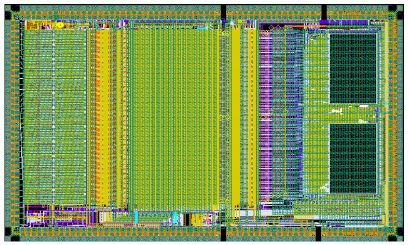


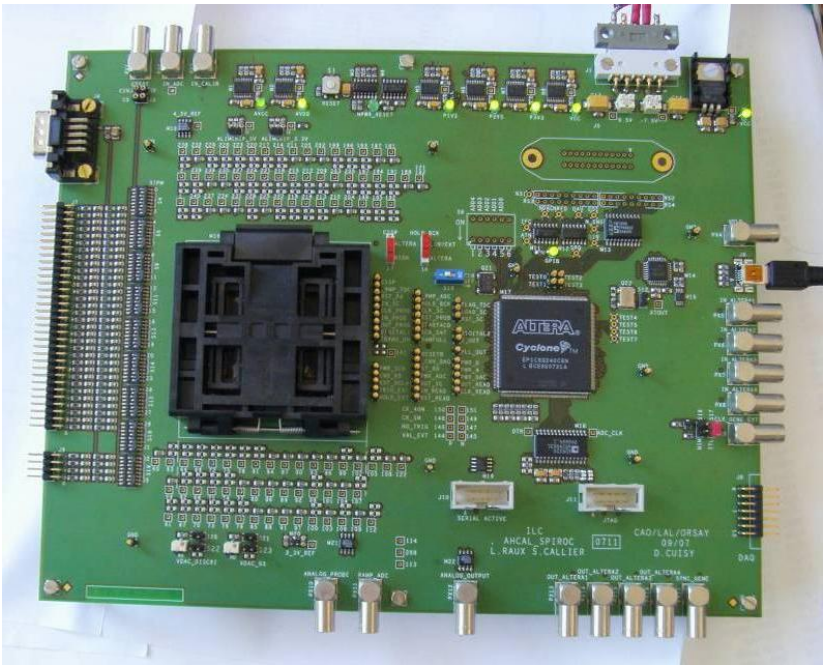
Mechanics and front end boards: DESY
Front end ASICs: LAL

Also used with W/Sci SiPM japanese ECAL with MPPCs

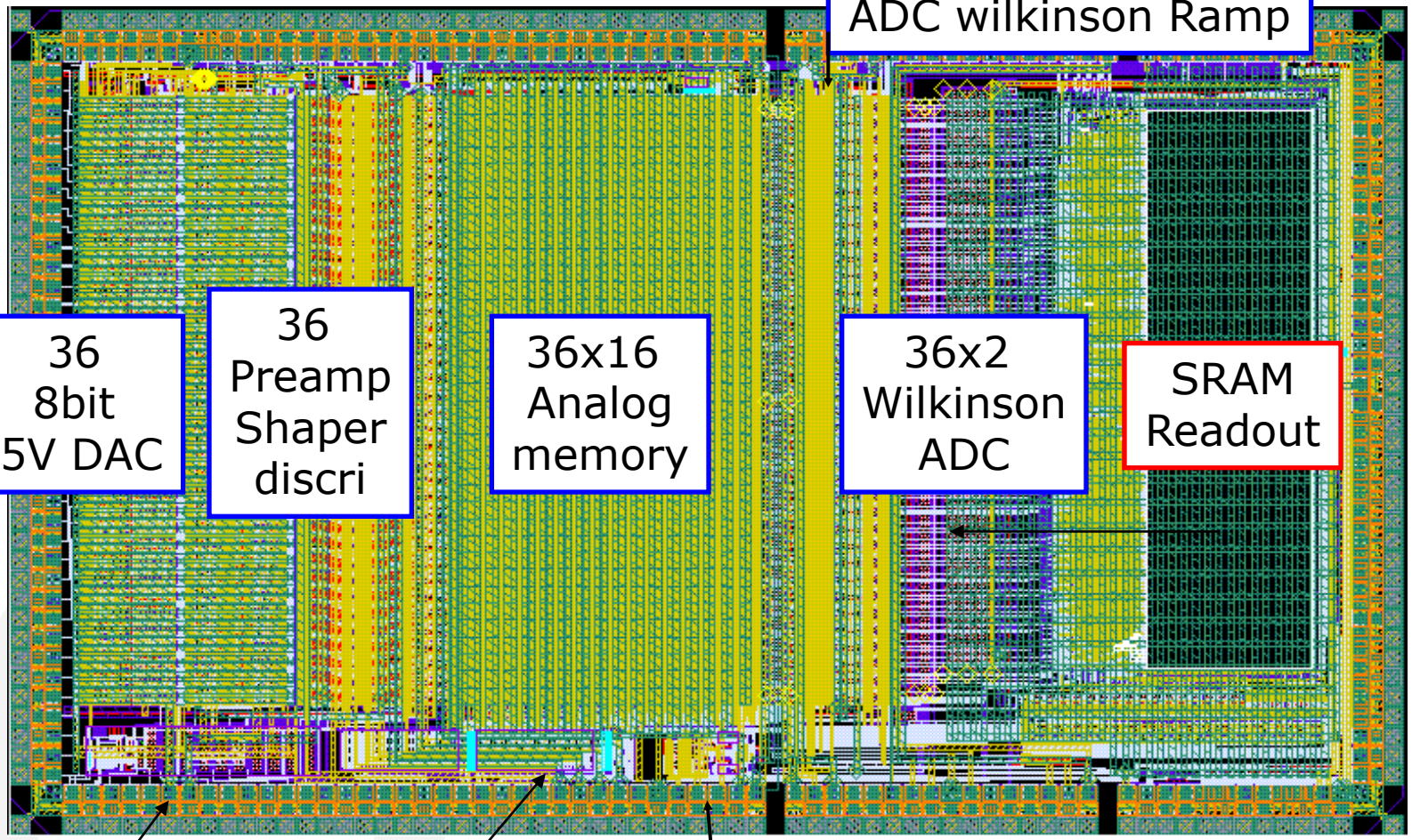
Second generation chip for SiPM

- SPIROC : Silicon Photomul. Integrated Readout Chip
  - 36 channels
  - Charge measurement
  - Time measurement
  - Autotrigger on MIP or spe
  - Sparsified readout compatible with EUDET 2nd generation DAQ
  - Chips daisy-chained
  - Pulsed power -> 25 µW/ch
- Fabricated in SiGe AMS 0.35 µm
  - Submitted in june 07
  - Chip area : 30 mm2



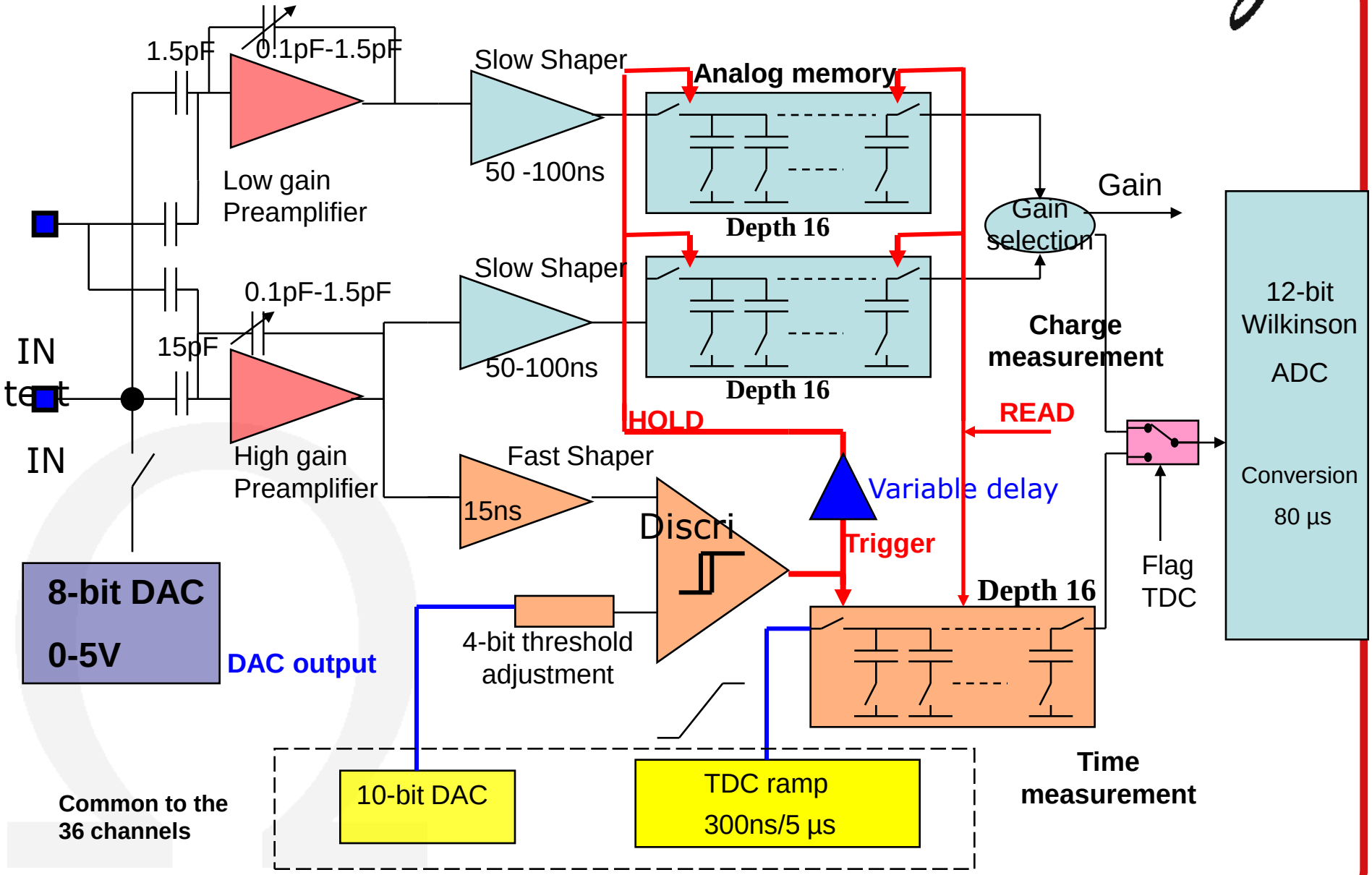


SPIROC layout



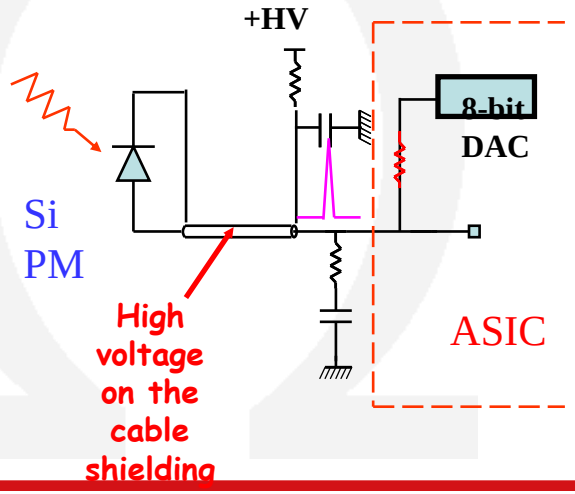
Fabricated in SiGe AMS 0.35 µm
Submitted in june 2007
Chip area : 30 mm² (4.2mm × 7.2mm)

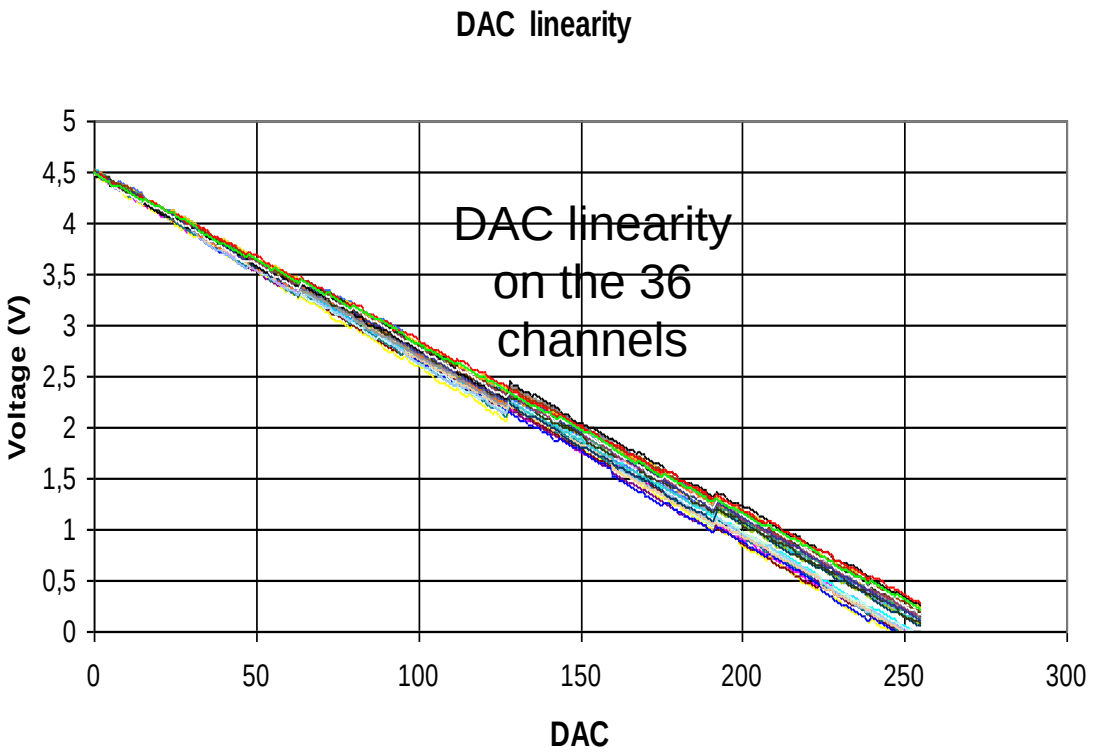
SPIROC : One channel schematic

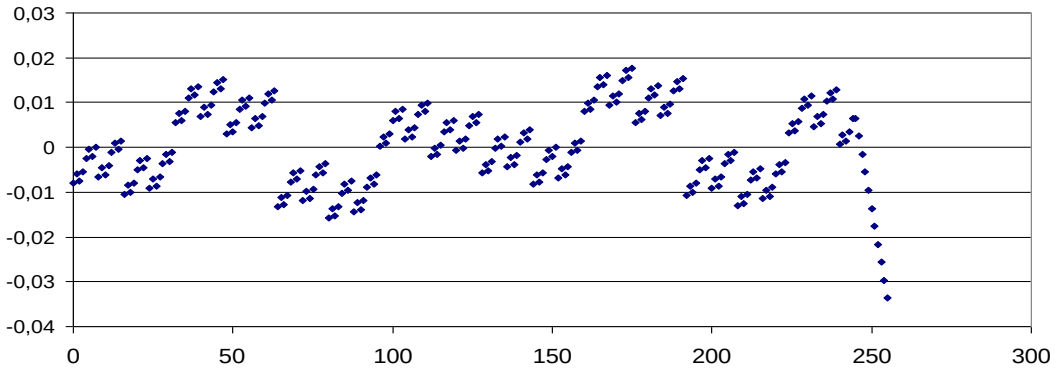


Input DAC

- **Input DAC to optimize SiPM bias voltage**
- **8-bit DAC, 5V range**
- **LSB=20mV**
- **36 DAC : one per channel**
- **Ultra low power (1µW) : no power pulsing**
- **Can sink 10 µA leakage current**
- **Linearity : ± 2%**
- **DAC uniformity between the 36 channels : ~3%**



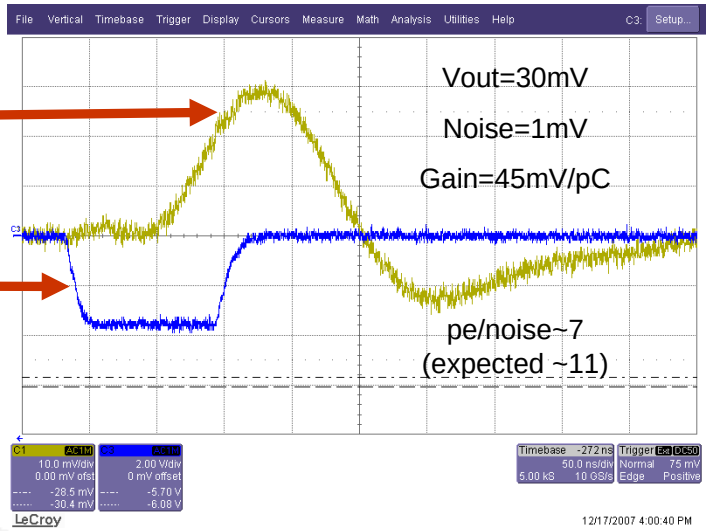


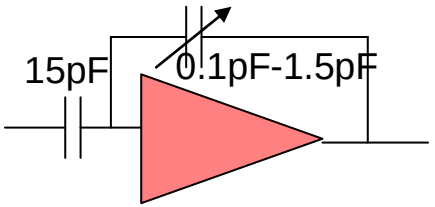


Charge measurement

High gain channel output

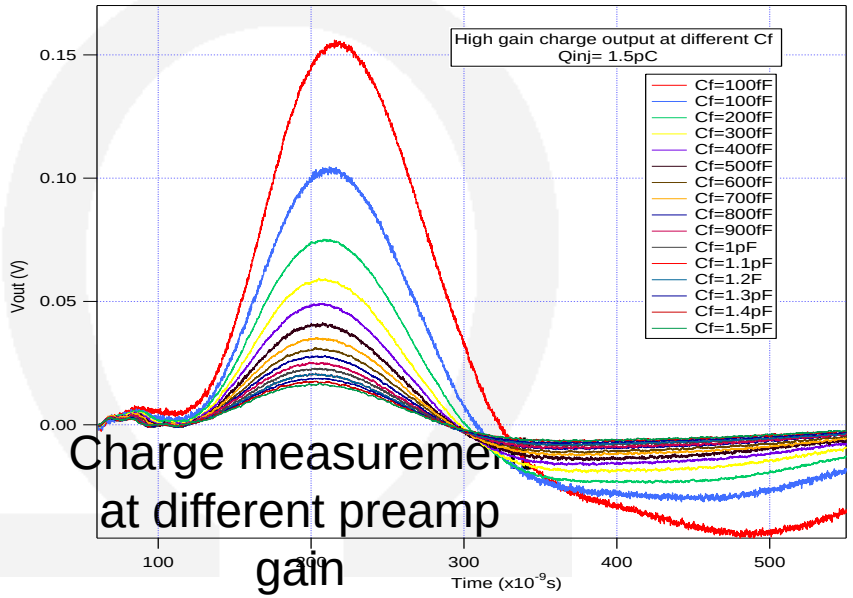
680fC (~4 pe @SiPM gain=10^6) in SPIROC

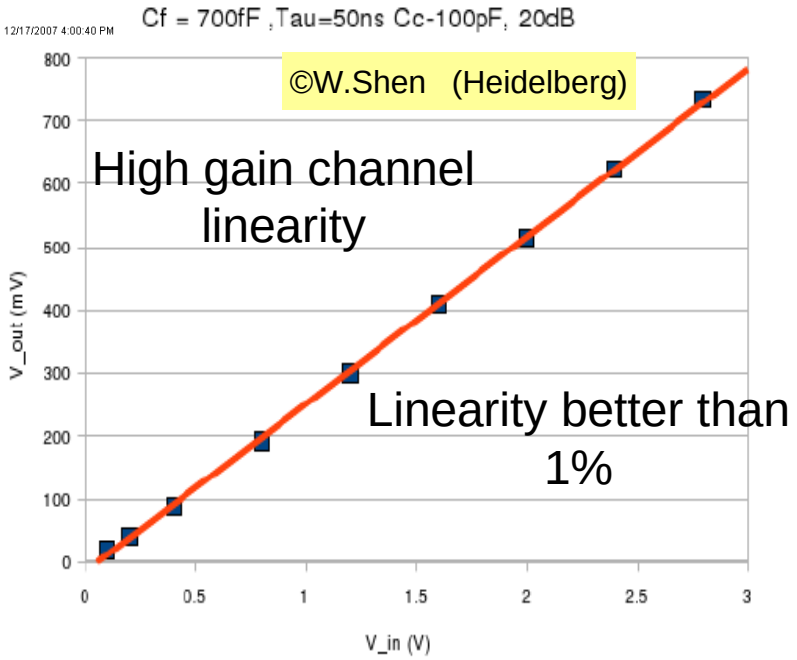




Low noise charge preamplifier capacitively coupled = voltage preamplifier

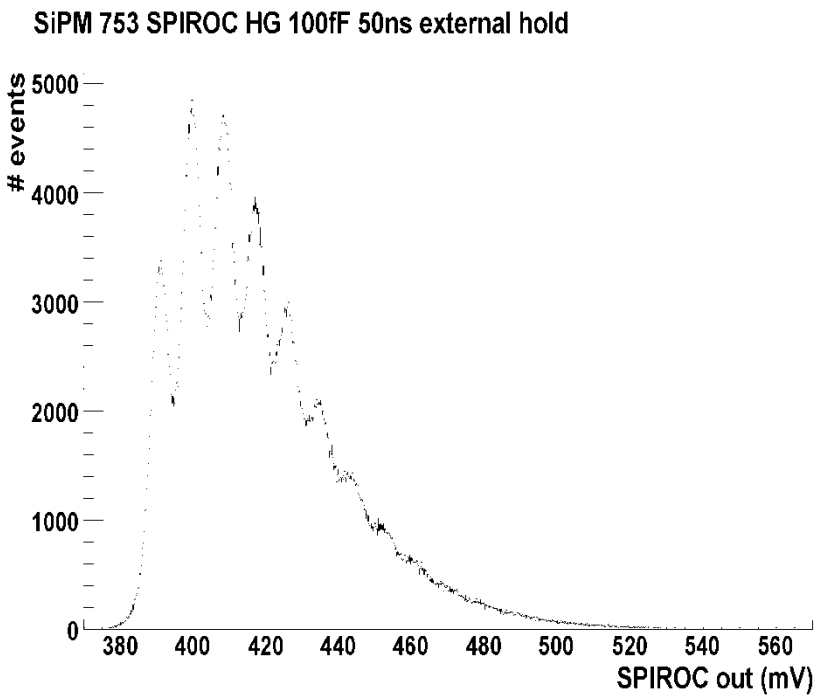
Preamp noise : 1.4 nV/sqrt(Hz)

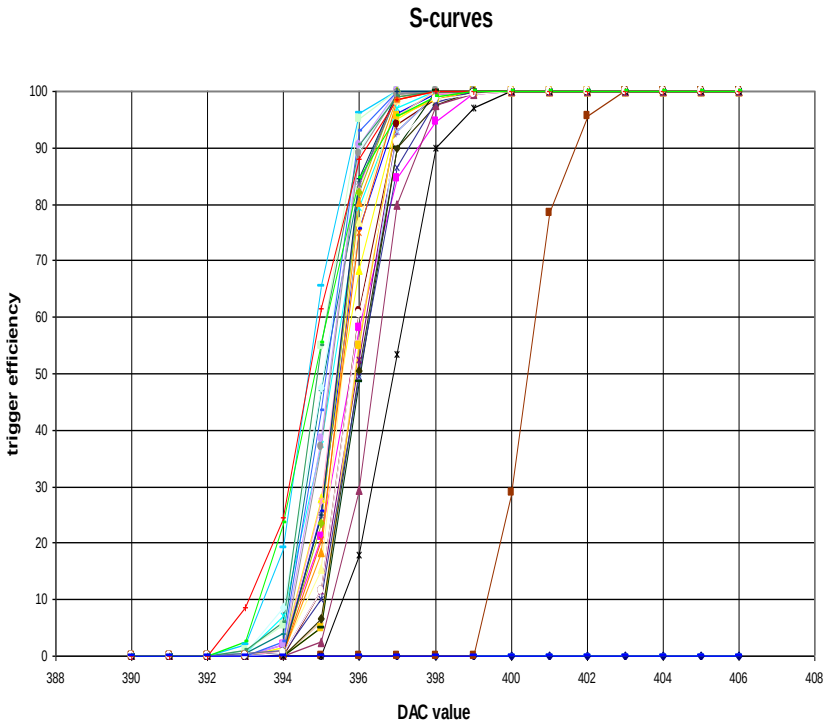




SPIROC performance

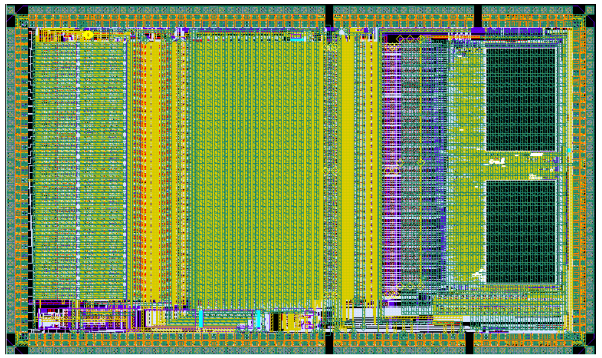
- Good analog performance
  - Single photo-electron/noise = 8
  - Auto-trigger with good uniformity
  - Complex chip : many more measurements needed





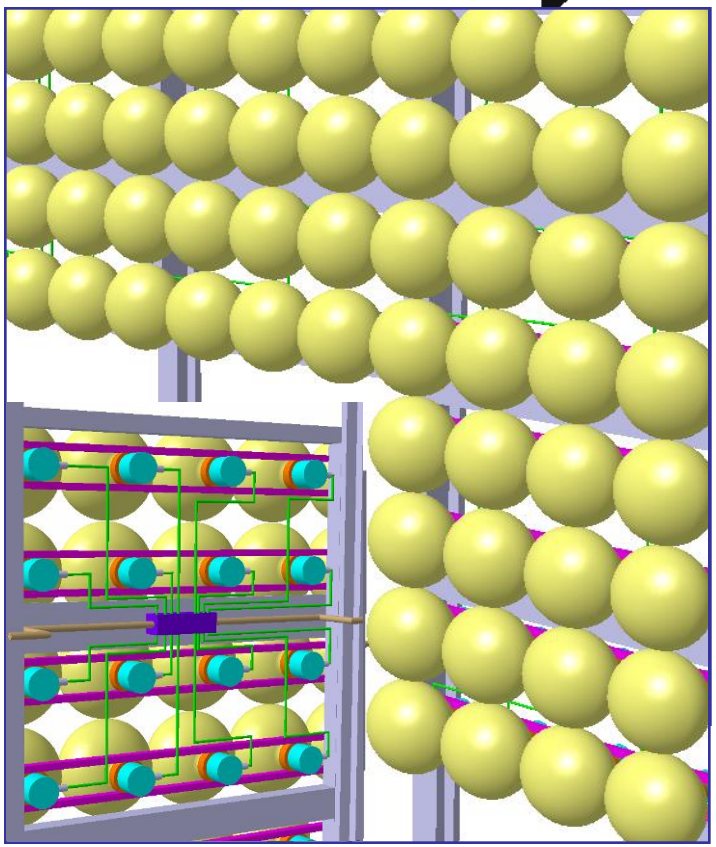
SPIROC main features

- Internal input 8-bit DAC (0-5V) for individual SiPM gain adjustment
- Energy measurement : 14 bits
  - 2 gains (1-10) + 12 bit ADC 1 pe → 2000 pe
  - Variable shaping time from 50ns to 100ns
  - pe/noise ratio : 11
- Auto-trigger on 1/3 pe (50fC)
  - pe/noise ratio on trigger channel : 24
  - Fast shaper : ~10ns
  - Auto-Trigger on ½ pe
- Time measurement :
  - 12-bit Bunch Crossing ID
  - 12 bit TDC step~100 ps
- Analog memory for time and charge measurement : depth = 16
- Low consumption : ~25µW per channel (in power pulsing mode)
- Individually addressable calibration injection capacitance
- Embedded bandgap for voltage references
- Embedded 10 bit DAC for trigger threshold and gain selection
- Multiplexed analog output for physics prototype DAQ
- 4k internal memory and Daisy chain readout

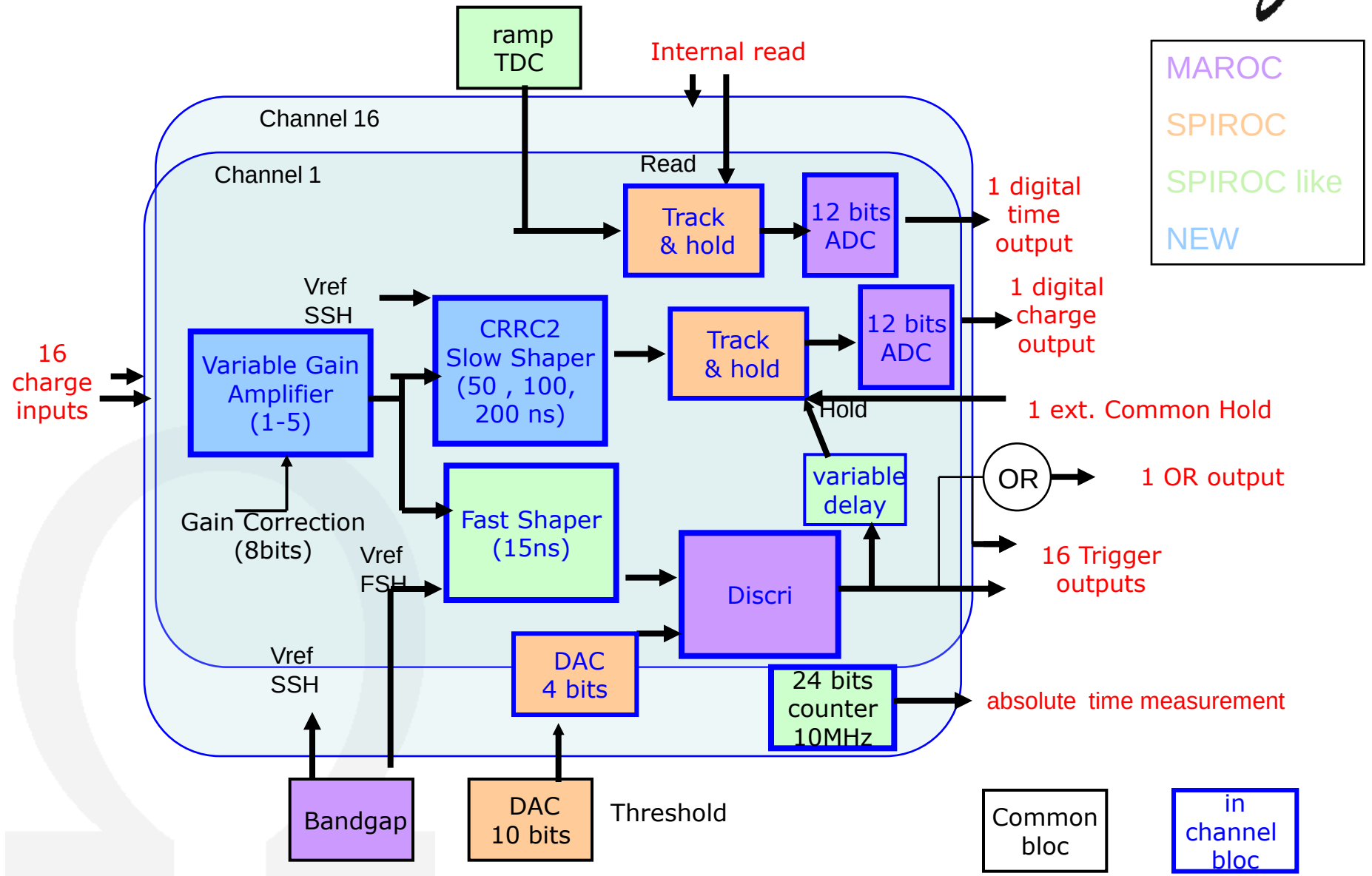


PMm^2 : large photodection area

- **"PMm2" (2006 – 2009), funded by the ANR** : LAL, IPNO, LAPP, Photonis
- Replace large PMTs (20") by groups of smaller ones (12")
  - central 16ch ASIC (PaRISROC)
  - 12 bit charge + 12 bit time
  - water-tight, common High Voltage
  - Only one wire out (DATA + VCC)
  - Target low cost
  - Reuse many parts from MAROC & SPIROC
- Application : large water Cerenkov neutrino
  - 1ns time resolution
  - High granularity
  - scalability

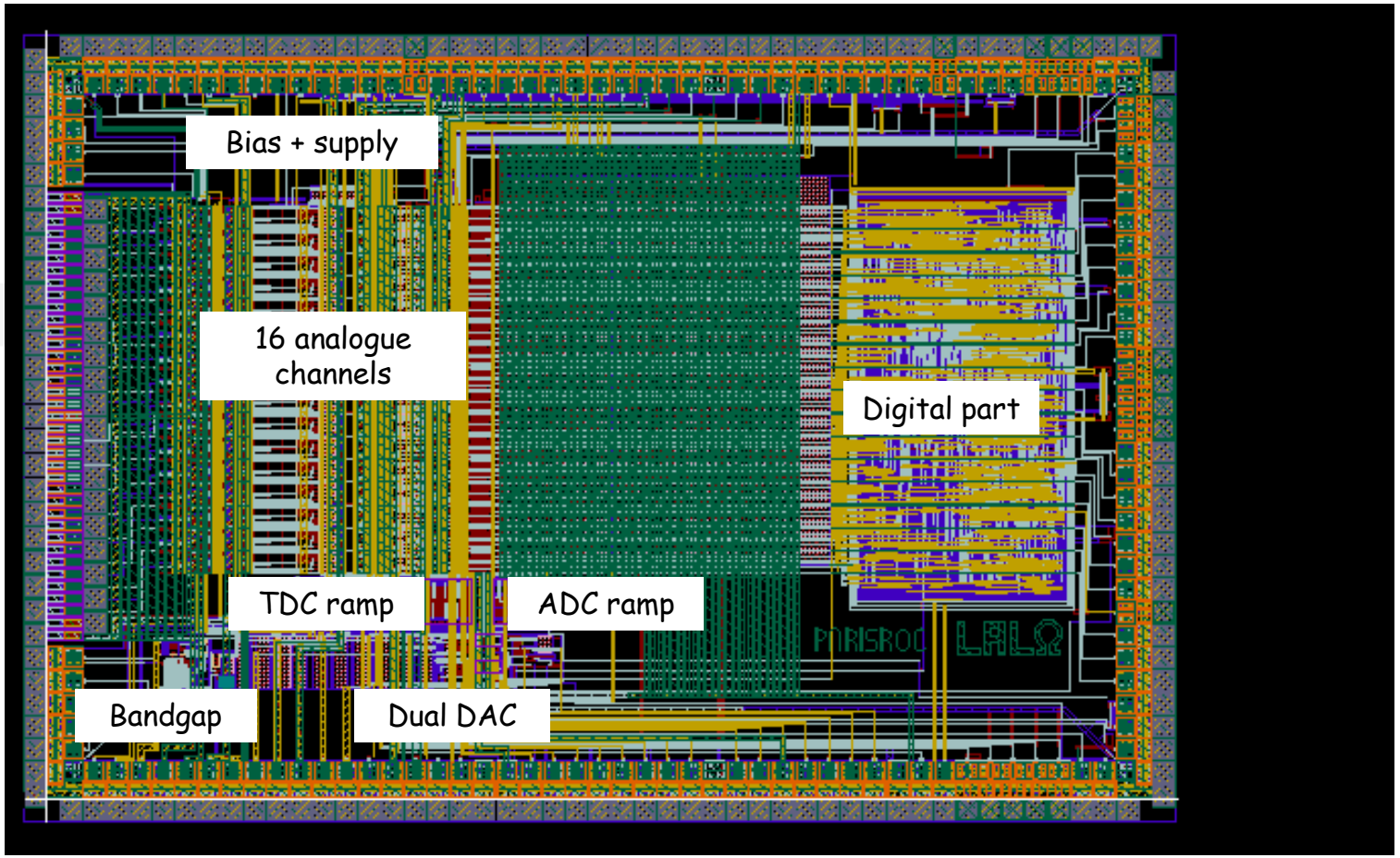


PMm² ASIC Architecture (Analog part)



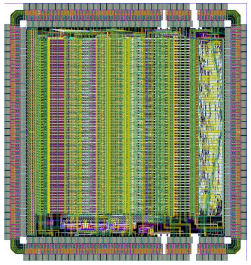
PArISROC specifications

- 16 channels read out chip for Photomultiplier array
- SiGe 0.35 µm technology. Chip submitted jun 08

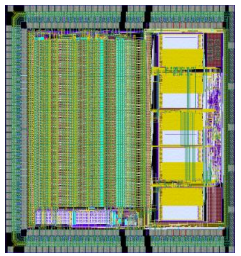


Orsay Micro-Electronics Groups Associated

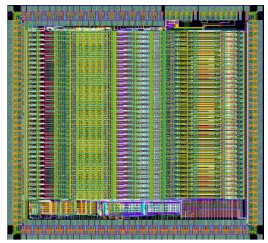
- A strong team of 10 ASIC designers…
  - around 20% of IN2P3 designers
  - A team with critical mass : pole created in 2007 = OMEGA
  - Expertise in low noise, low power high level of integration ASICs
  - 2 designers/ project
  - 2 projects/designer
  - Regular design meetings



MAROC 2



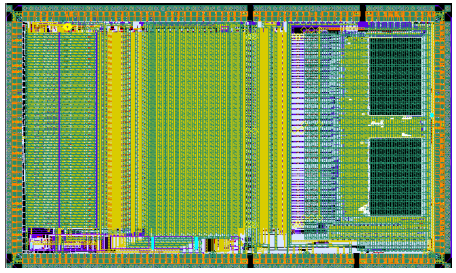
HARDROC



SKIROC

- Within the LAL Electr. Depart. (50 p.)
  (Support for tests, mesurements, PCBs…)
- Collaboration with IPNO, LLR, CSNSM

- A steady production
  - A strong on-going R&D
  - Building blocks SiGe 0.35µm



SPIROC

More information

- OMEGA

  Université Paris Sud Orsay
  LAL - Building 200
  91898 Orsay Cedex - FRANCE

- OMEGA Web Site:

  http://omega.in2p3.fr

- Contact:

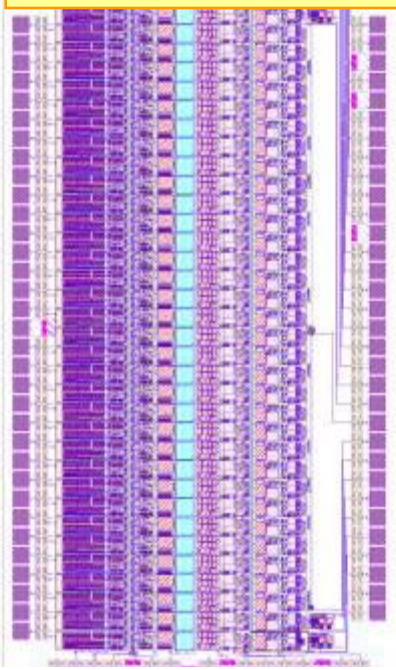
  Christophe de La Taille: taille@lal.in2p3.fr

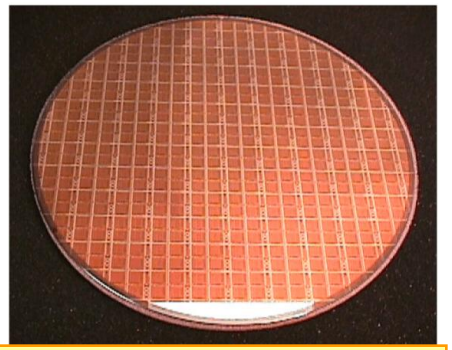
(R)evolution of analog electronics

- ASICs : Application Specific Integrated Circuits
  - Access to foundries through multiproject runs (MPW)
  - Reduced development costs : 600-2000 €/mm^2 compared to dedicated runs (100-2000 k€)
  - Full custom layout, at transistor level
  - mostly CMOS & BiCMOS

- Very widespread in high Energy Physics
  - High level of integration, limited essentially by power dissipation and parasitic couplings (EMC)
  - Better performance : reduction of parasitics
  - Better reliability (less connections)
  - But longer developpement time

Layout 32ch ASIC

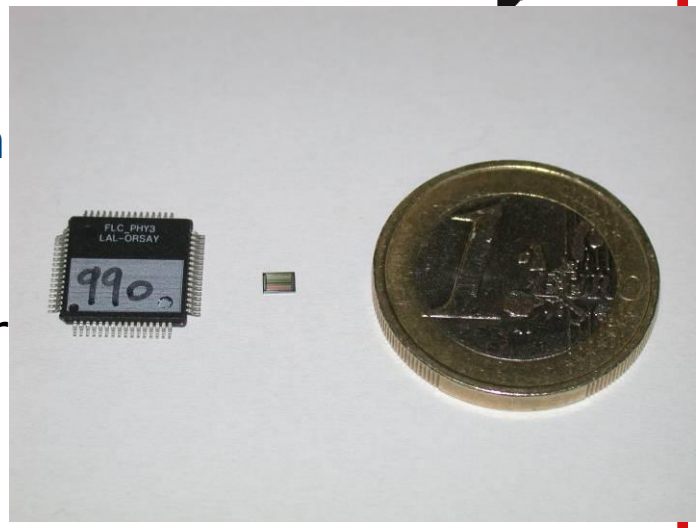




300 mm wafer (IBM)

Cost of ASICs

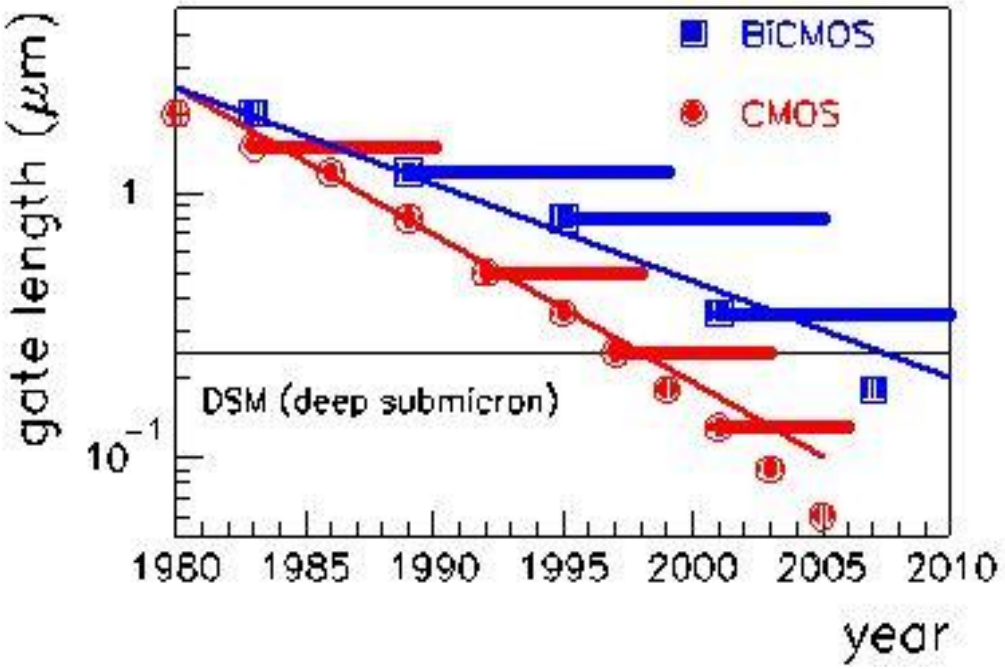
- MPW (multi-project wafers)
  - CMOS 0.35µm (AMS) : 650 €/mm2
  - BiCMOS SiGe 0.35 µm (AMS) : 900 €/mm
  - CMOS 0.13µ (STm) : 2500 €/mm2
  - CMOS 90 nm (STm) : 5000 €/mm2
  - Usually a few 10 to 100 pieces in a MPW r



- Production runs
  - Masks : 91 k€ (CMOS 0.35µm)
  - 8" wafers : 4 k€, useful area : 25 000 mm2 = several thousands of chips
- Packaging
  - Ceramic : 20-30€/chip
  - Plastic : 2k€ + 1-2 €/chip
- Example : chip 10mm2 16 channels
  - 100 chips (MPW) : 120€/chip, 7€/channel
  - 10 000 chips (4wafers) : 12€/chip < 1€/channel

Evolution of CMOS technologies (2)

- Differences between analog/mixed signall and digital technologies
  - Very fast evolution of digital technologies (faster design migration)
  - More « perene » analog technologies (SiGe, BiCMOS…) (driven by mobile telecom and automotive)



- low voltage