PANDA DAQ and FEE

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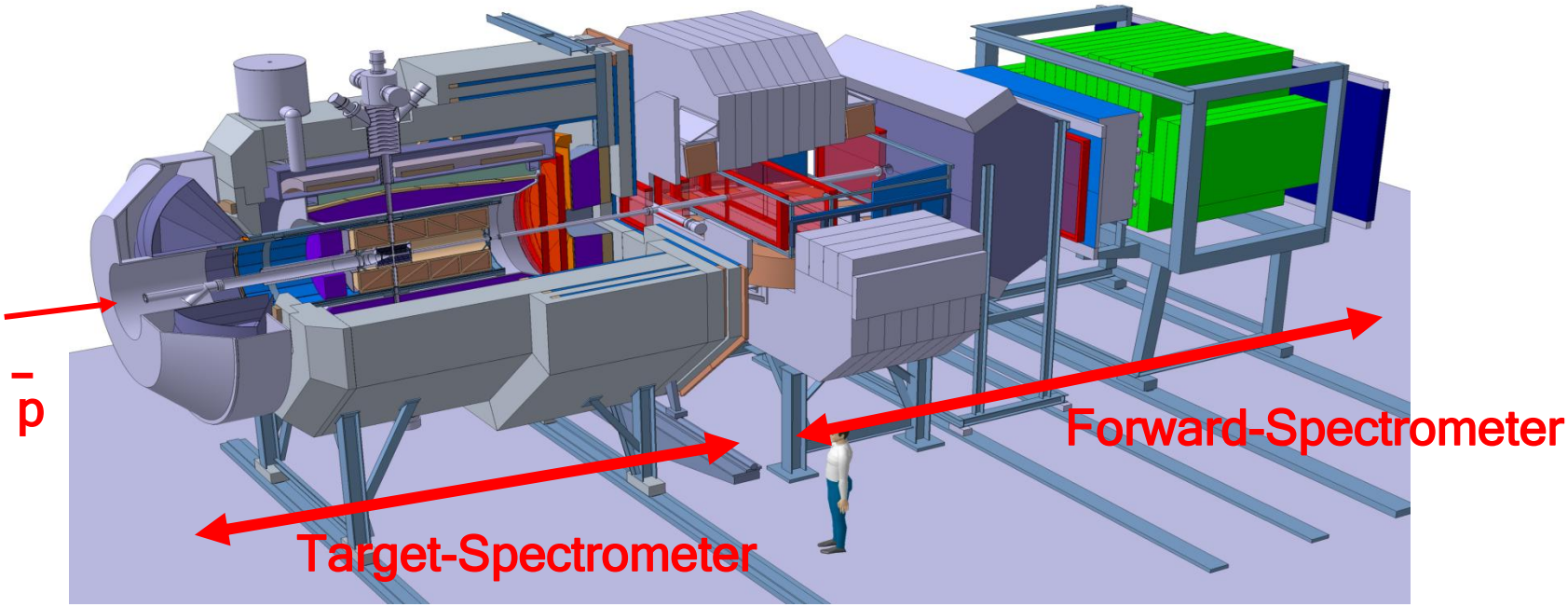
Talk overview

- PANDA experiment
- Trigger less FEE & DAQ
- PANDA detectors and data rates
- FE electronics
- TDC: GET4 and HPTDC
- DAQ architecture
- SODA time distribution system

PANDA experiment

- Physics: Strong interaction studies with antiprotons
- Continuous antiproton beam of 10^11 /s
- Fixed target : pellets of frozen hydrogen or gas jet, nuclear targets
- 2 10^7 annihilations/s
- Two stage spectrometer
- DAQ: dead time less, trigger less

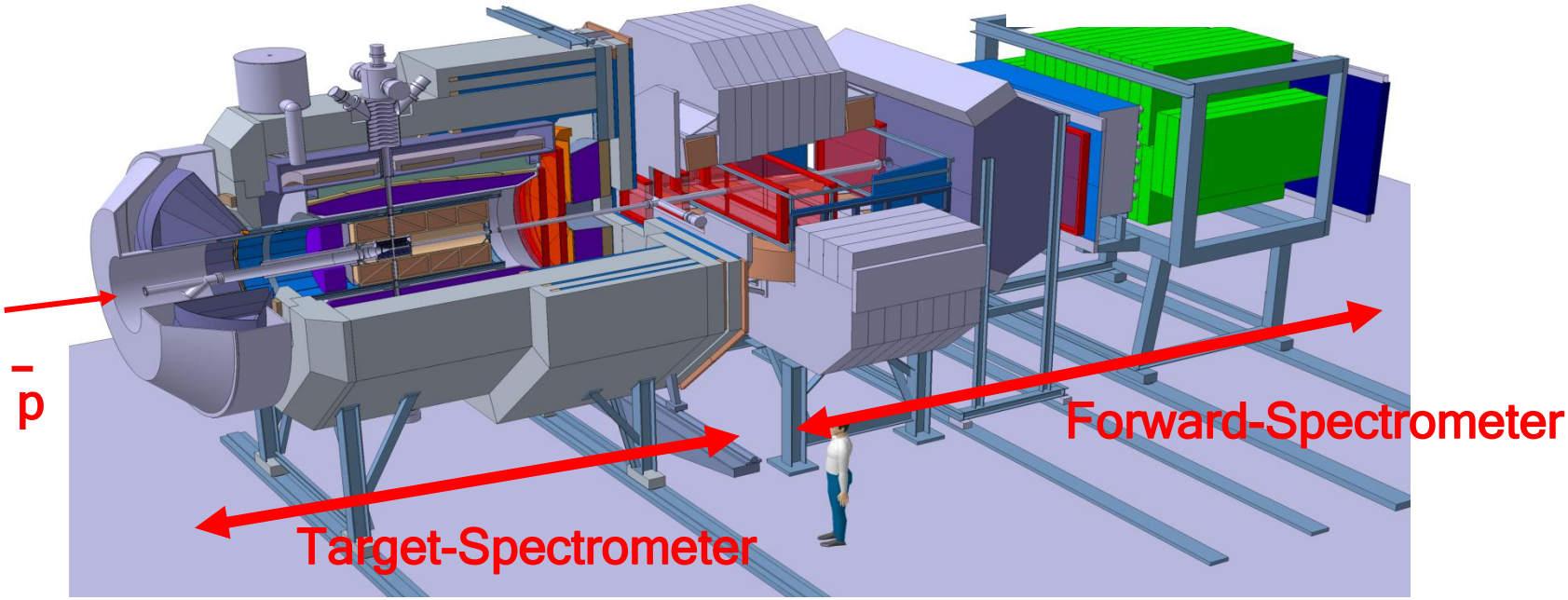


PANDA experimer

- Physics: Strong interaction studies with antiproto
- Continuous antiproton beam of 10^11 /s
- Fixed target : pellets of frozen hydrogen or gas je
- 2 10^7 annihilations/s
- Commissioning 2014 ?
- DAQ: dead time less & trigger less

Detectors:

- Silicon Pixel & Strip tracker
- Straw trackers
- TPC tracker
- GEM tracker
- Electro-magnetic calorimeters
- Muon detectors
- DIRC detectors
- ToF

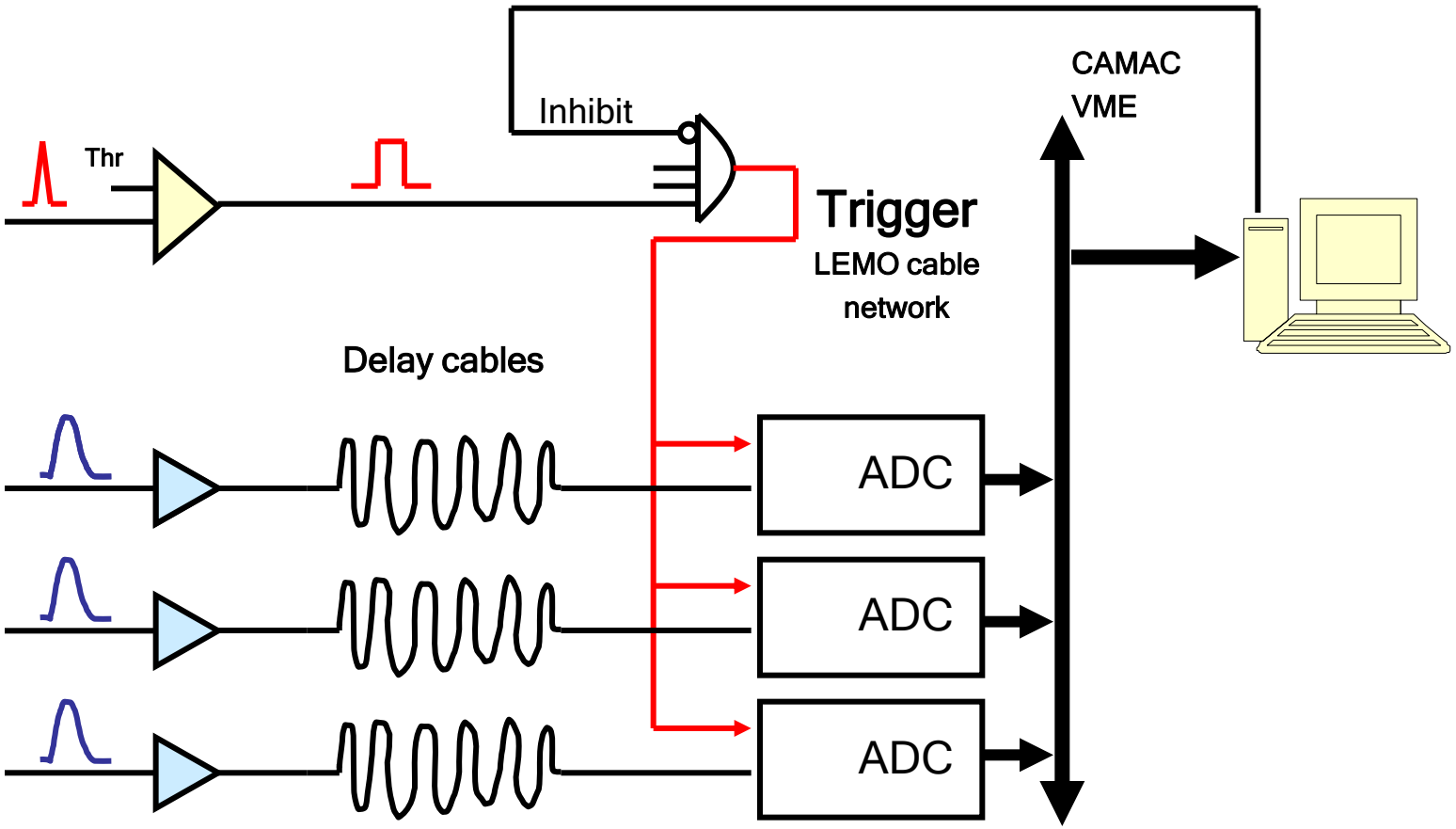


Motivation for TRIGGER less DAQ

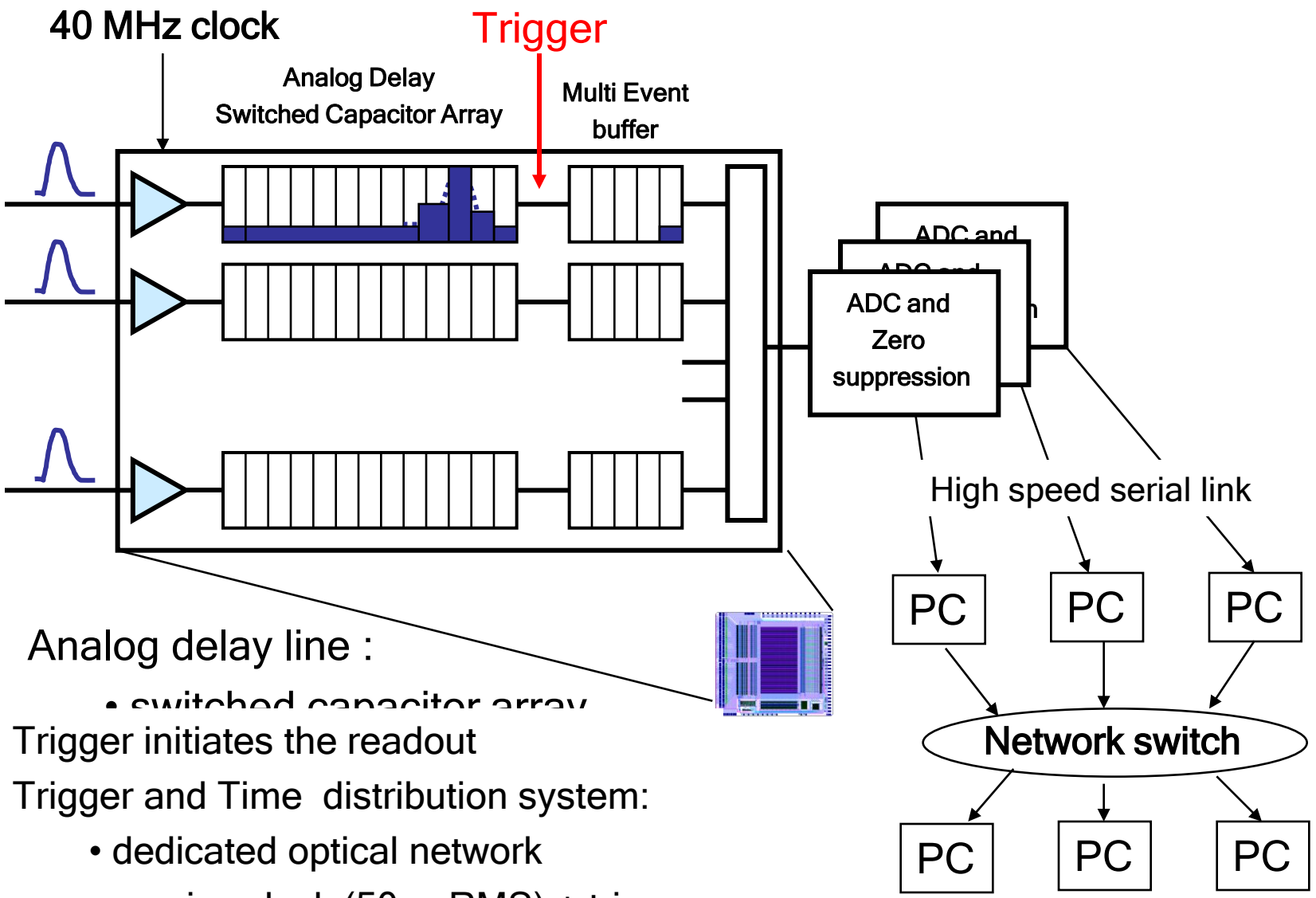
- Wide physics cases – different criteria for event selection
- Complicated event selection criteria
  - Identification of short lived particles - Impact Parameter
  - photon clusters in EMC with veto of charged particles in front e.g.η_c
  - Electron identification
  - Particle ID in MVD, TPC/Straw detectors (dE/dX)
  - Cherenkov PID
  - Λ reconstruction
  - Muon Identification
  - …

Almost every detector is needed for trigger decision

Classical DAQ



Trigger latency about 100 - 500 ns (40-130 m)



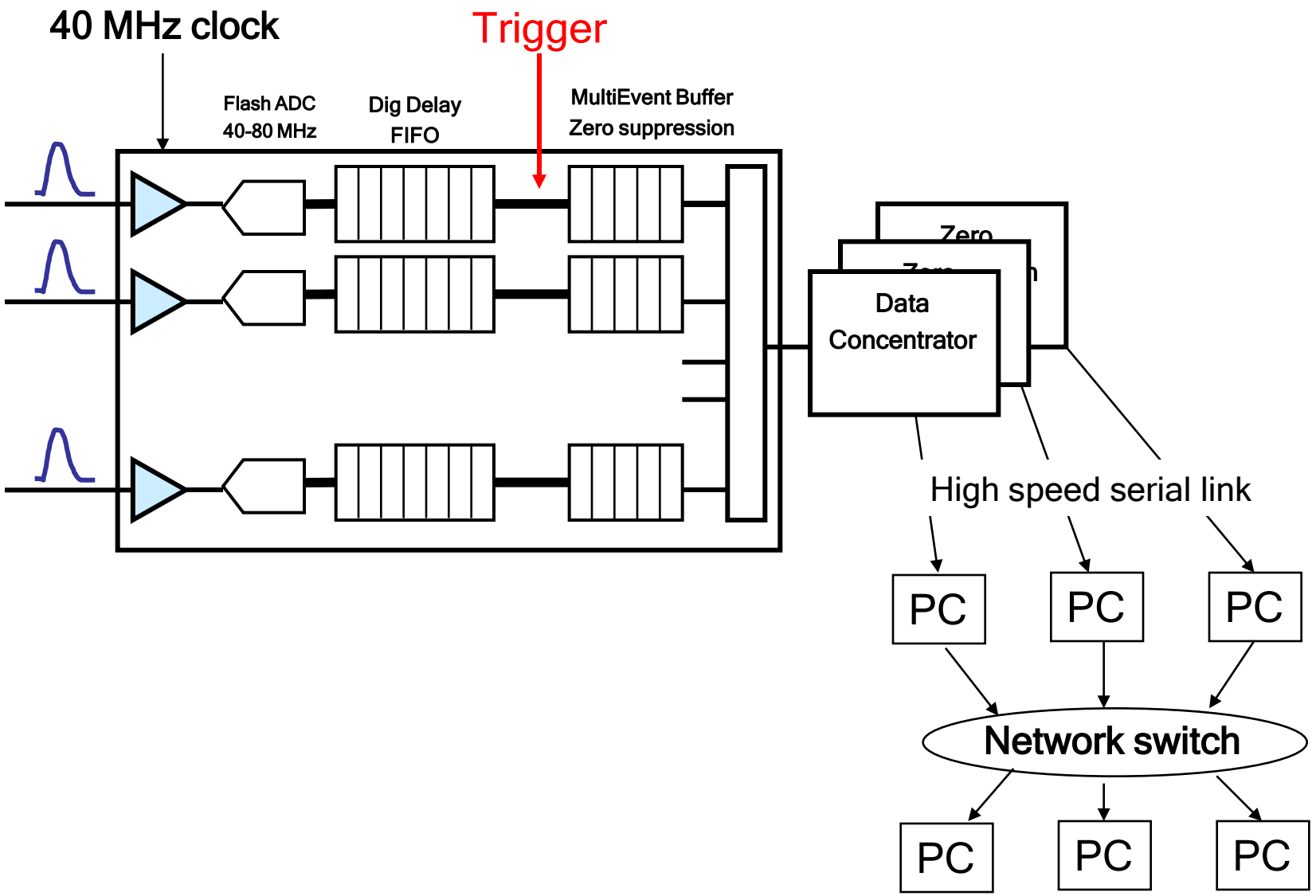
Analog delay line :

- switched capacitor array

Trigger initiates the readout

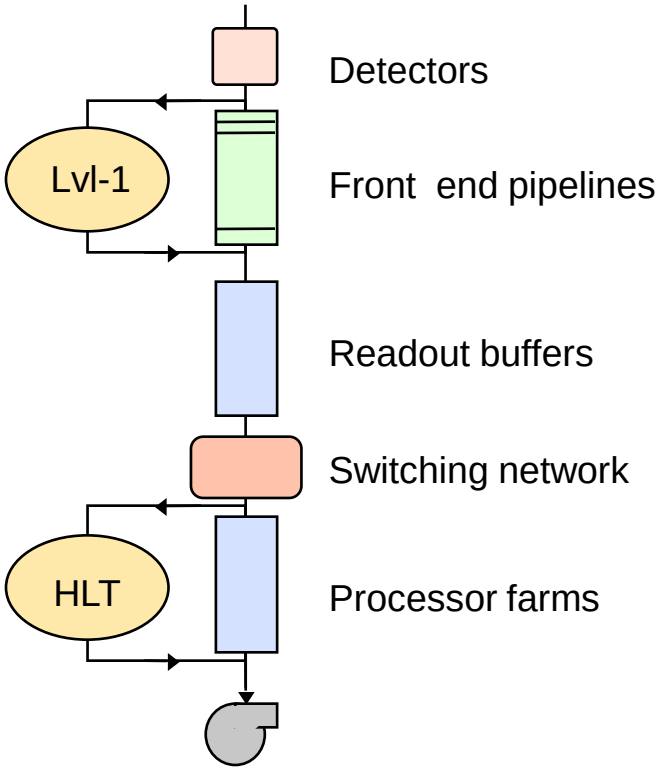
Trigger and Time distribution system:

- dedicated optical network
- precise clock (50ps RMS) + trigger
- more than 1000 destinations

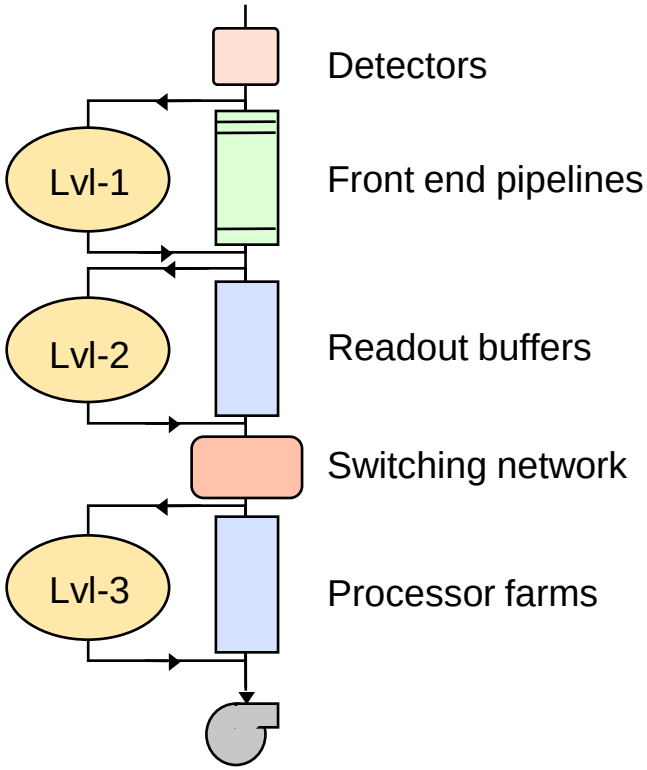

40 MHz clock
Trigger
Flash ADC
40-80 MHz
Dig Delay
FIFO
MultiEvent Buffer
Zero suppression
Zero
Data
Concentrator
High speed serial link
PC
PC
PC
Network switch
PC
PC
PC

DAQ architecture

CMS, COMPASS

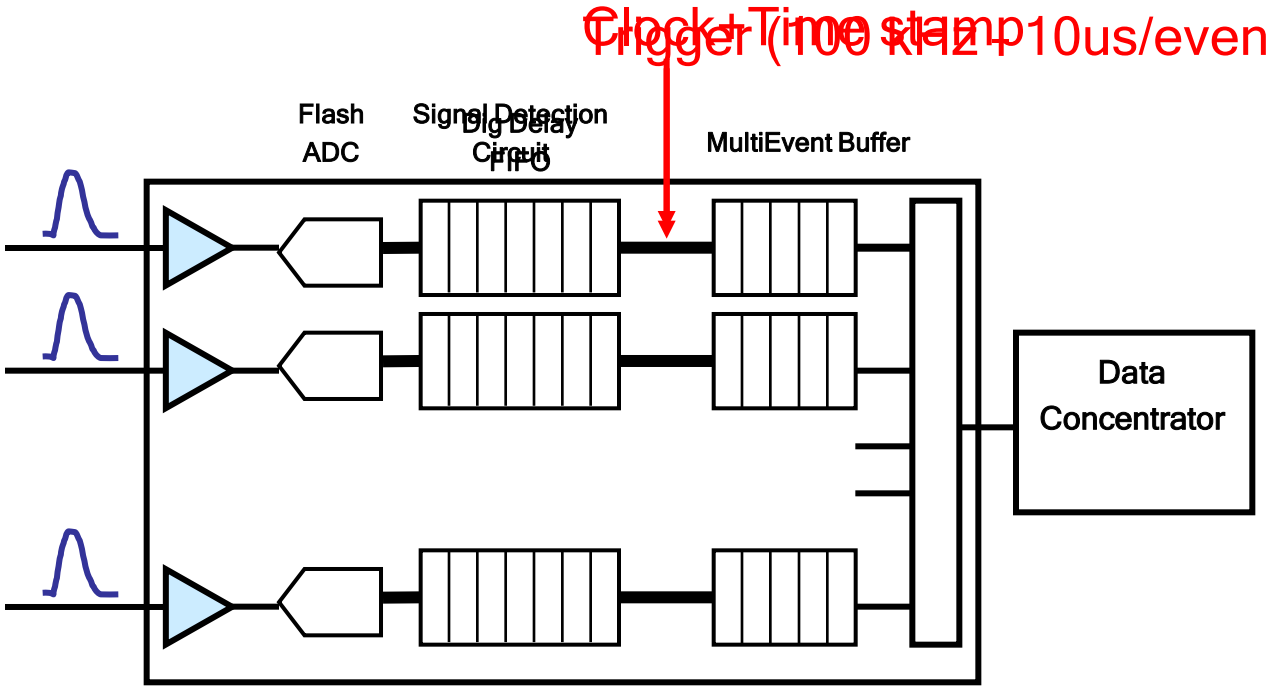


ATLAS, LHCb



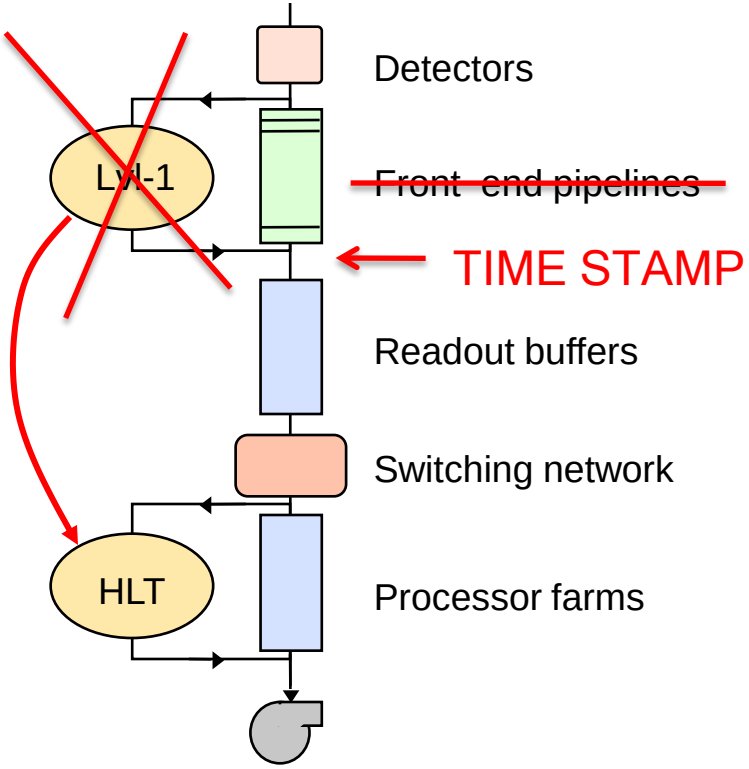
What does it mean “trigger less DAQ” ?

- No electrical or optical trigger signal
- Global clock
- Each channel detects signal -> time stamps it -> sends out



Trigger less DAQ

PANDA DAQ



Trigger logic becomes
a part of High Level Trigger

Drawing from Alexander Oh, CERN

Motivation for trigger less readout

Other reasons:

- Technologically Feasible
- Trigger => online data processors
- Online software ⇔ Offline software

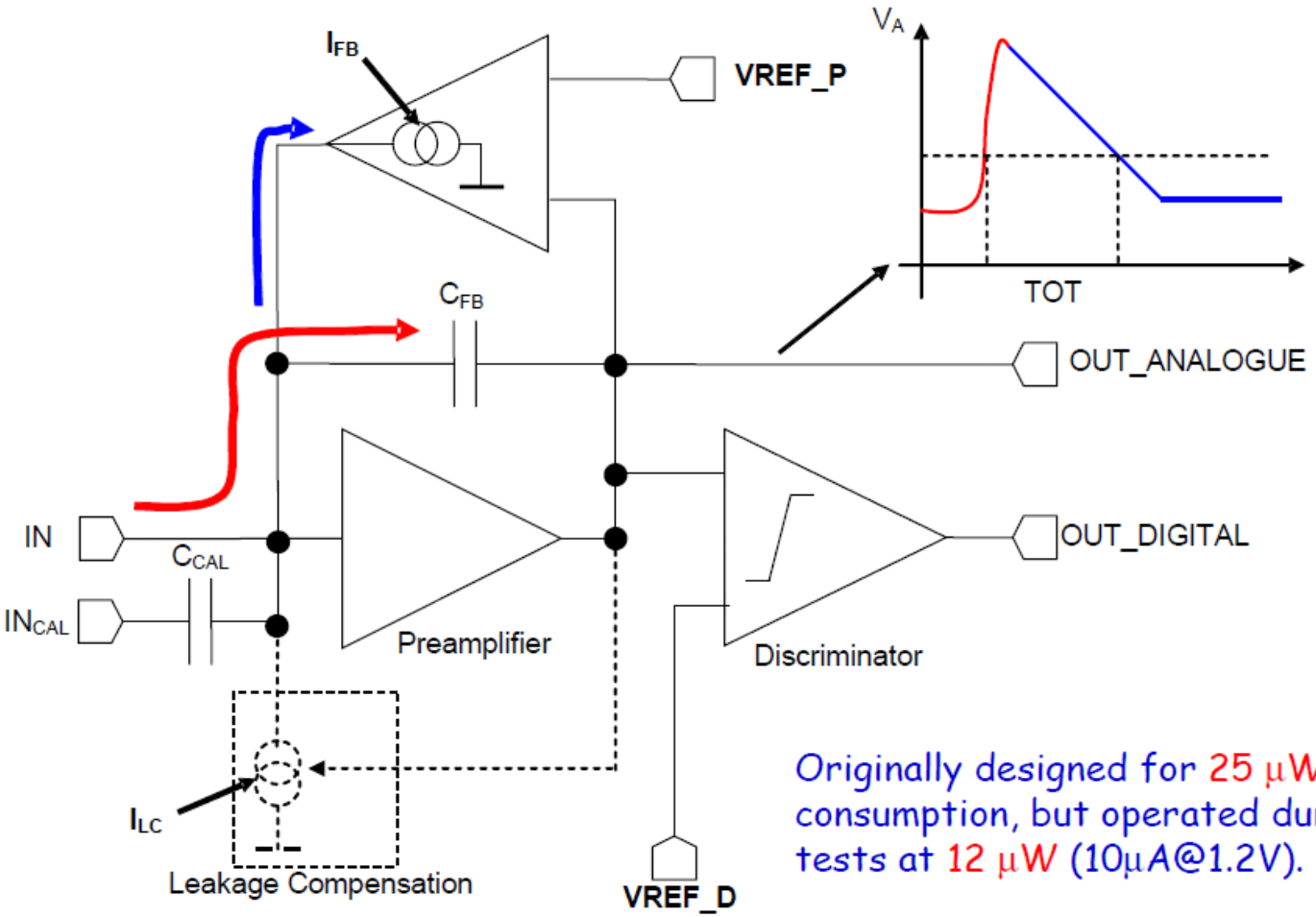
Trigger less FEE => Logical step in development

But requires development of new ASICs

Front-end electronics

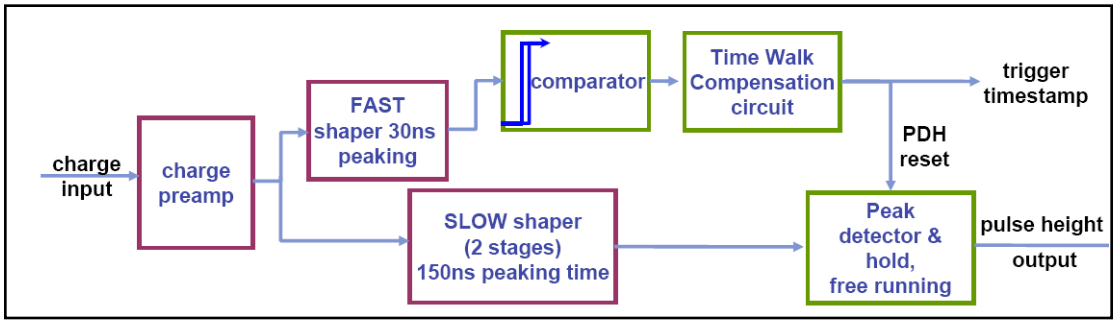
MicroVerexDetector		
Pixel	TOPIX(INFN)	6 ns , ToT
Strip	FAIR-XYTER (GSI)	3 ns , Peak Detector
TPC	FAIR-XYTER/SuperALTRO(CERN)	
Planar GEM	FAIR-XYTER	
StrawTubeTracker	Amp + discr + TDC	2 ns , ToT
MDC – Straw Tubes	Amp + discr + TDC	2 ns , ToT
Muon Chamber	Amp + discr + TDC	
EMC		
Barrel/Endcap	APFEL ASIC + Sampling ADC	pipeline ADC + FPGA
Forward	Sampling ADC	pipeline ADC + FPGA
DIRC		
barrel	Amp + discr + TDC	100 ps, ToT
ToP/FDD	Amp + discr + TDC	40 ps, ToT
TOF	TDC	

TOPIX



Originally designed for 25 μW of power consumption, but operated during the tests at 12 μW (10μA@1.2V).

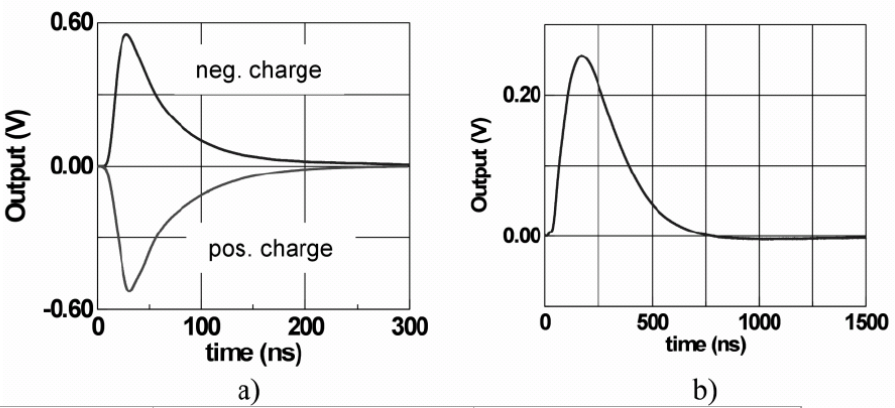
FAIR-XYTER chip development



Data driven/self triggering
12mW/channel

Status:

- first submission 2006
- circuit being revised
- next submission 2009



	FAST channel	SLOW channel
ENC	26.9 e/pF + 200 e	12.7 e/pF + 233 e
peaking time[a] (1% to 99%)	18.5 ns	139 ns

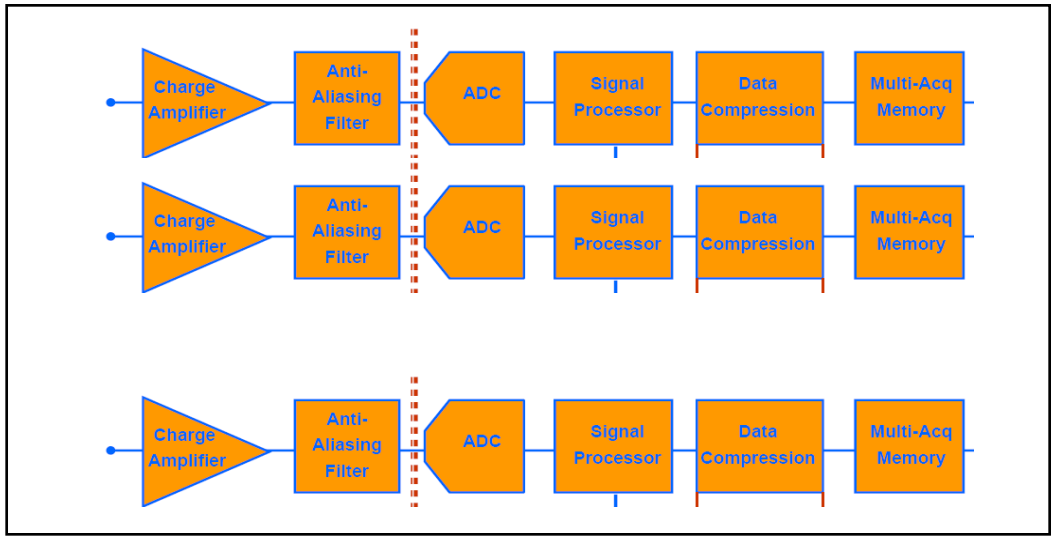
Engineered for
30 pF, giving 1000 e 600 e

SUPER ALTRO

CERN's ASIC for ILC TPC

- 12 bits
- 20 MSPS
- 32/64 channels/chip
- Interleave options
  - 40-80 MSPS
- Expected power consumption
  - 16mW/channel @20MHz
  - 32mW/channel @40MHz

- To be submitted in 2009



32/64 channels/chip, CMOS 0.130 µm

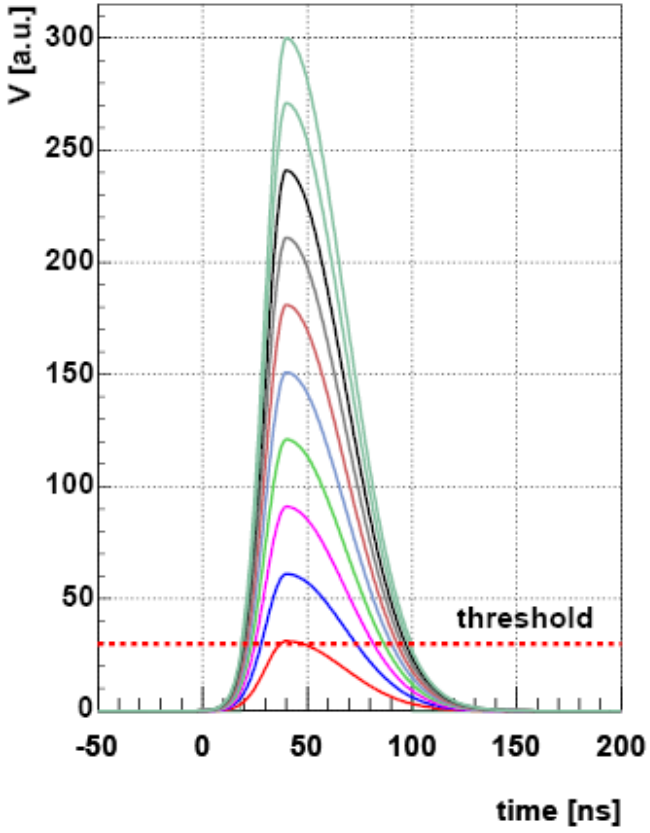
Straw FEE

Evaluation of Preamplifier – Shaper – Discriminator chips :

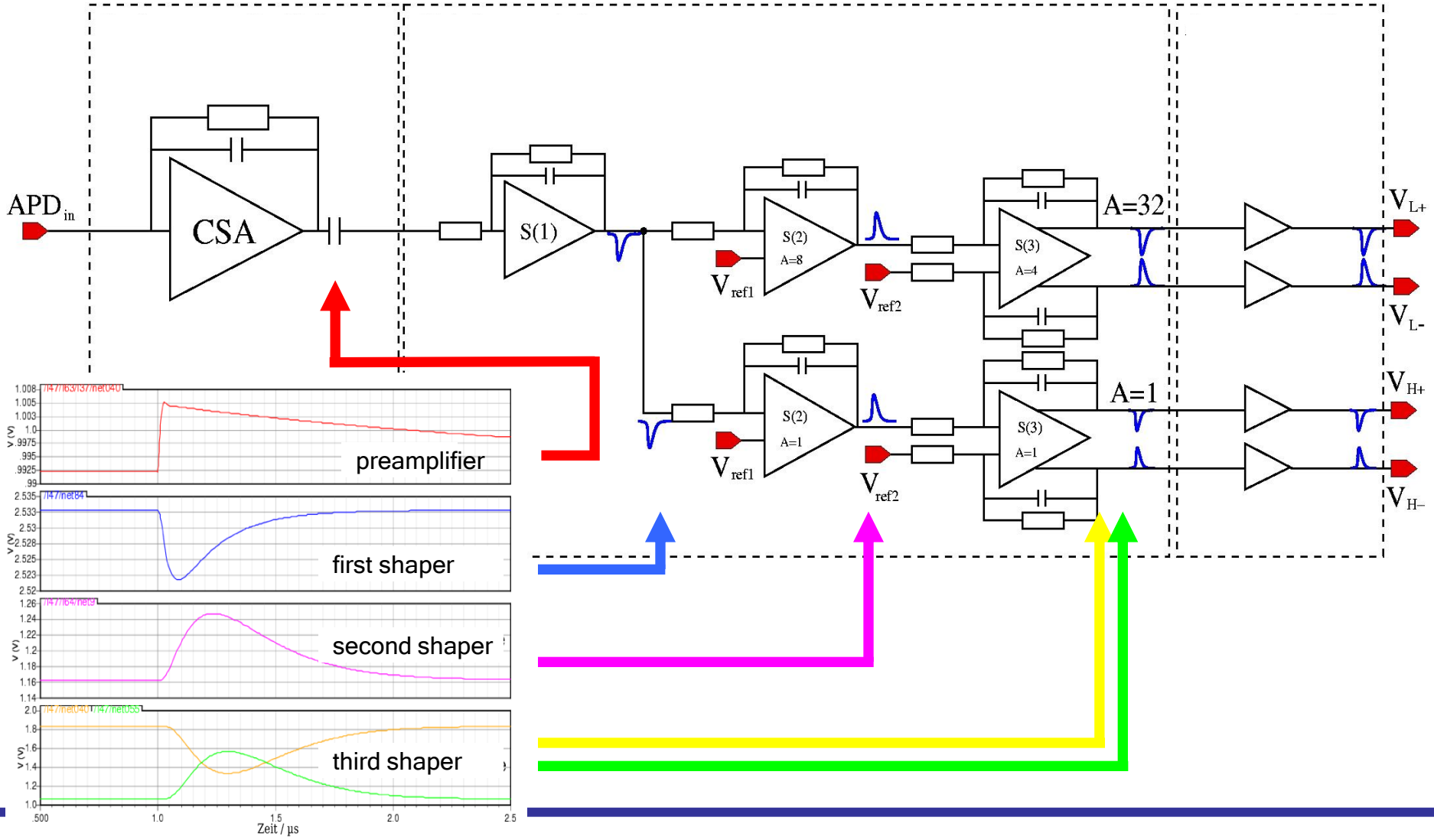
- CORIOCA
- CMP16
- ASDQ

Requirements:

- 2 ns resolution
- ToThreshold for dE/dX 5% resolution



APFEL ASIC, EMC APD readout



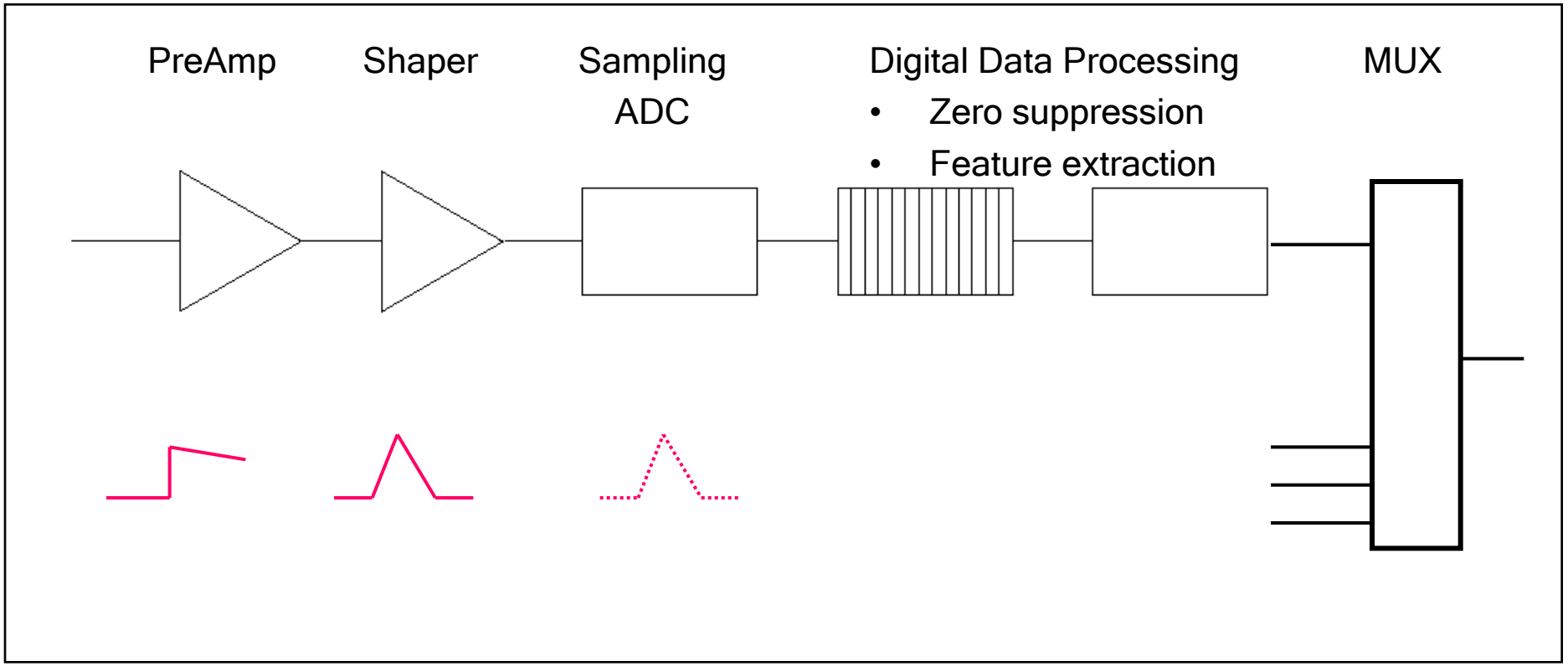
APFEL ASIC performance

	Requirements	Results @ T = - 20° C	Unit
Noise:	**4500**	**4456 ± 35** ✓	**e^-**
Max. input charge:	**7**	**7,84 ± 0,4** ✓	**pC**
Dyn. range:	**10000**	**10889 ± 251** ✓	**1**
Integration time:	**250**	**248 ± 3** ✓	**ns**
Event rate:	**350**	**500** ✓	**kHz**
Power consumption:	**60**	**52 ± 1** ✓	**mW/Channel**

Front-end electronics

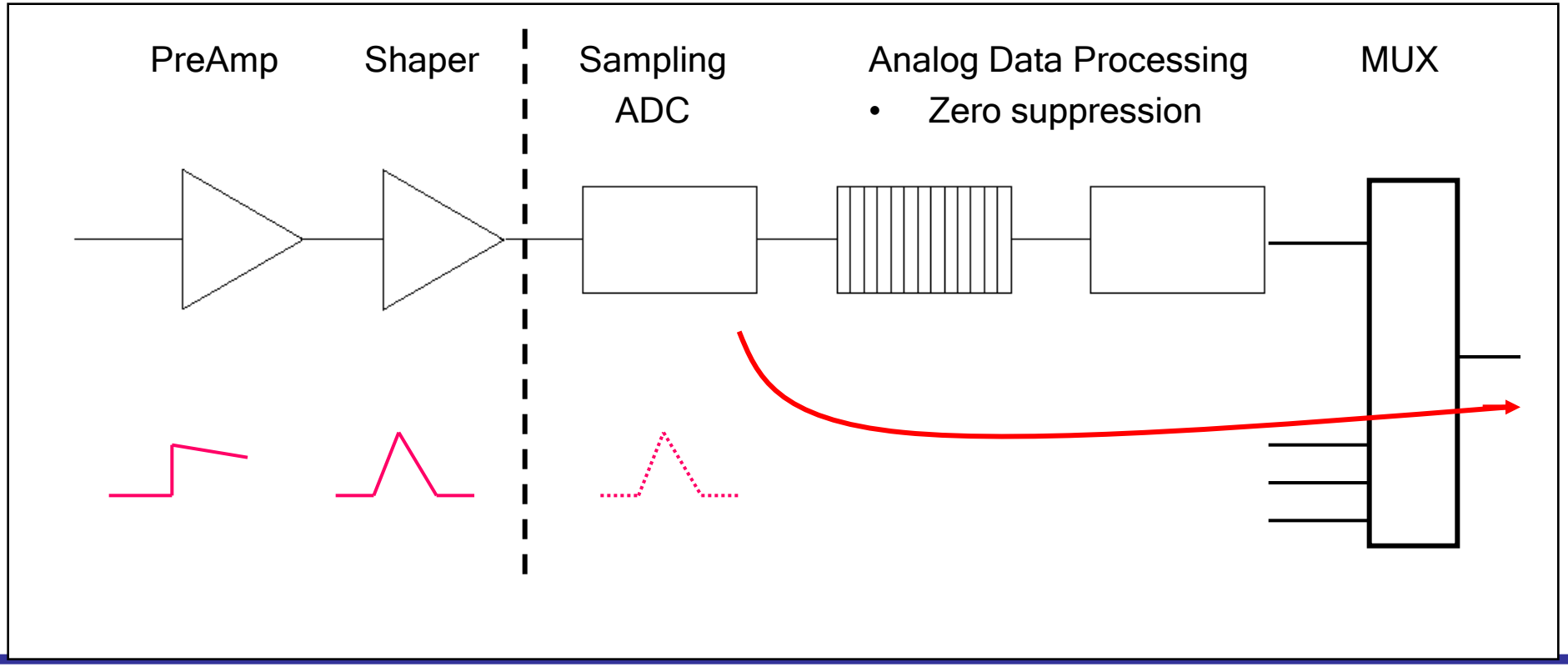
MicroVerexDetector		
Pixel	TOPIX(INFN)	6 ns , ToT
Strip	FAIR-XYTER (GSI)	3 ns , Peak Detector
TPC	FAIR-XYTER/SuperALTRO(CERN)	
Planar GEM	FAIR-XYTER	
StrawTubeTracker	Amp + discr + TDC	2 ns , ToT
MDC – Straw Tubes	Amp + discr + TDC	2 ns , ToT
Muon Chamber	Amp + discr + TDC	
EMC		
Barrel/Endcap	APFEL ASIC + Sampling ADC	pipeline ADC + FPGA
Forward	Sampling ADC	pipeline ADC + FPGA
DIRC		
barrel	Amp + discr + TDC	100 ps, ToT
ToP/FDD	Amp + discr + TDC	40 ps, ToT
TOF	TDC	

Best choice : sampling ADC readout

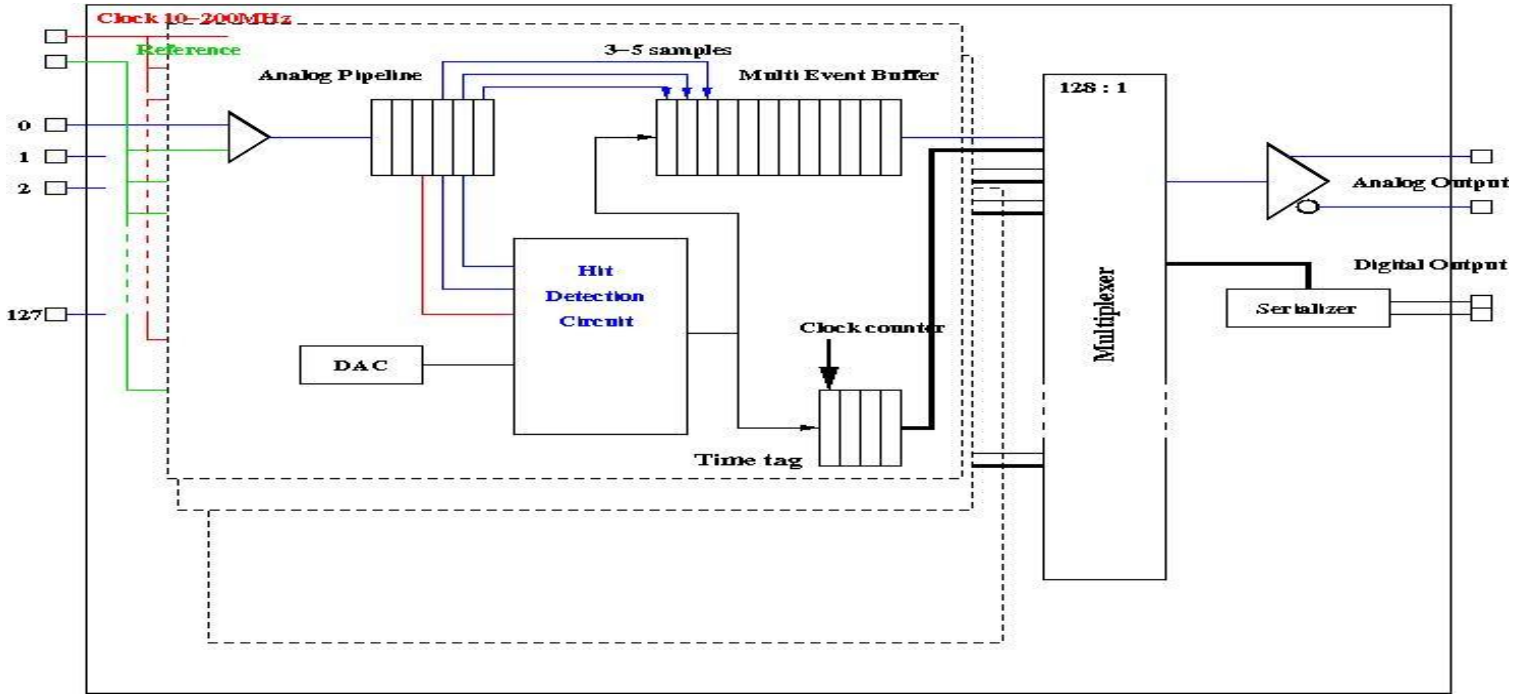


Another Idea

PANDA detectors hit rate < 200kHz
Use advantage of “low” detector occupancy => analog zero suppression + multiplexer



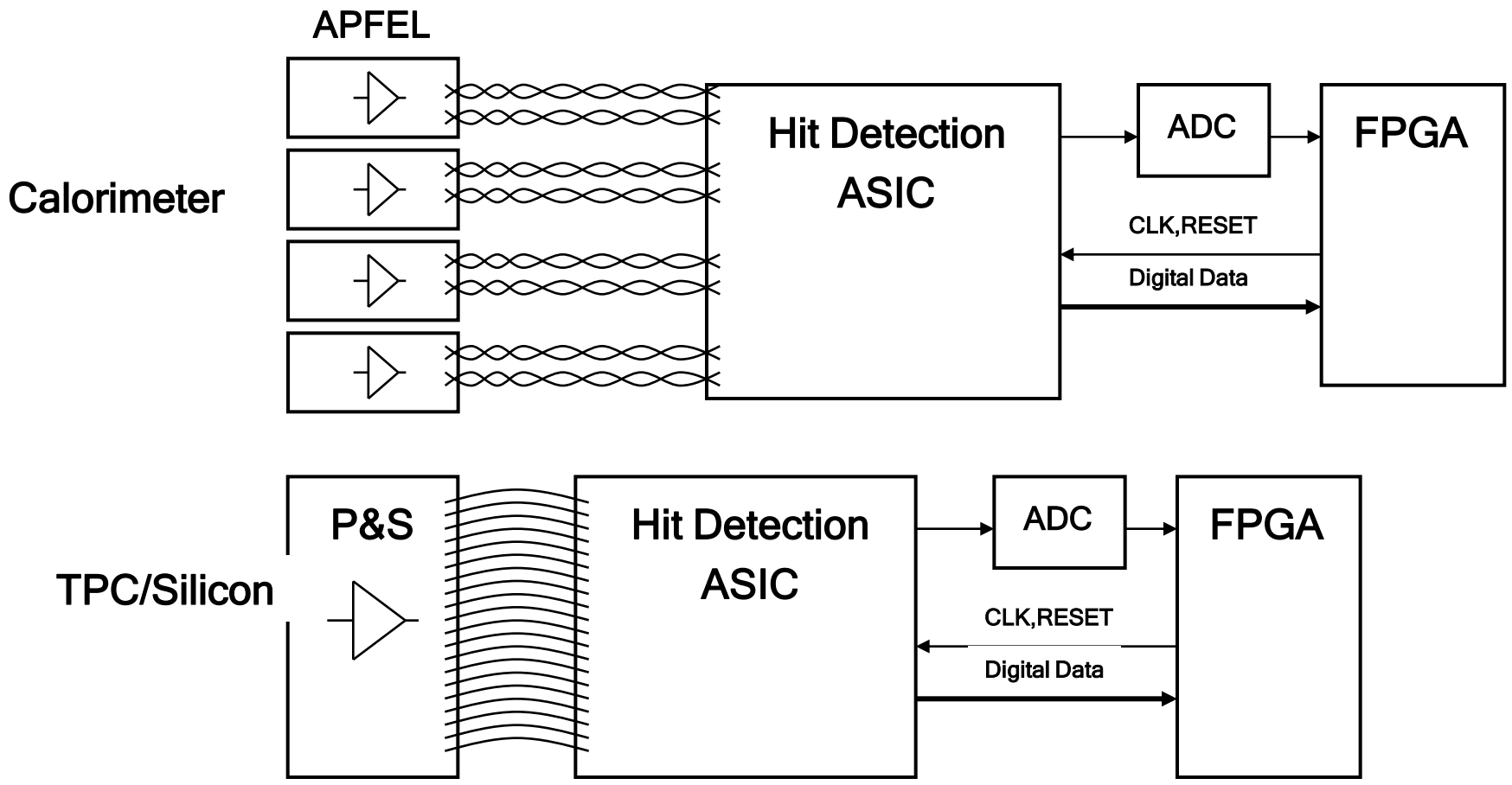
Hit detection ASIC



Functional description:

- Analog pipeline : switched cap.array runs @10-200MHz or higher
  - converts continuous analog signal into discrete time samples
- hit detection circuit
  - Programmable FIR filter: weights 3 samples and compares with threshold
- Feature extraction is done by external FPGA after digitization
- If runs at 500Mhz then can be used instead of TDC

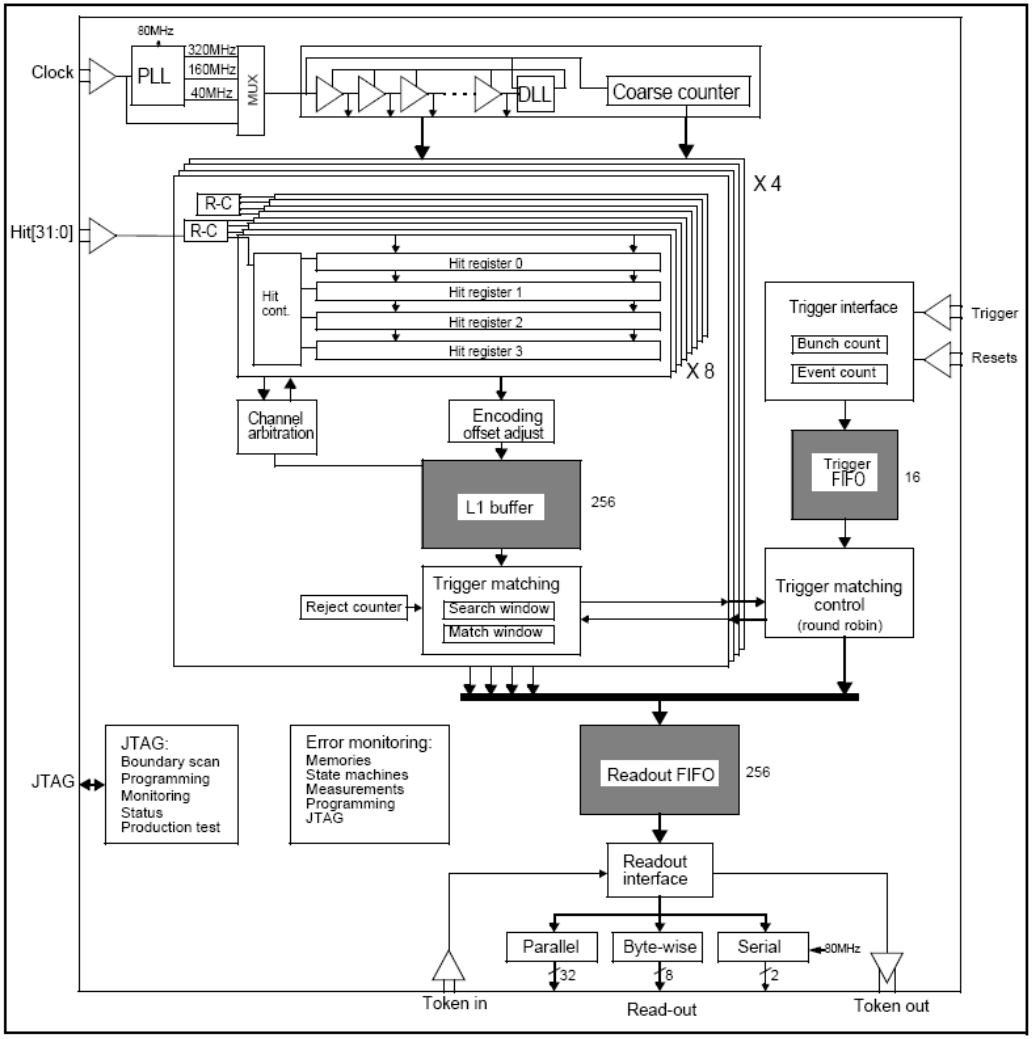
Read out schemes



Front-end solutions

MicroVerexDetector		
Pixel	TOPIX(INFN)	
Strip	FAIR-XYTER (GSI)	CSA + Hit detection ASIC
TPC - GEM	FAIR-XYTER/SuperALTRO	CSA + Hit detection ASIC
Planar GEM	FAIR-XYTER	CSA + Hit detection ASIC
StrawTubeTracker	CARIOCA/ASDQ +TDC	CSA + Hit detection ASIC
MDC – Straw tubes	CARIOCA(LHC) +TDC	CSA + Hit detection ASIC
Muon Chamber	Amp+Discr.(Minsk)	CSA + Hit detection ASIC
EMC		
Barrel/endcap	APFEL(GSI) +SADC	CSA + Hit detection ASIC
Forward	SADC	CSA + Hit detection ASIC
DIRC		
barrel	NINO ? + TDC	
ToP/FDD	NINO ? + TDC	
TOF	TDC	

HPTDC



CERN development for LHC experiments

Trigger driven

Bin size 100/25 ps

Resolution 25 ps

32/8 channels/chip

0.25u technology - radiation tolerant

2MHz/channel hit rate capability

Trigger less readout:

generate 1MHz trigger signal

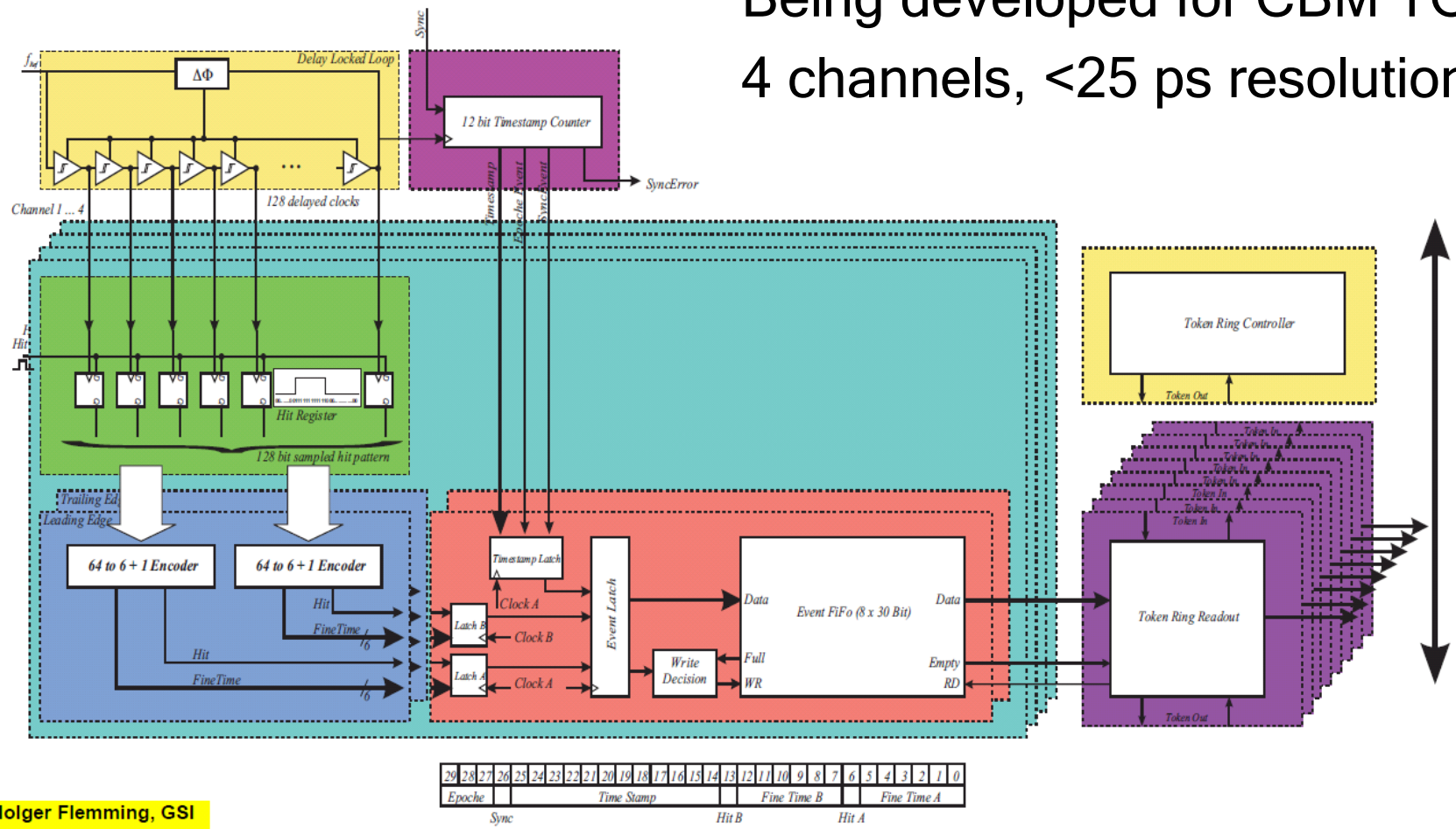
GET4 TDC

- Very high time resolution < 25ps
- Double hit resolution < 5ns
- Event rate up to 50 kHz per channel
- Capability to measure time over threshold
- Low power consumption with less than 30 mW per channel
- Number of Channels: ~ 65.000
- Triggerless operation:
  - Each event combined with a timestamp
  - Epoche event on timestamp counter overflow
- Timestamp counters of all chips have to run synchronously

GET4 TDC

Being developed for CBM TOF

4 channels, <25 ps resolution



Holger Flemming, GSI

Bodenmais, 2009

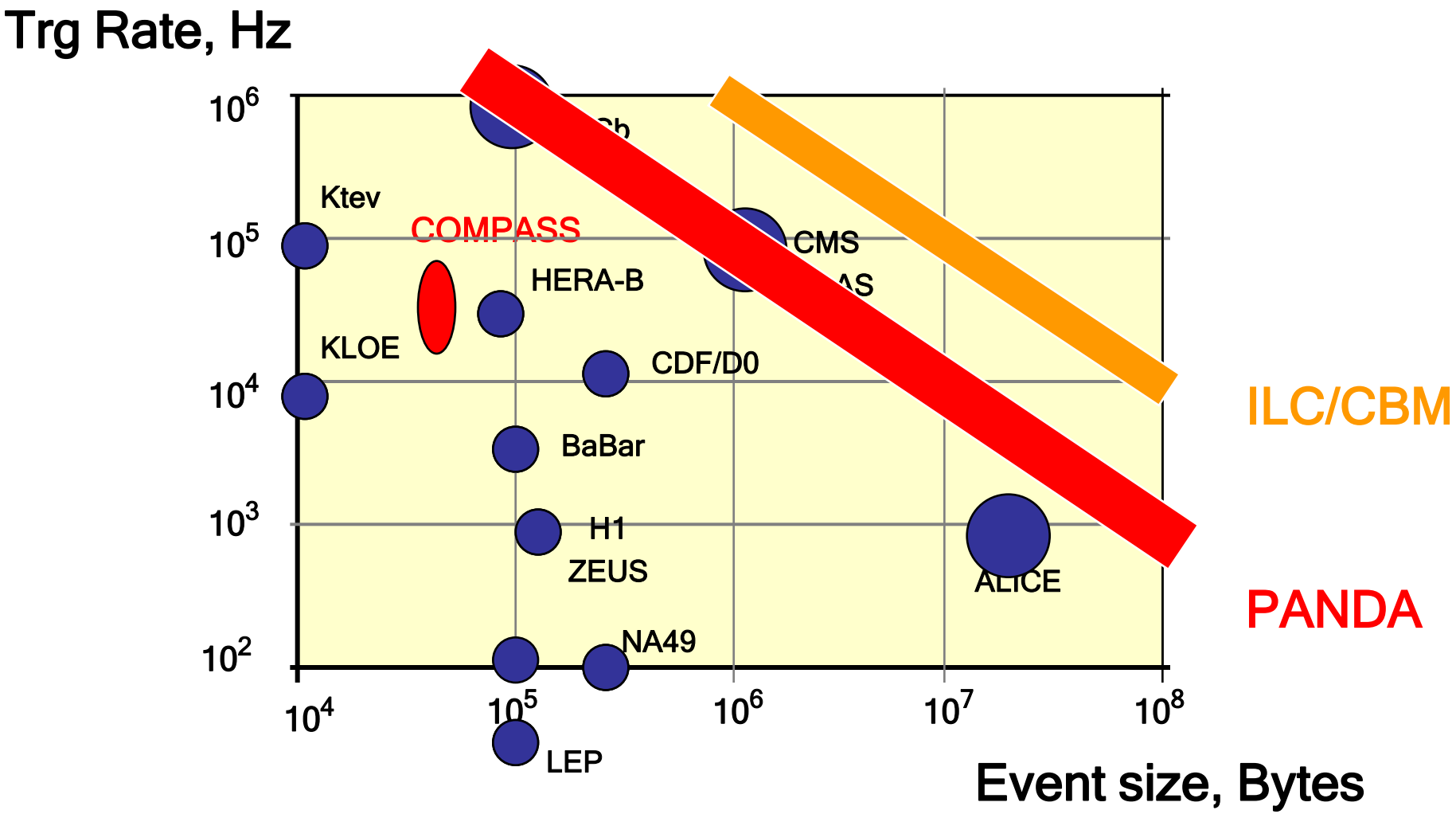
PANDA TDC solution

- HPTDC for Straw, Muon detectors
- GET4 TDC for DIRCs, TOF

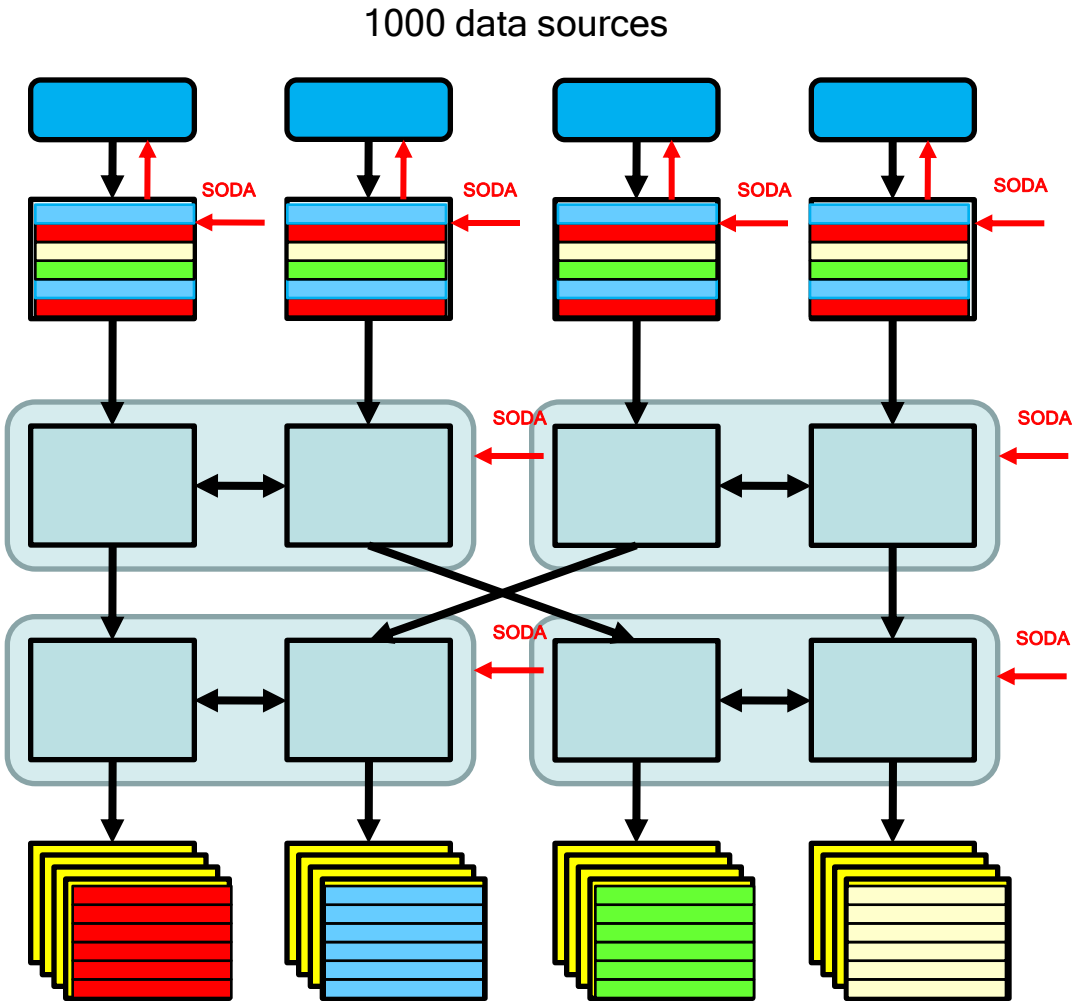
PANDA data rate

	# channels	Hit rate	Data rate
MicroVerexDetector			6 GB/s
Pixel	few M		
Strip	200 k		
StrawTubeTracker	5 k	35 MHz	0.35 GB/s
TPC - GEM	78 k	14 GHz	56 GB/s
Planar GEM	100 k	2 GHz	8 GB/s
MDC – Straw tubes	15 k	~2 GHz	20 GB/s
EMC			
Barrel/endcap	15 k	0.5 GHz	8/2 GB/s
Forward	1.5 k	1 GHz	16/4 GB/s
DIRC			
barrel	5 k	1 GHz	4 GB/s
ToP/FDD	1k/4k	5 GHz	20 GB/s
		Total:	140/120 GB/s

Compare rates



DAQ Architecture



Detector Frontends

Data Concentrator

First Stage Burst Builder

Second Stage Burst Builder

Compute Nodes Computer farms

SODA - time distribution system

Data processing

- FEE-Data concentrator
  - Feature extraction : time & amplitude
  - Clusterization
  - Time ordering
  - Slicing continuous data stream into data blocks
- Burst builder
  - Deliver data of one burst to one Compute Node
- Compute Node or Computer farms
  - All other tasks

Slicing Data in time

- **Slicing synchronously with HESR**
  - HESR duty cycle: 2us beam + 400 ns gap
  - Burst block size ~300 kB
  - Big Block size fluctuation – 20/40 events

  Detector's drift time < 200 ns but TPC Tdrift = 50 us

- **Super burst of 500 us**
  - TPC data at boundaries copied to both data blocks
  - Super block size ~60 MB
  - Advantage: small variation of block sizes

SODA functionality

- Provision of clock reference < 20ps
- Synchronization with HESR operation
  - Burst or super burst
- Monitoring status of FE and DAQ components
- Data flow control
  - Define switch topology

DAQ electrical-mechanical standard

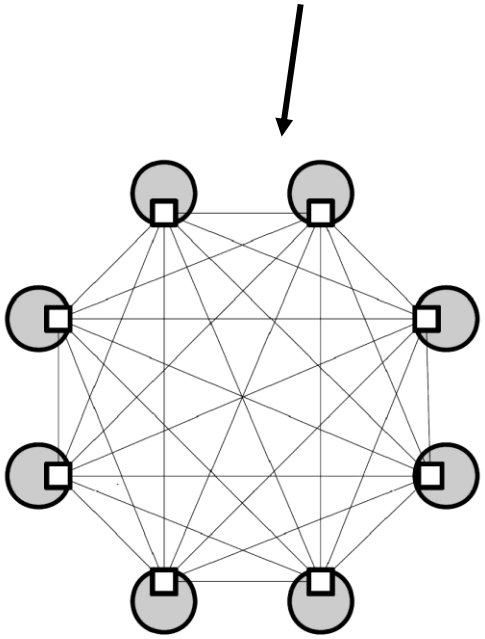
ATCA (Advanced Telecommunication Computing Architecture)

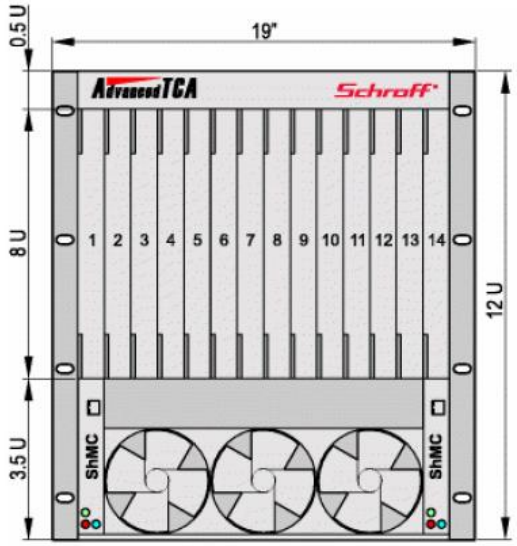
8U module 322x280 mm^2

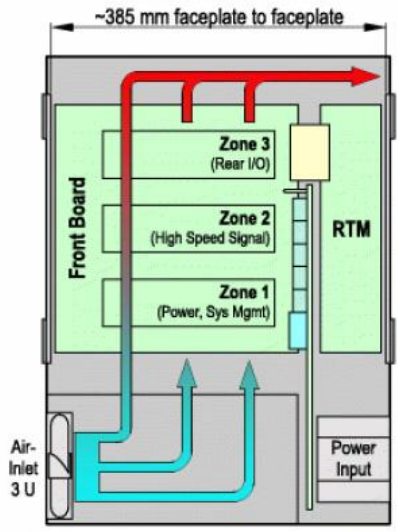
Power redundant 48V , 150W/module

Backplane – high speed point to point connections :

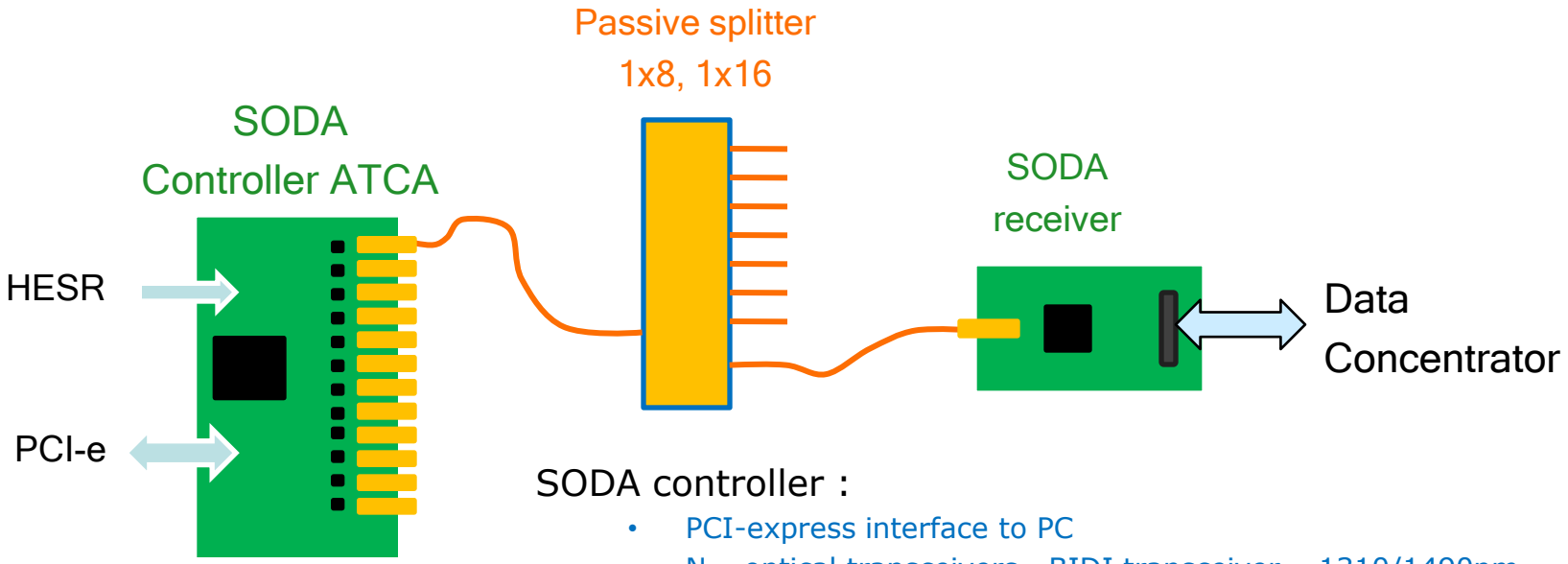
- double star – 2 HUB modules to all others
- full mesh – every module to any other module







SODA architecture



SODA controller :

- PCI-express interface to PC
- N – optical transceivers, BIDI transceiver – 1310/1490nm
- Lattice ECP2M FPGA with SERDES: Controller -> Receiver
- Texas Instrument TLK1221 SERDES: Receiver->Controller
  - fast Relock Times less than 256 ns

Optical splitter :

- Single mode fiber
- Insertion losses
  - 1x8; 1x16; 1x32

SODA receiver:

- Mounted directly on Data Concentrator module
- Lattice ECP2M FPGA SERDES
- Optical transceiver BIDI 1490/1310nm

THANK YOU

Spare slides

COMPASS RICH1 before upgrade

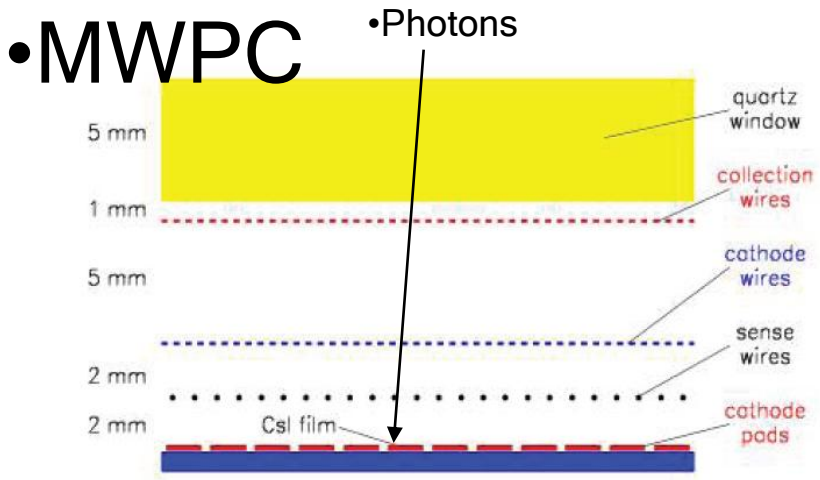
Trieste: INFN, Univ. & ICTP,
Turin: INFN and University,
Bielefeld University,

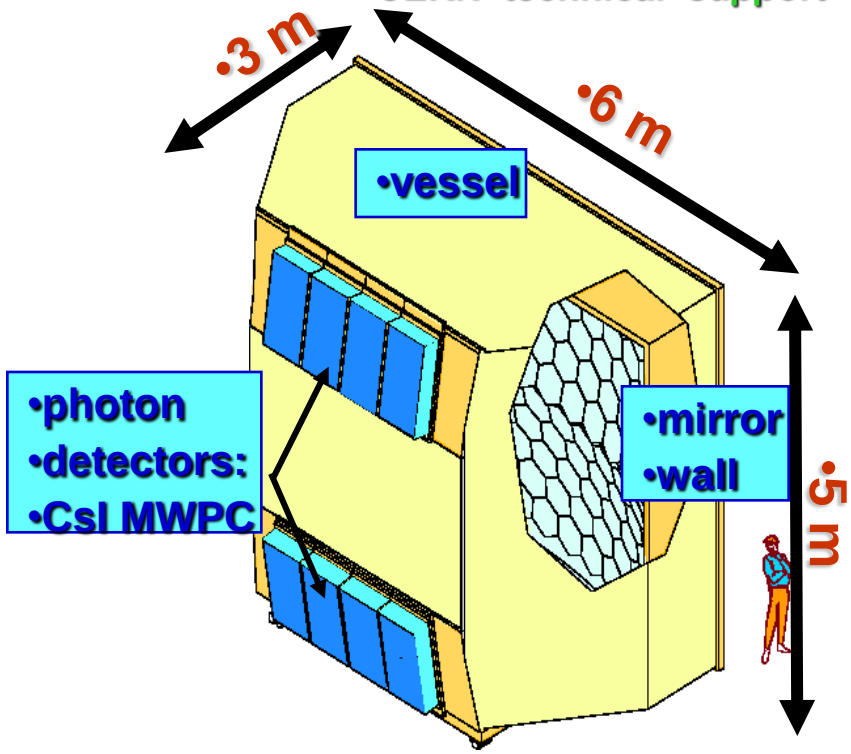
CERN technical support

Large acceptance
- H: 500 mrad
- V: 400 mrad

Radiator gas: C4F10
PID: π, p, K in 5-50 GeV range
Photon detection: MWPC with CsI coating,
Detected photons with λ = 160-200nm

MWPC:
8 chambers , 144x72 pads each
80 000 pads(8x8mm2) read by GASSIPLEX FE chip



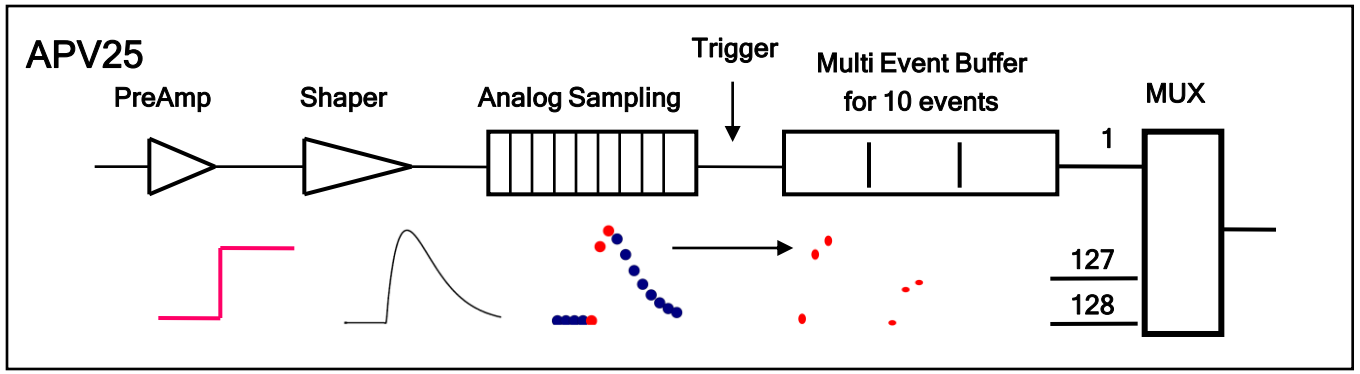


FEE: APV25-S1 - generic ASIC

APV25-S1 developed for CMS silicon µ-strip detectors

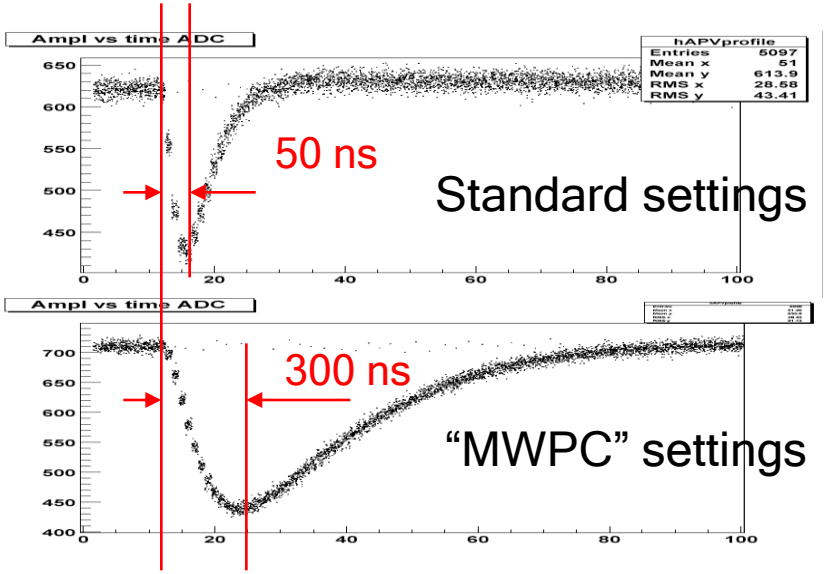
Features:

- 128 channels
- analog pipeline (SCA) runs with 40MHz clock
- 1 or 3 samples /event
- 50 ns peaking time
- external trigger
- no zero suppression

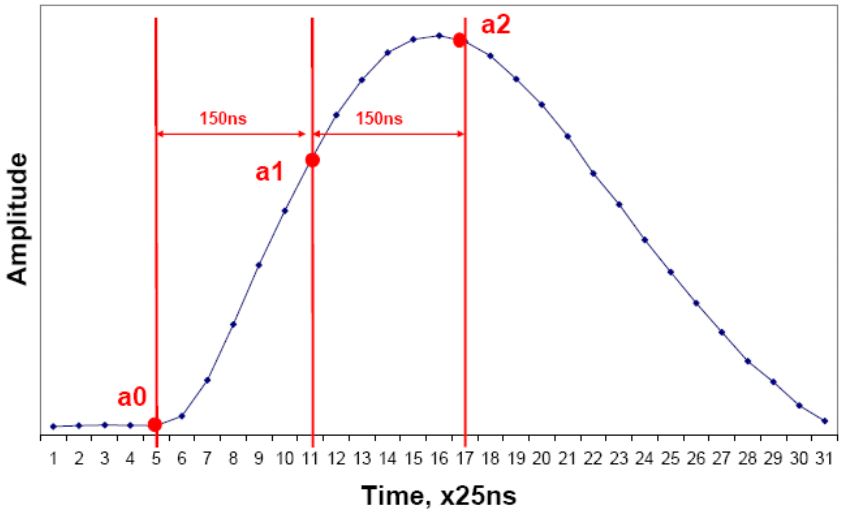


- COMPASS : Silicon, GEM, RICH MWPC CsI photo cathodes
- programmable preamplifier and shaper ->
  peaking time can be programmed between 50 and 300 ns
- 3 or more samples/event -> Pulse Shape Analysis -> Amplitude & Time
- Low cost read out – less than 5 Euro/channel

APV25S1 programmable range



APV response



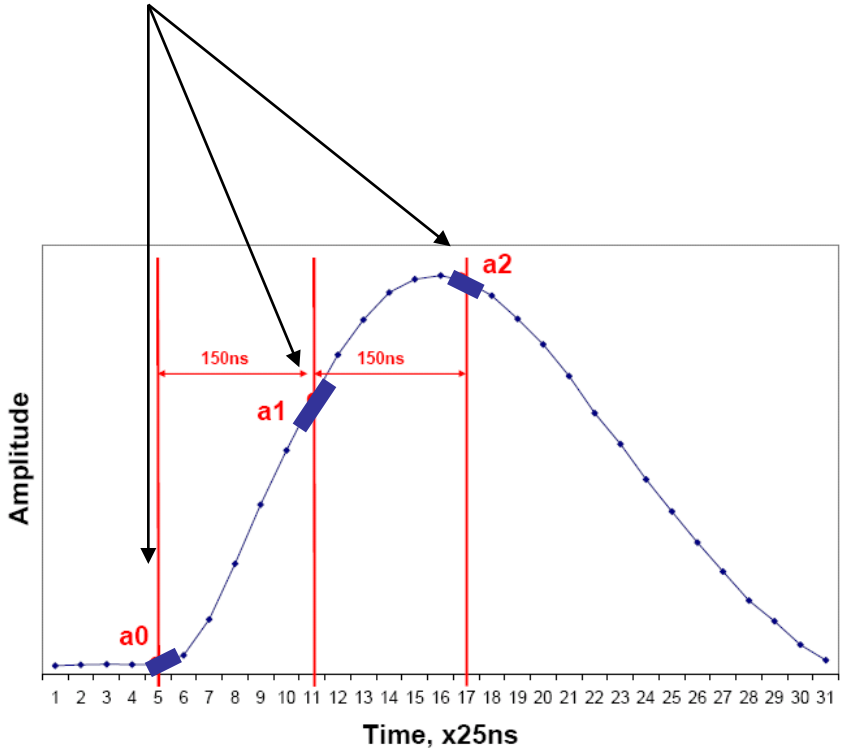
Reading 3 samples

- first sample -> pedestal
- second sample -> slope
- third sample -> amplitude

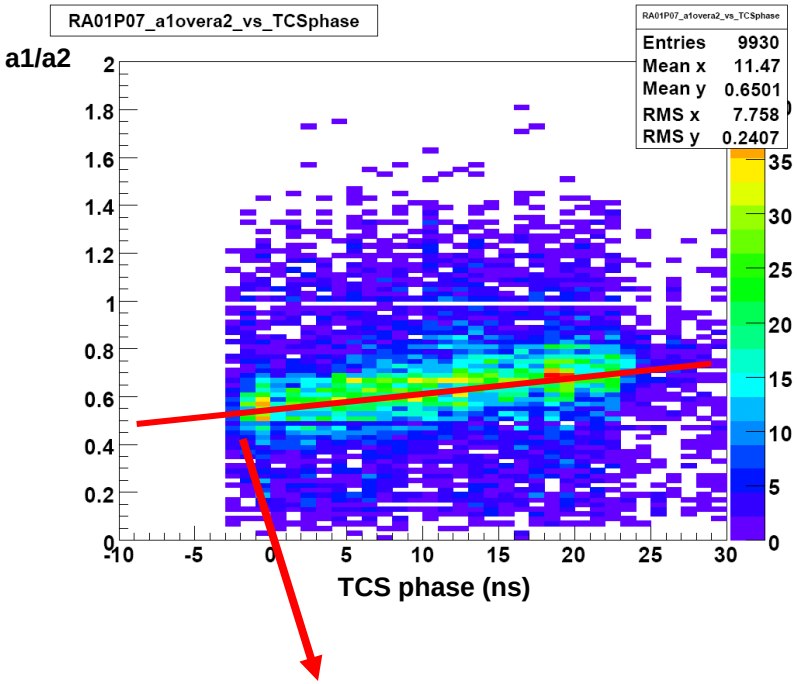
Time measurement with APV25-S1

Time measurement:

- a0, a1, a2 sampled by TCS clock (40MHz)
- beam is asynchronous to clock
- 25 ns jitter



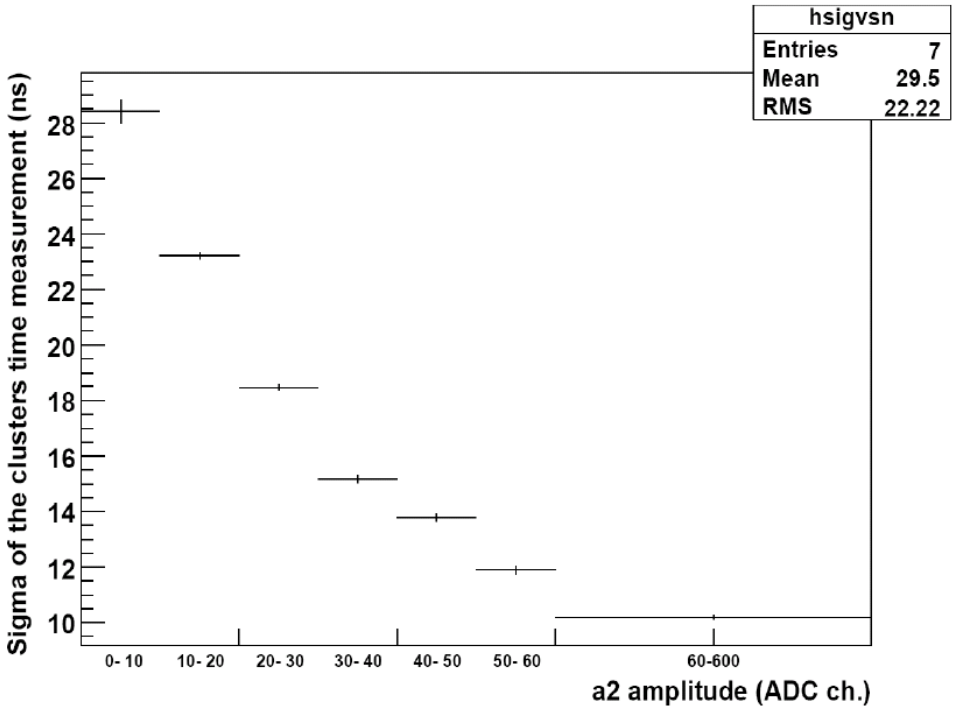
a1/a2 vs clock phase



Equation for time calculation

T = a1/a2 * 156.25 – CLOCK_phase

RICH time resolution vs amplitude

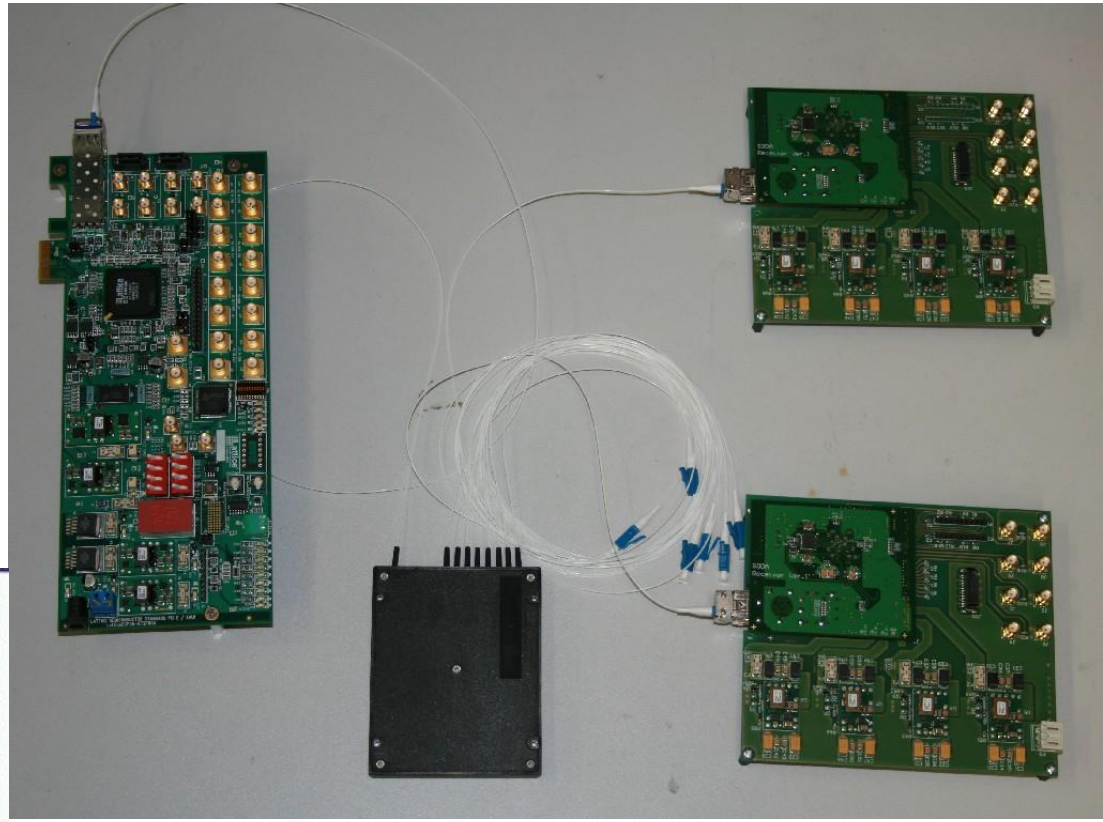


Silicon : σ = 2ns

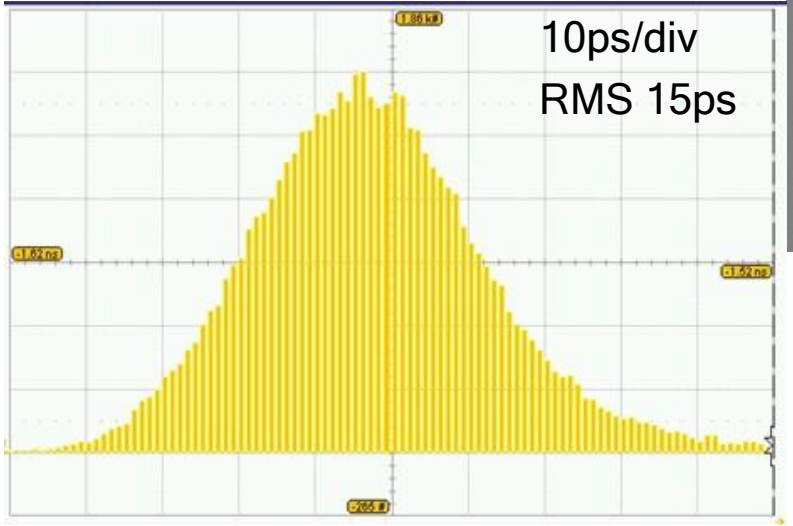
GEM : σ = 10ns

Test setup

- Lattice PCI-e evaluation card
- Optical splitter 1:8
- 2x SODA receivers mounted on evaluation cards



Reference Clock vs Recovered Rx Clock



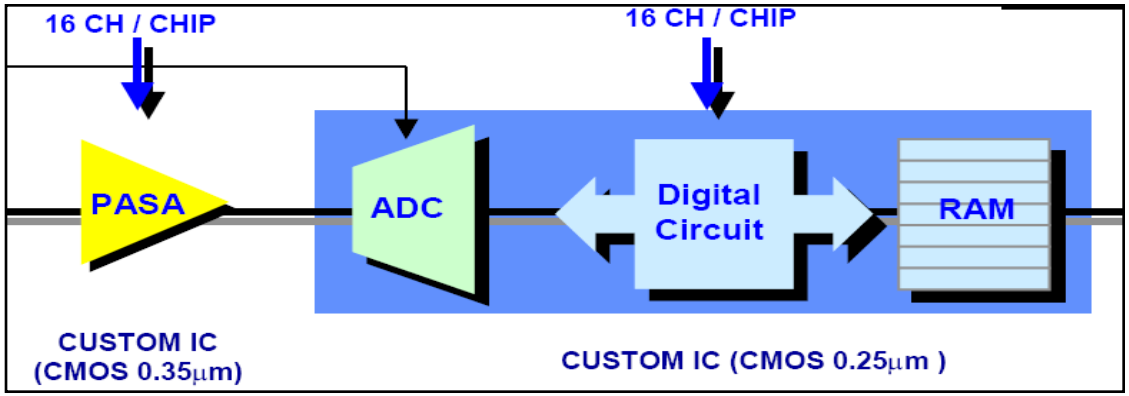
PASA and ALTRO chips

Developed for ALICE TPC (MWPC) 2003

Preamplifier/Shaper independent chip -PASA

ALTRO optimized for low power

- 10bit ADC 20MSPS – commercial IP core
- Advanced digital signal processing
- Pipeline architecture
- Power consumption 40mW/channel @ 20MHz



Motivation for TRIGGER less DAQ

- Wide physics cases – different criteria for event selection
- Complicated event selection criteria
  - Identification of short lived particles - Impact Parameter
  - photon clusters in EMC with veto of charged particles in front e.g. η_c
  - Electron identification
  - Particle ID in MVD, TPC/Straw detectors (dE/dX)
  - Cherenkov PID
  - Λ reconstruction
  - Muon Identification
  - …

Almost every detector is needed for trigger decision

Technical reasons:

- Feasible design of FEE with built-in zero suppression
- Available higher performance and lower power FPGA/CPUs
- High performance networks
- Flexible software trigger algorithms – closer to offline data processing

Logical step in development of readout systems