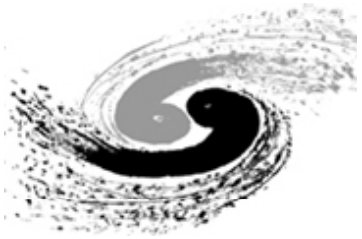
Recent Progress on the Compute Node



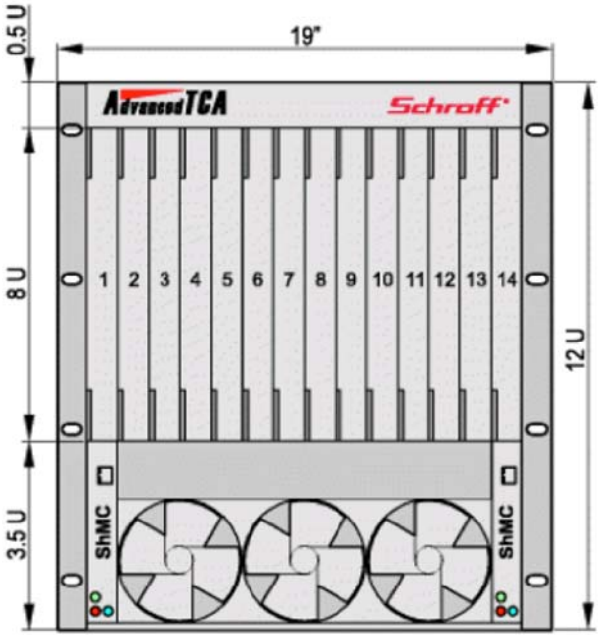
Qiang Wang

April 23th, 2009

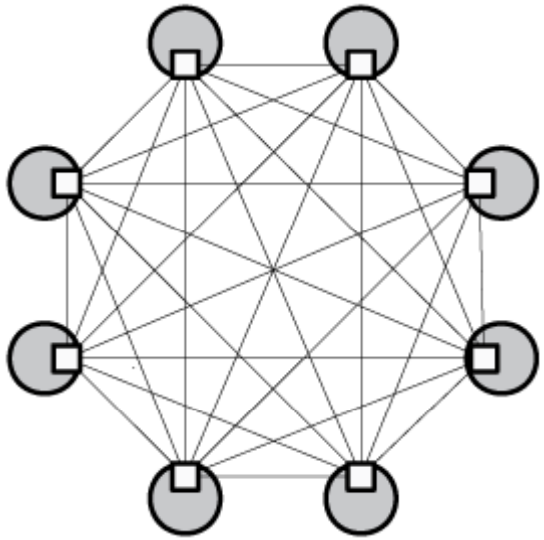
Outline

- Introduction to Compute Node
- Boot up system design
- Debugging of Compute Node (Old version)
- Hardware design modification
- Demo system
- Next steps

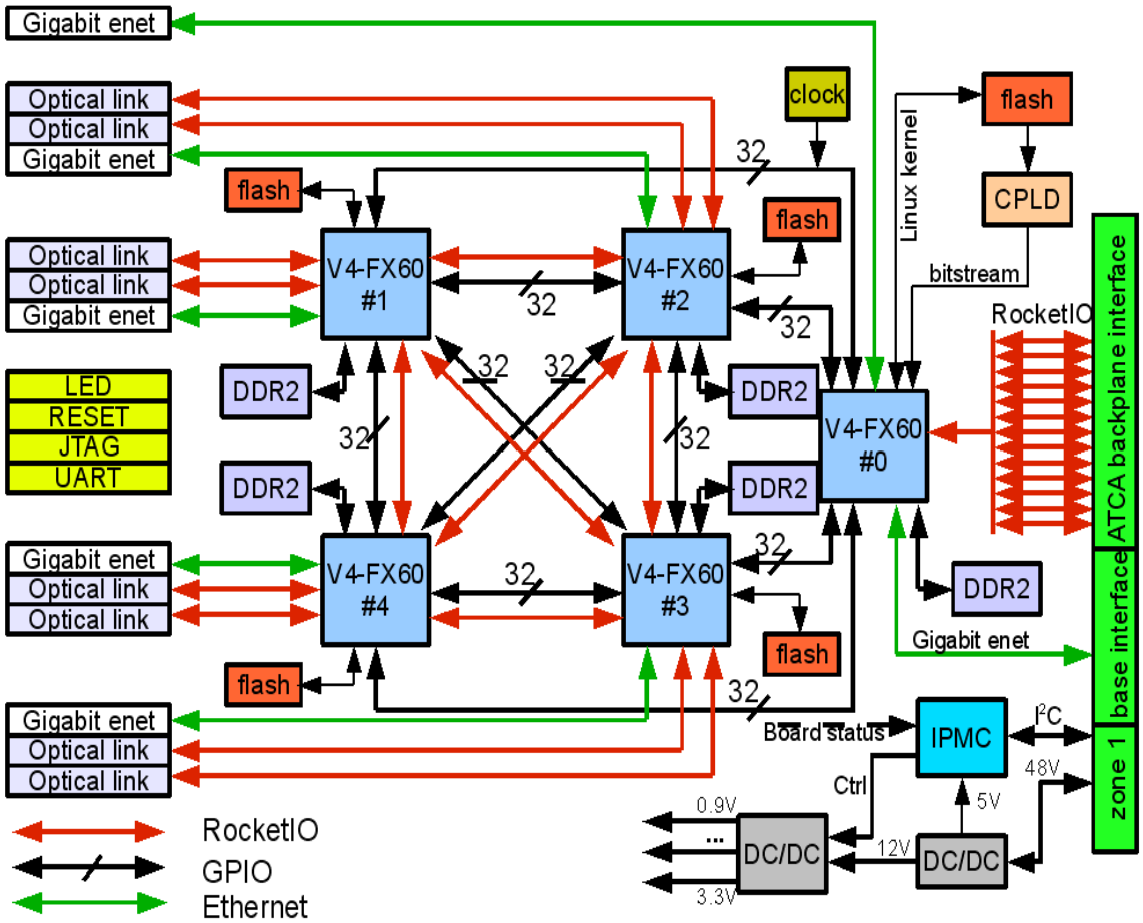
Introduction to Compute Node



- A key module for PANDA Trigger and Data Acquisition system
- An universal high performance platform prepared for multiple applications
- ATCA standard (Full Mash topology in backplane)
- FPGA(now Virtex-4)



Introduction to Compute Node



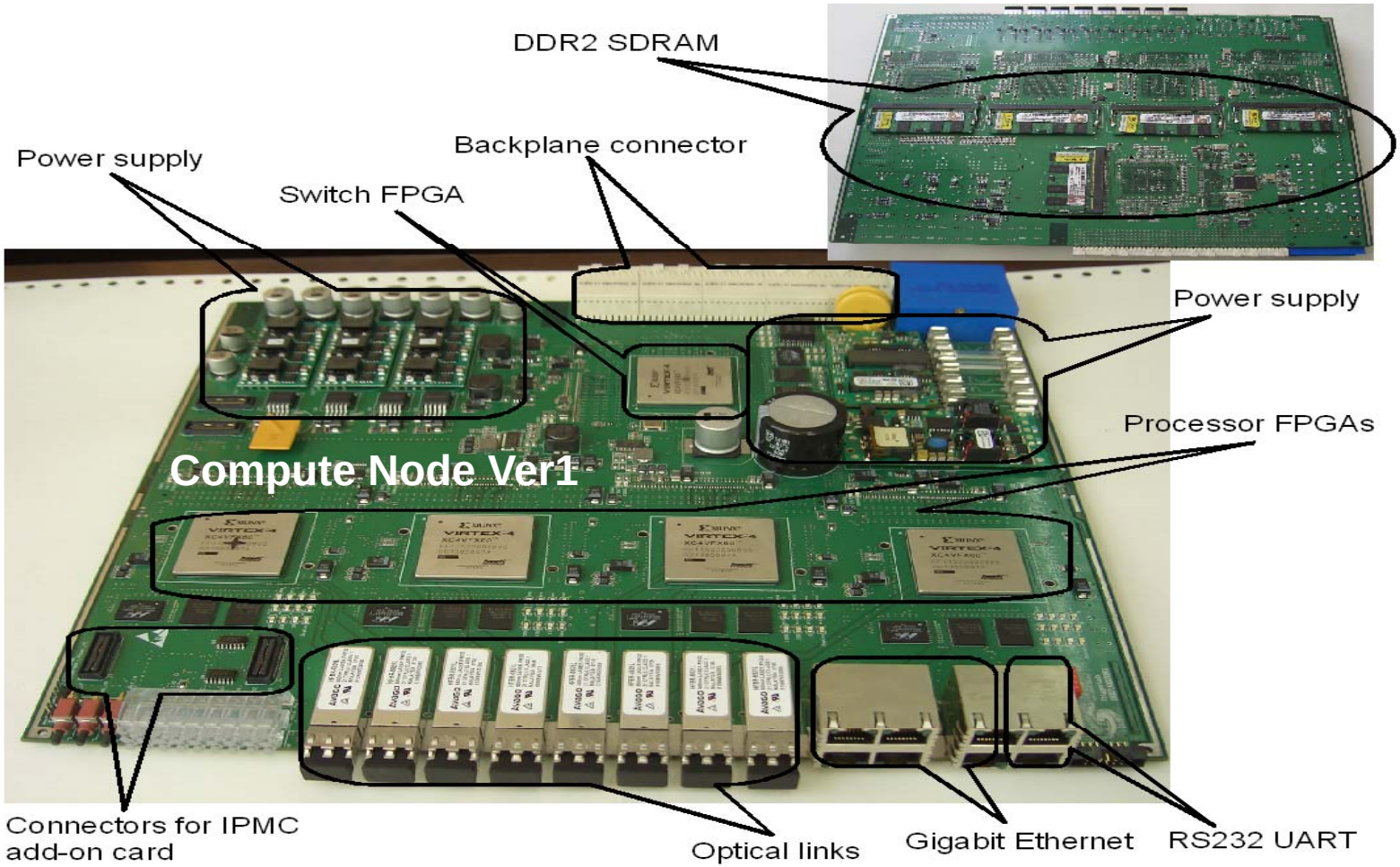
High Computing power

- 5x (Virtex-4 FX 60 FPGA + 2GB DDR2)

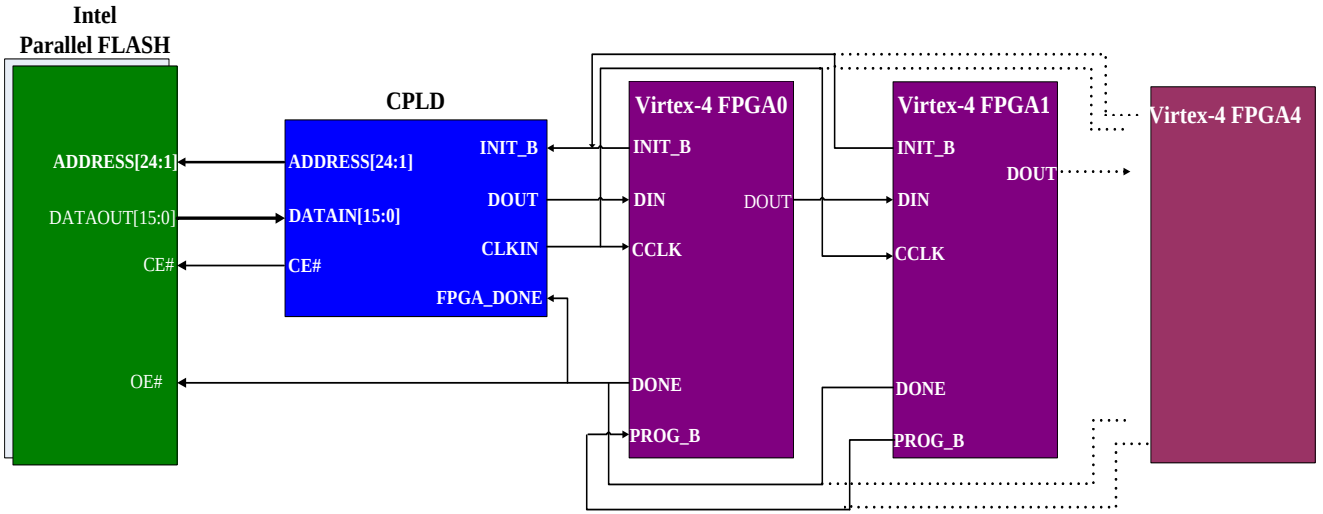
High bandwidth

- 6 Gigabit Ethernet (one on backplane base channel)
- 8 Optical link
- 13 RocketIO to backplane

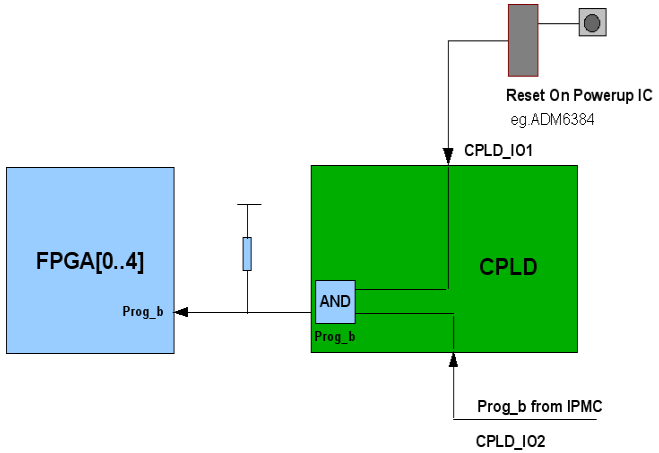
Introduction to Compute Node



Boot up system design



- Using CPLD to control the configuration procedure. Five FPGAs are configured in Slave Serial Mode.
- Add a rest-on-powerup IC to be able to boot up on power up.
- Reboot when power up, pressing configuration button (remote rebooting controlled by IPMC).



Boot up system design

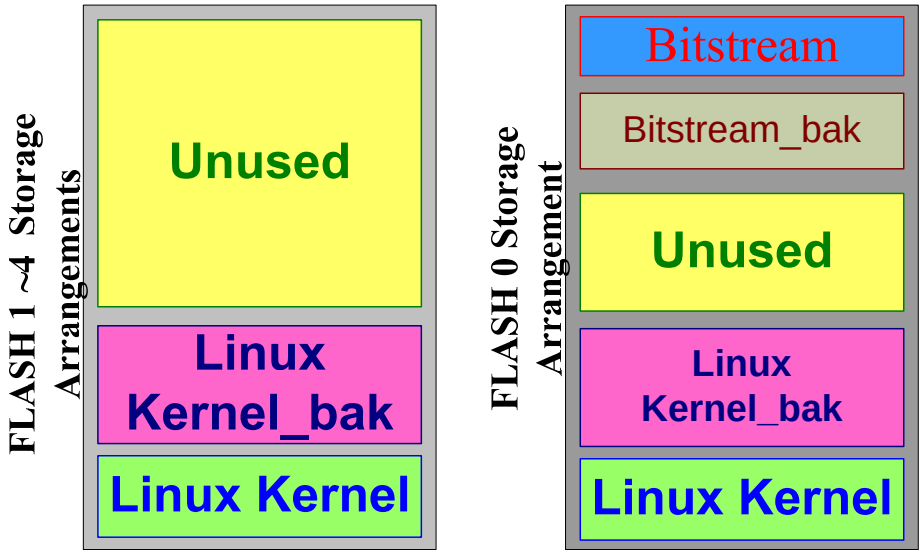


Fig. Flash storage arrangement

- Using different Flash memory arrangement for FPGA0 and FPGA1~4
- Concentrate all five FPGAs' bit files into a single one for booting up five FPGAs at one time
- Multi-boot capability is considered

Boot up system design

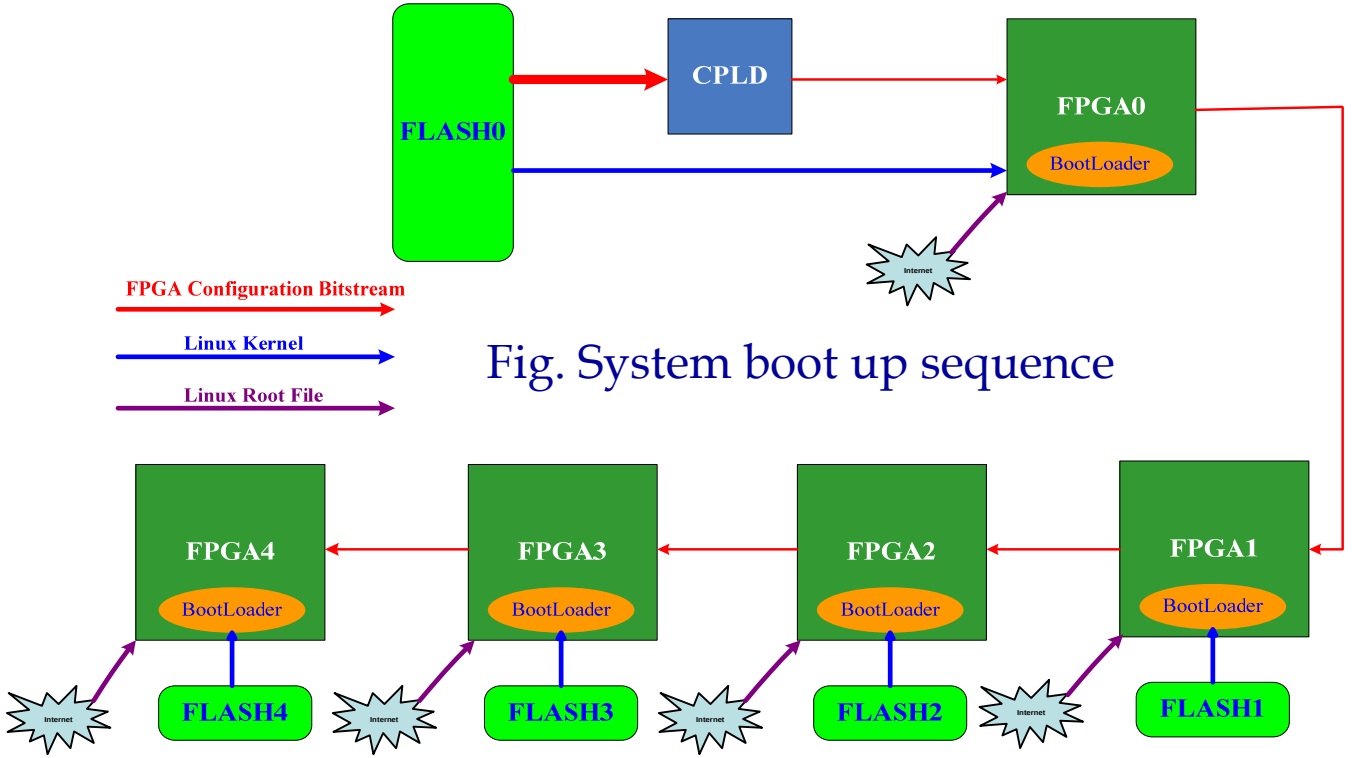


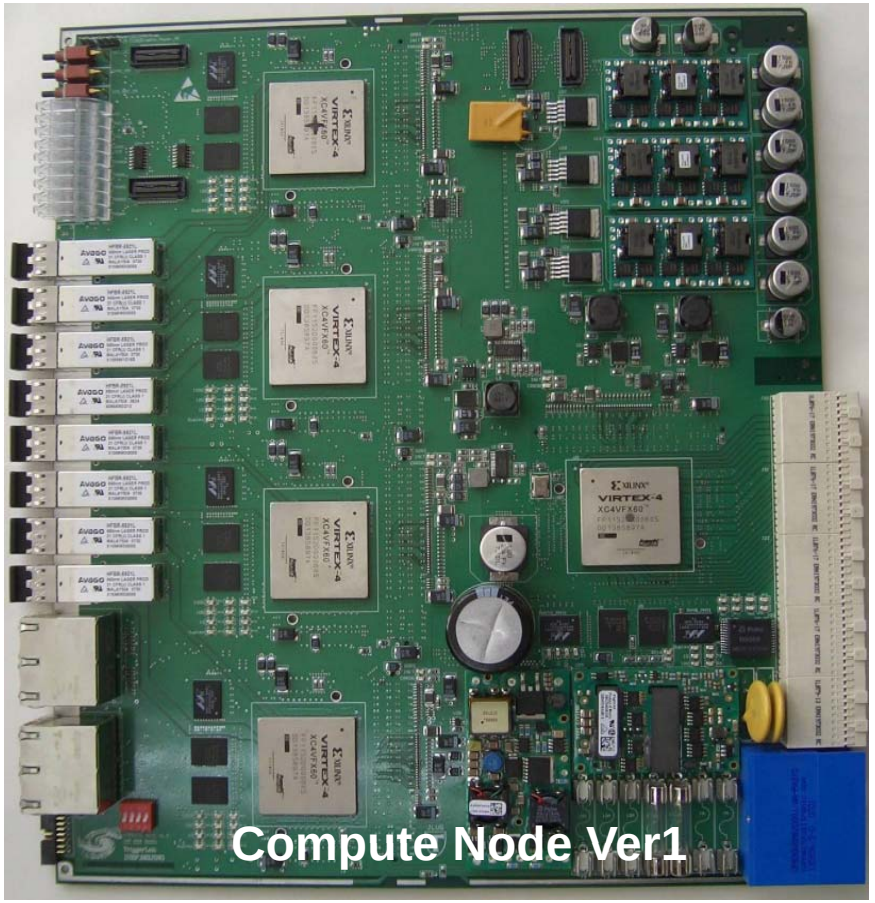
Fig. System boot up sequence

- Each FPGA in the chain is configured with the dedicate bit file.
- Linux system boot up correctly with Linux kernel stored in Flash memory and an NFS root file system built on host PC.

Debugging of Compute Node

Most function can fulfill our application and some problems found during debugging

- RocketIO for cross link between on board FPGAs can not work.
- PHY chip(88E1111)can not be configured correctly without revising its driver in Linux kernel
- FPGA0 Ethernet signal is not good, the layout length exceed the design rule
- Configuration circuit not fit for multiple FPGA configuring cases
- Optical transceiver not use SFP type which limit the application.
- Problem with I2C chip address setting
- Some component profile not fit
- RocketIO do not AC coupled to backplane
- Base channel connected in 100Mpbs mode
- And some small errors



Hardware modification

All found errors in first version are corrected in new version of CN

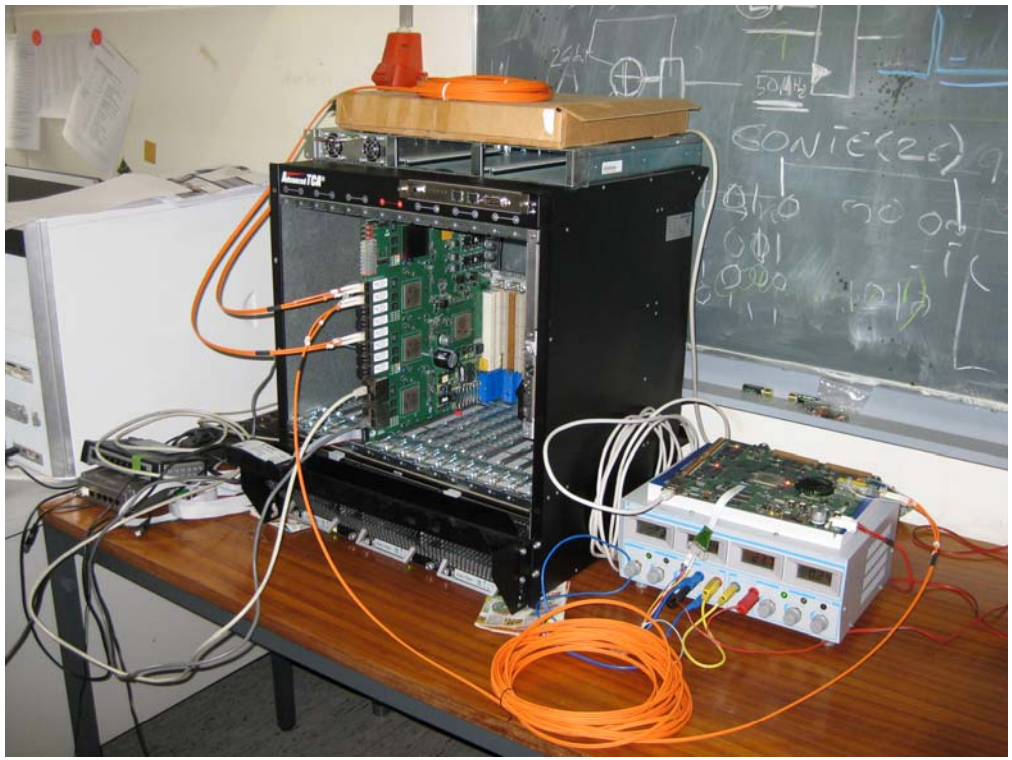
- ✓ **Add another oscillate for each FPGA**
- ✓ **Default configuration for Ethernet PHY was corrected**
- ✓ **Ethernet connector individually to reduce signal layout length to qualify better SI (especially for FPGA0 Ethernet port).**
- ✓ **Configuration circuit was revised for multiple FPGA application**
- ✓ **SFP/SFP+ compatible optical transceiver is used in new Version (SFP+ can work at up to 8.5Gbps which will be fit for higher bandwidth application)**
- ✓ **I2C chip address configuration was corrected**
- ✓ **Base channel connected in 1 Gbps mode**
- ✓ **The connector on front panel are modified to low profile ones**
- ✓ **And others**

Hardware modification

- 2 new boards are available for IHEP,4 new boards for Giessen will be available very soon.

A demo system

- Optical link between Compute Node and TRB is set up, Linux system work smoothly with Optical link transmitting test data at full speed, power consumption is measured in this case.



The next steps

- Interconnection between four FPGAs on the board will be tested very soon.
- Backplane RocketIO transmitting test will be done when we have more CNs ready.
- Some ready algorithms will be fixed in the system to do some test with simulation data.
- Testing with TRB (Hades Trigger Readout Board) continues

Thanks!