PANDA DAT SYSTEM
towards the final architecture

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Agenda

- Designing and modeling
  - Requirements from PANDA exp
  - Conditions and Assumptions
    - global clock, hw signals from machine, FEE operation
  - Modeling tool and strategies - systemC
- Architectures:
  - PUSH-PULL
  - PUSH-ONLY

Requirements from PANDA

- interaction rate: 10 MHz
- typ. event size: 4 – 8 kB
- raw data flow: 40 - 80 GB/s
- flexibility in the choice of triggering algorithm
- cost efficient (COTS components)

Conditions

- System wide clock signal
- Lack of hardware trigger
- „burst signal” from machine:
  - 2us beam time + 400 ns idle

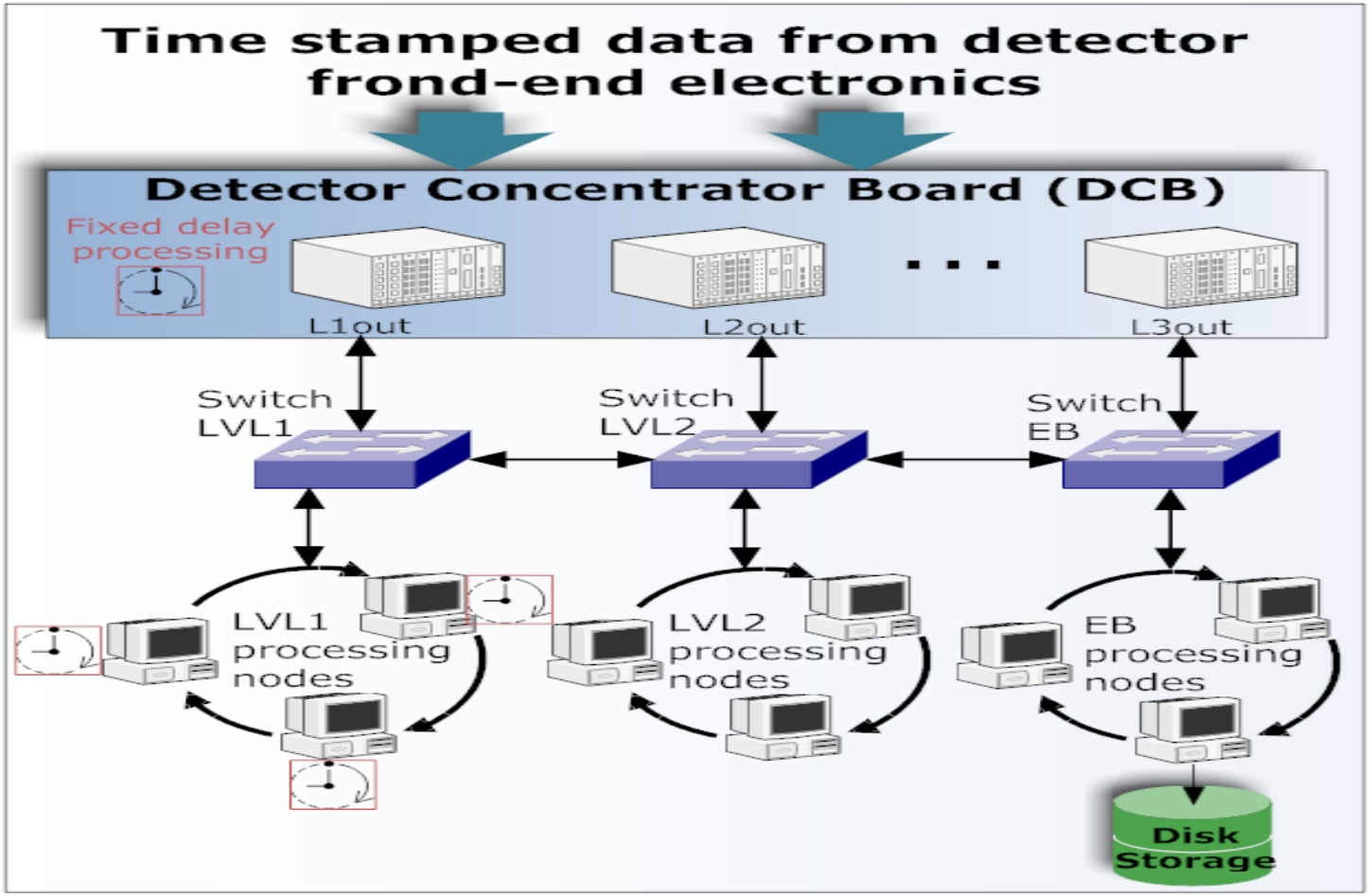
FEE Assumptions

- Front End Electronics:
  - Receives precise synchronous clock signal from the central distribution system
  - Continuously sampling mode of operation
    - capable of autonomous hit detection
  - Tags data with the interaction time based on the central clock

Modeling

- Dicrete event simuation as opposed to clocked
  - State of the modeled system is analysed only in discrete moments in time when the state changes
  - Analysis can lead to generation of new, future moments of change
  - Best suited for architectural studies
    - TLM – Transaction Level Modeling
  - SystemC

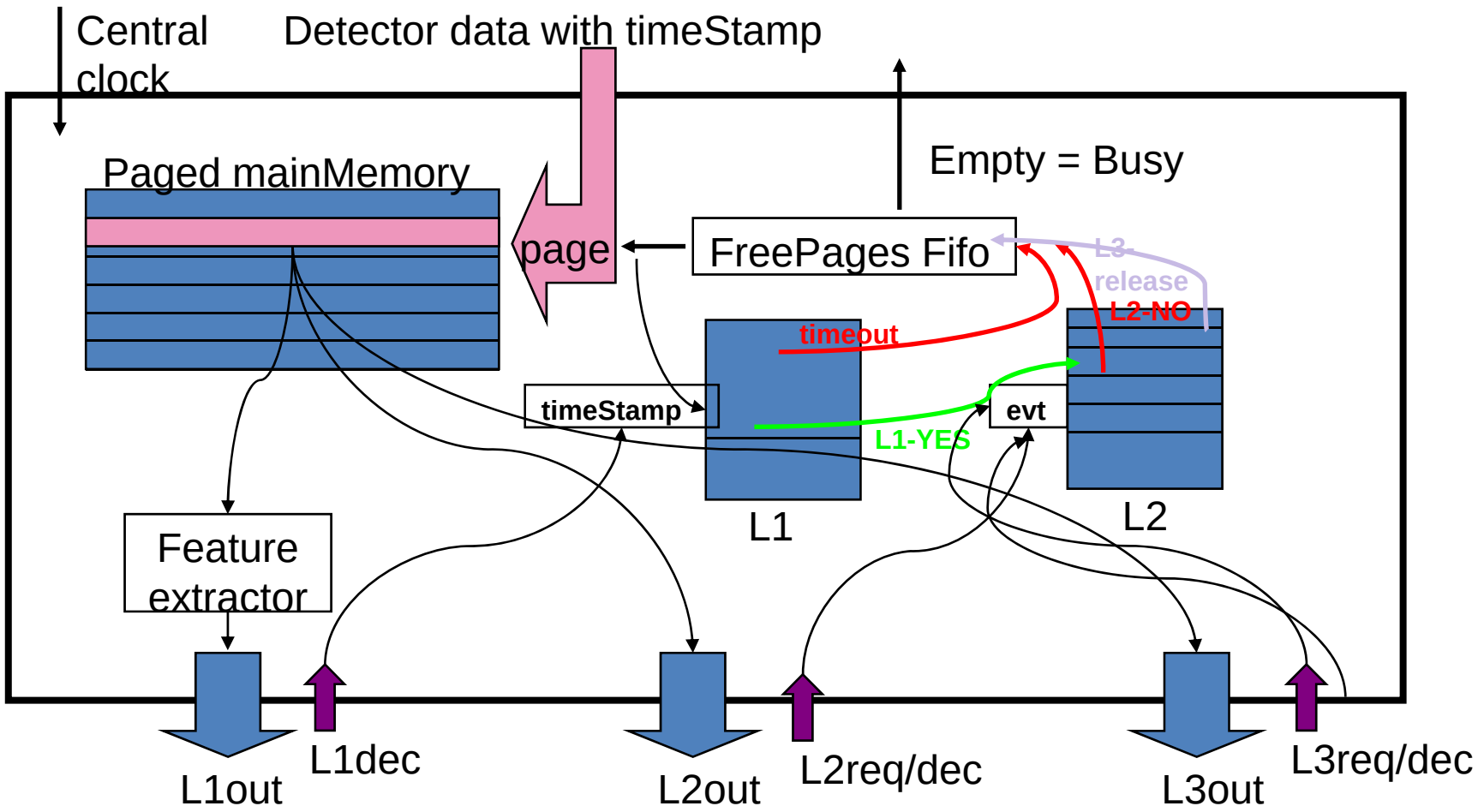
PUSH-PULL architecture



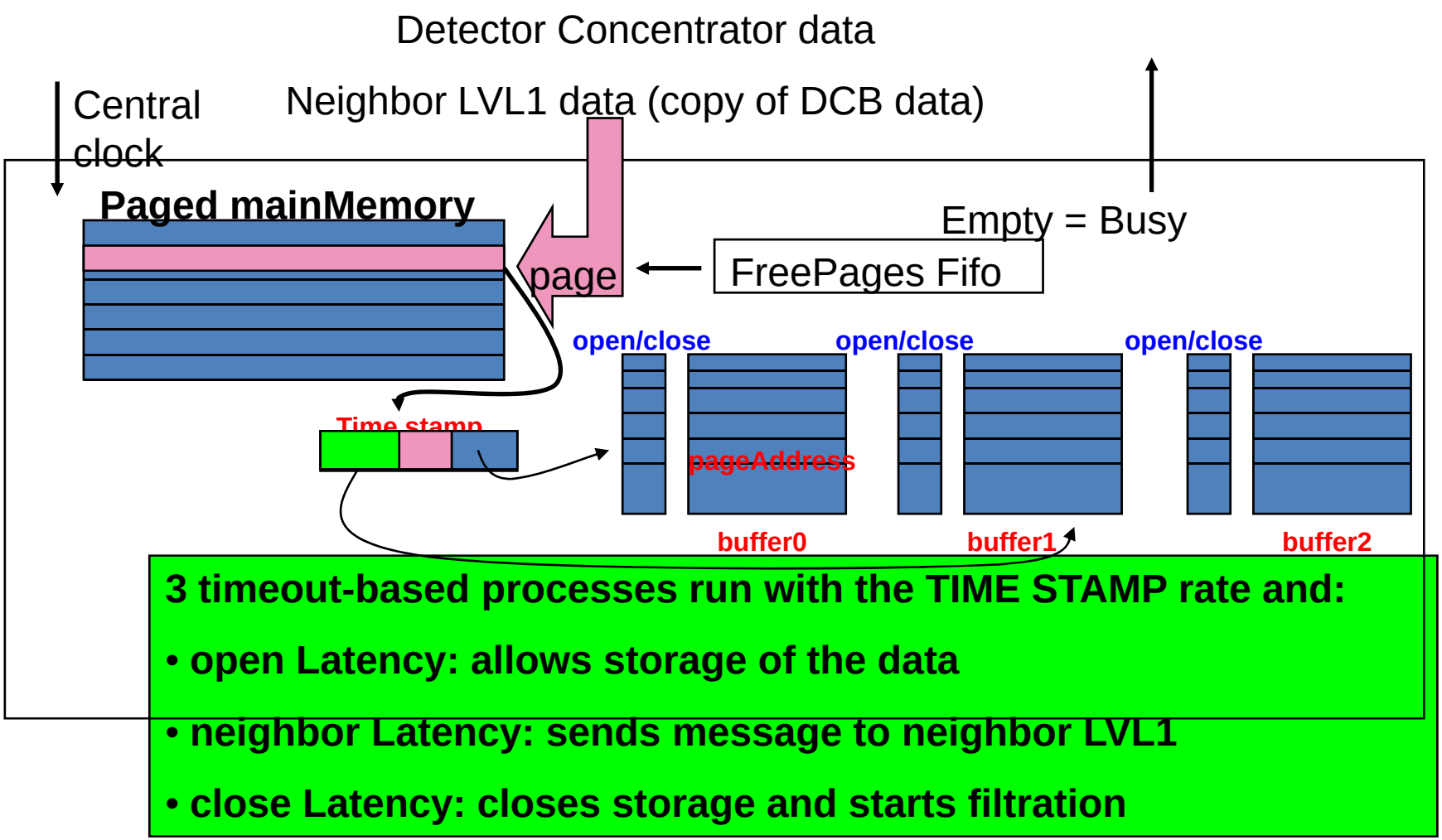
PUSH-PULL: main features

- Three filtering levels leading to Event Building
  - DCB local correlations (hardware)
  - L1 PANDA wide correlation (hardware/software)
  - L2 PANDA wide correlations (software)
- No hardware trigger signal needed (data identification based on time stamps)
- Scalable: addressing scheme allows for load and throughput balancing

PUSH-PULL: Detector Concentrator Board



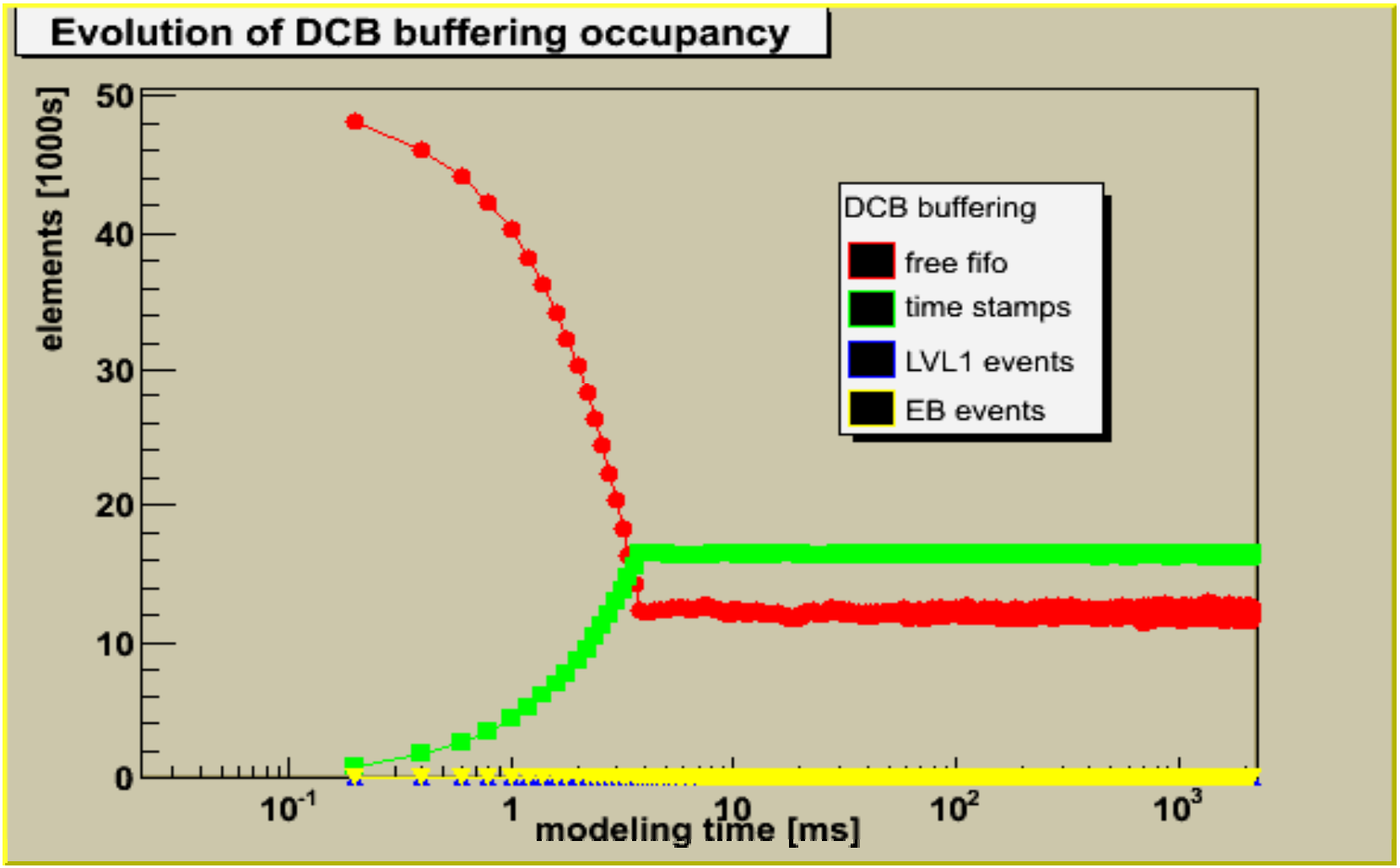
PUSH-PULL: L1 Processing Node



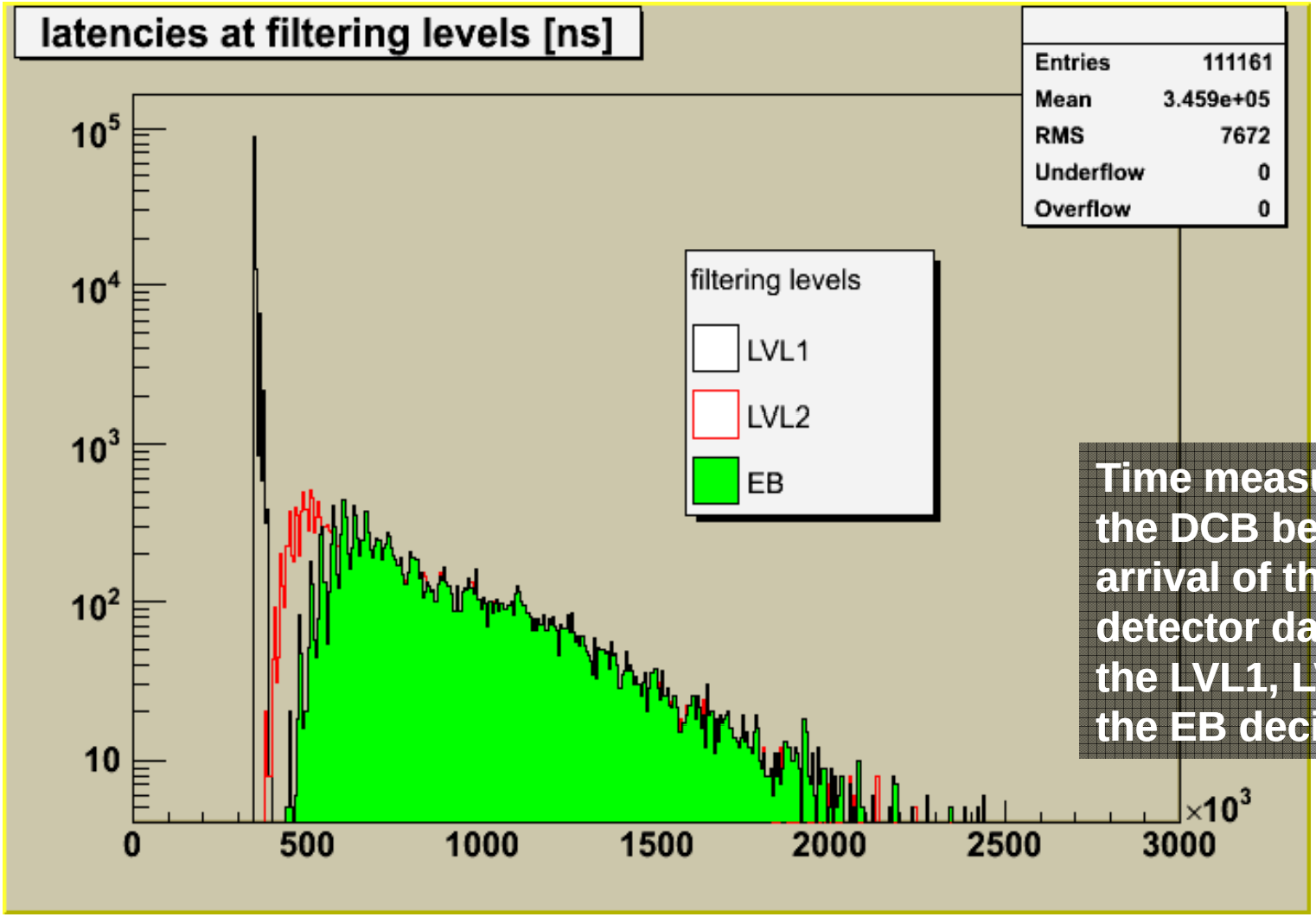
PUSH-ONLY model

- **Model of the architecture:**
  - **Creates physics generator (100 ns inv exp inter-event)**
  - **Creates 5 detectors with various sizes of data**
  - **Creates 40 DCBs (8 DCBs per detector)**
  - **Creates 40 LVL1 processing nodes, 40 LVL2 processors and 40 EB processors**
  - **Creates 3 Ethernet switches**
  - **Connects all the components with 1Gbps Ethernet links**

PUSH-PULL modeling results

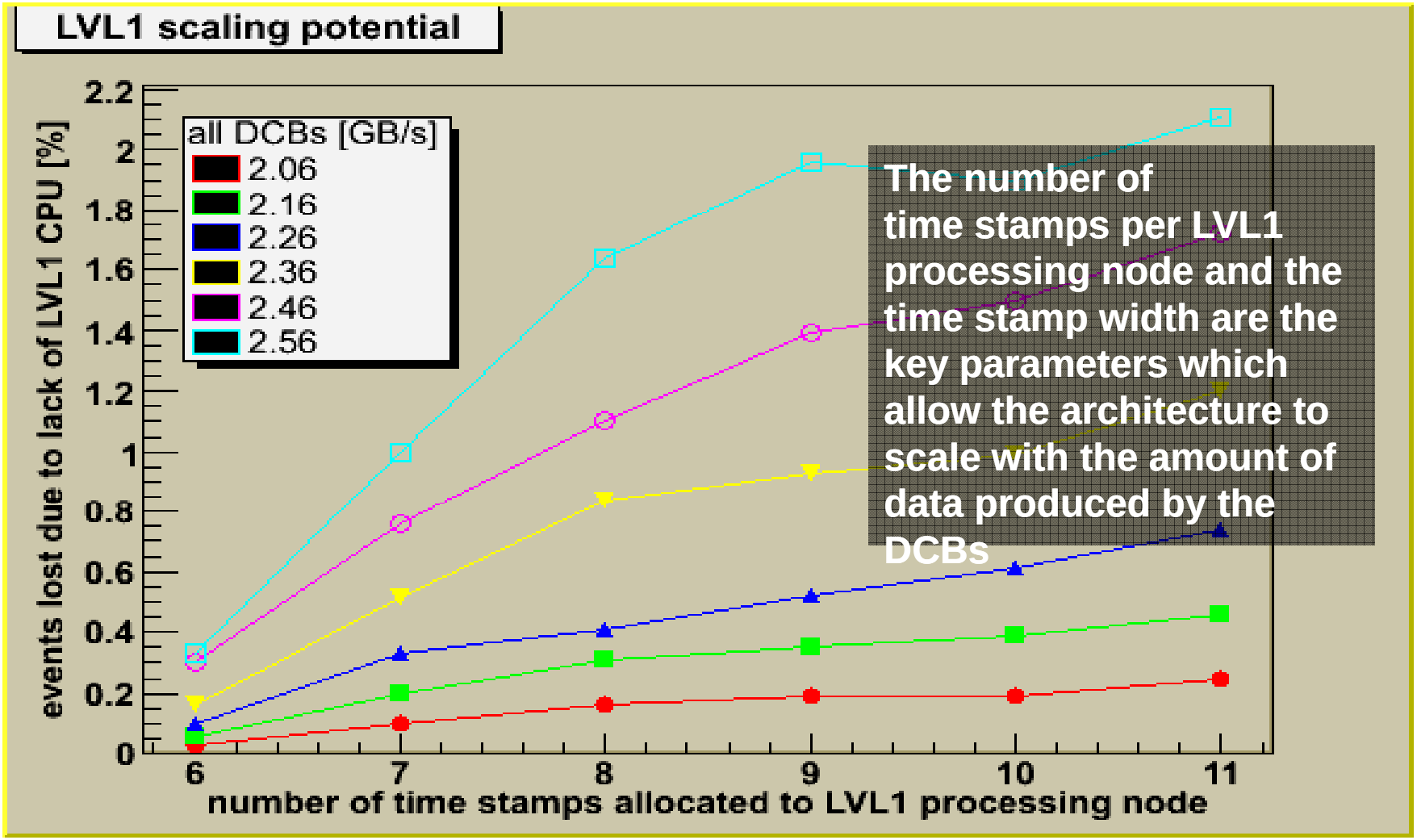


PUSH-PULL modeling results

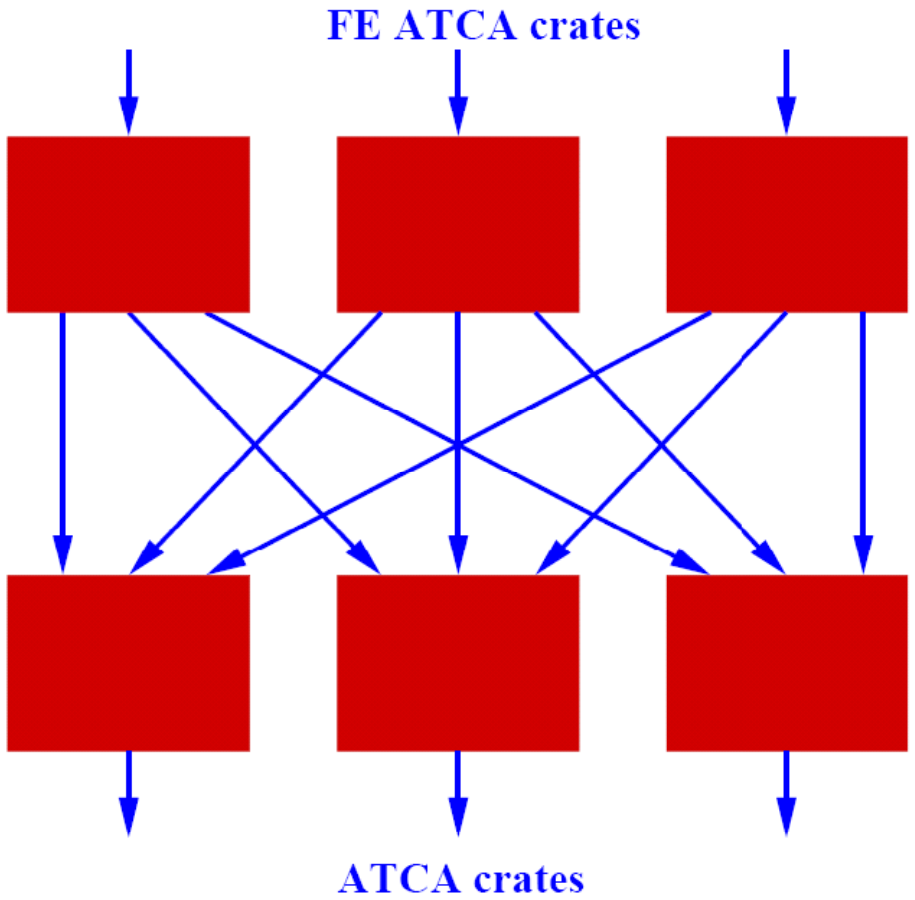


Time measured at the DCB between arrival of the detector data and the LVL1, LVL2 and the EB decision

PUSH-PULL modeling results



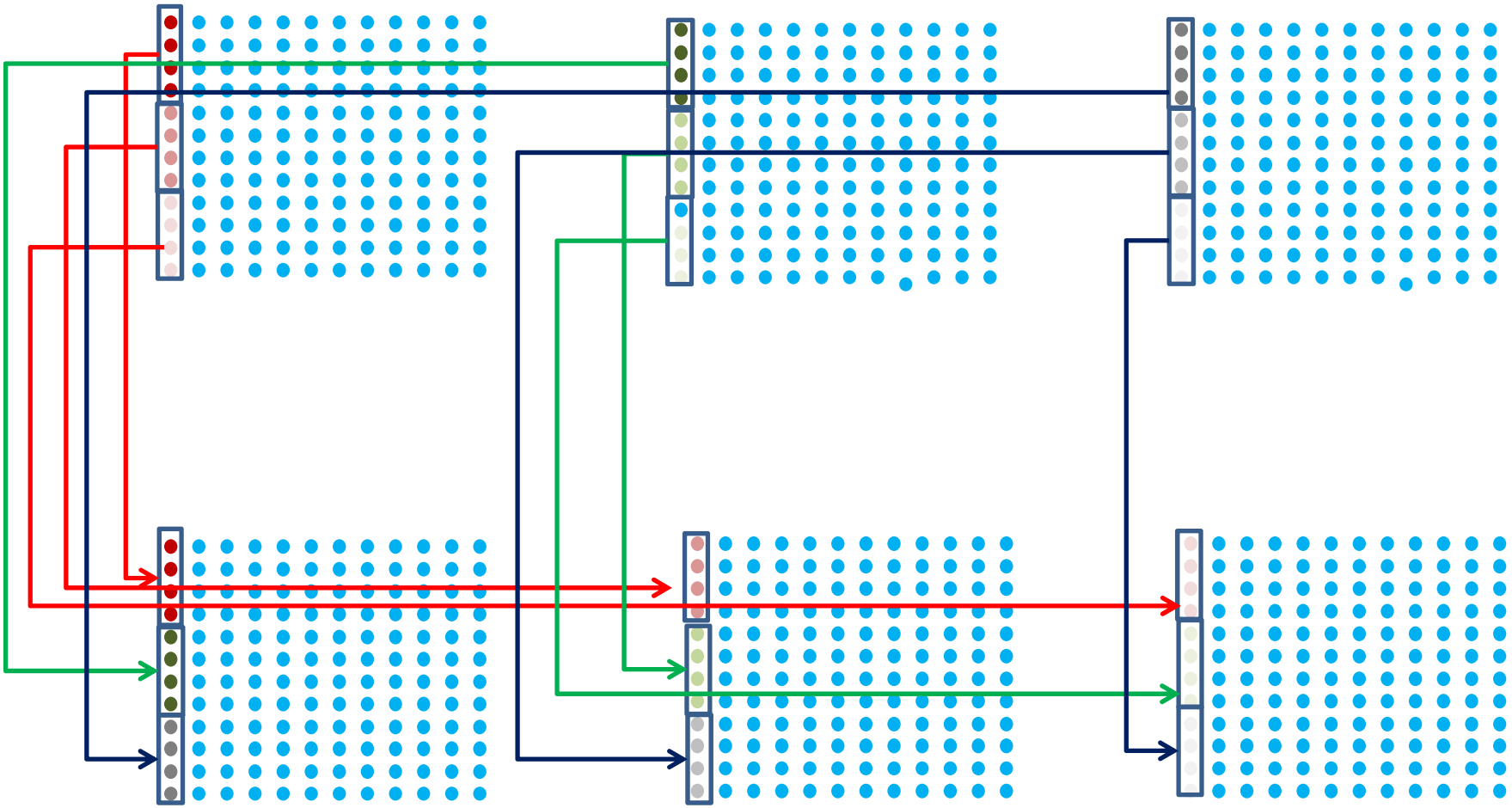
PUSH-ONLY architecture



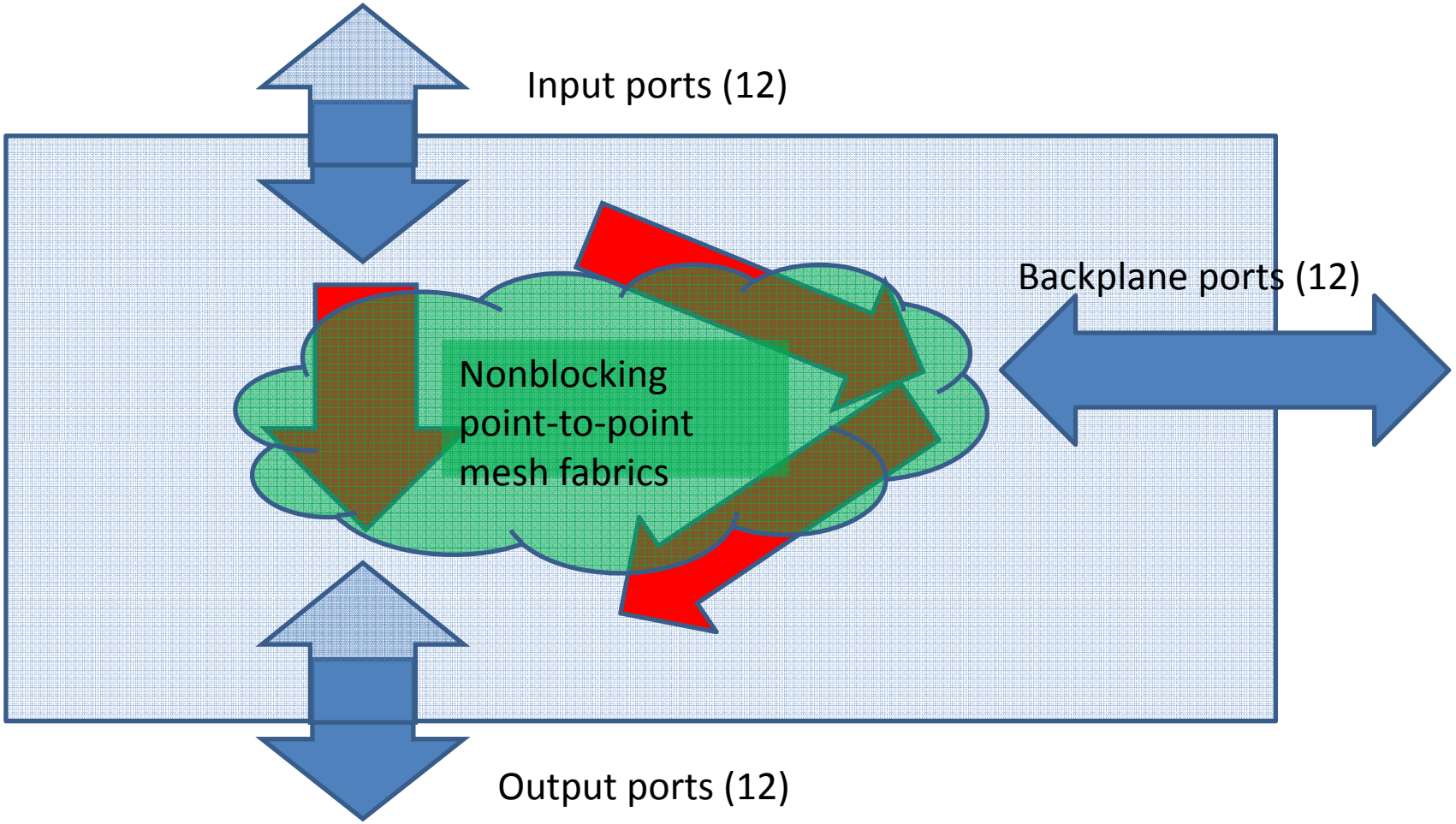
PUSH-ONLY main features

- FEE requires hardware signal (BURST START, BURST END) to tag data.
- Performs PANDA wide BURST BULDING
  - no filtering (target throughput: 100GB/s)
- Based on ATCA standard
  - input: 432 FEE inputs, 36 FEE modules
  - output: 432 CPU outputs, 36 CPU modules
  - internal throughput: >= 2Gbps links

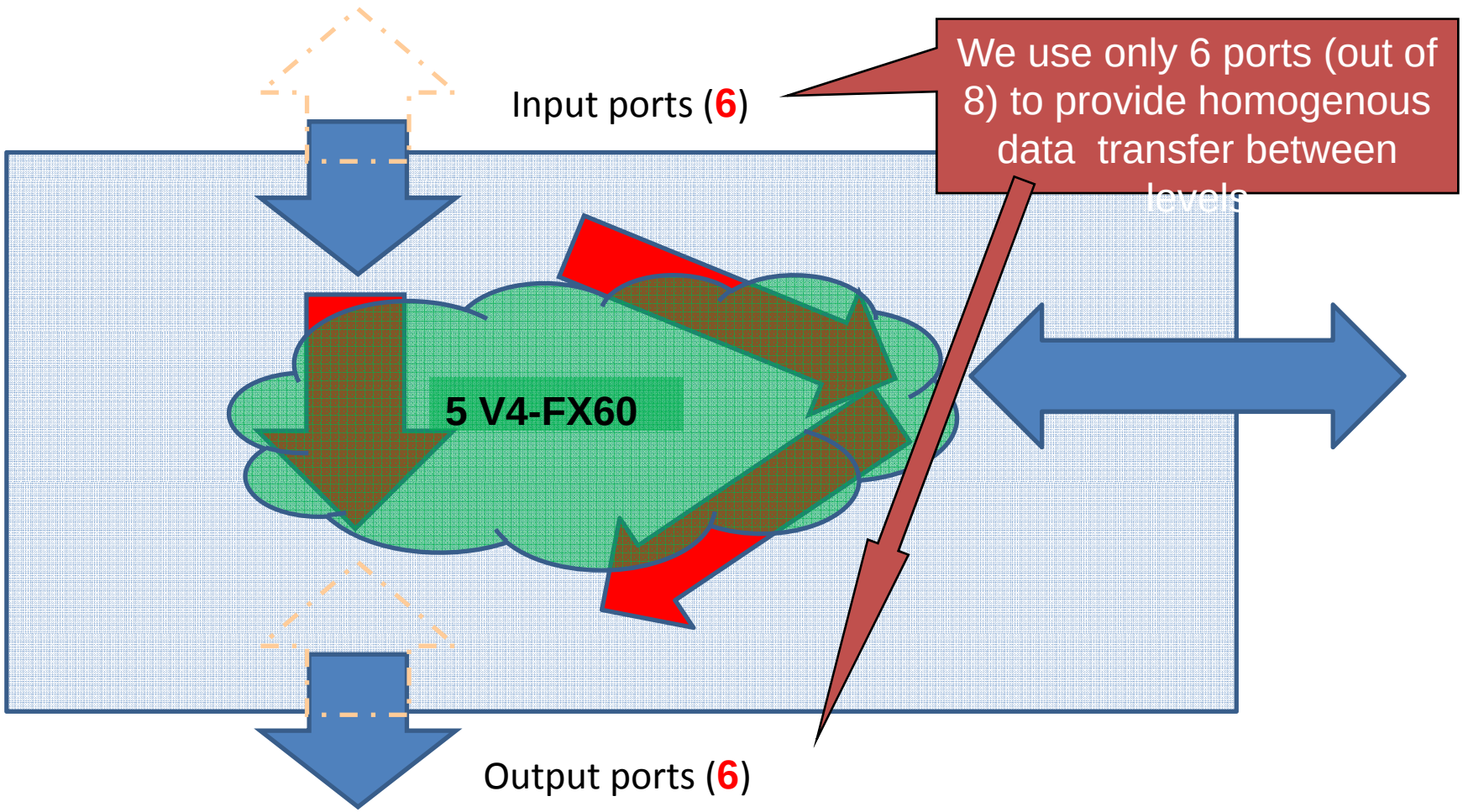
PUSH-ONLY possible wiring



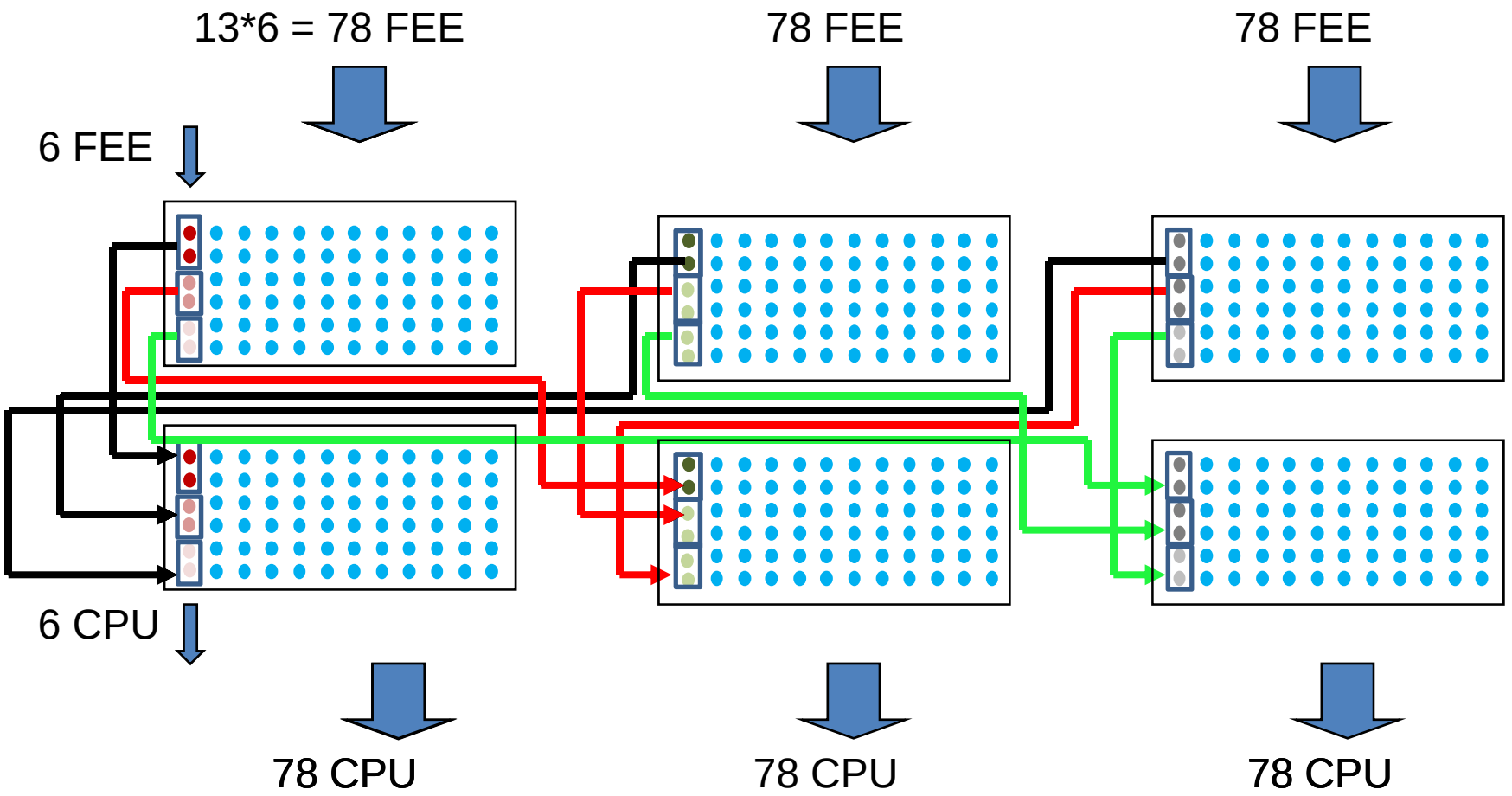
PUSH-ONLY: ATCA module model



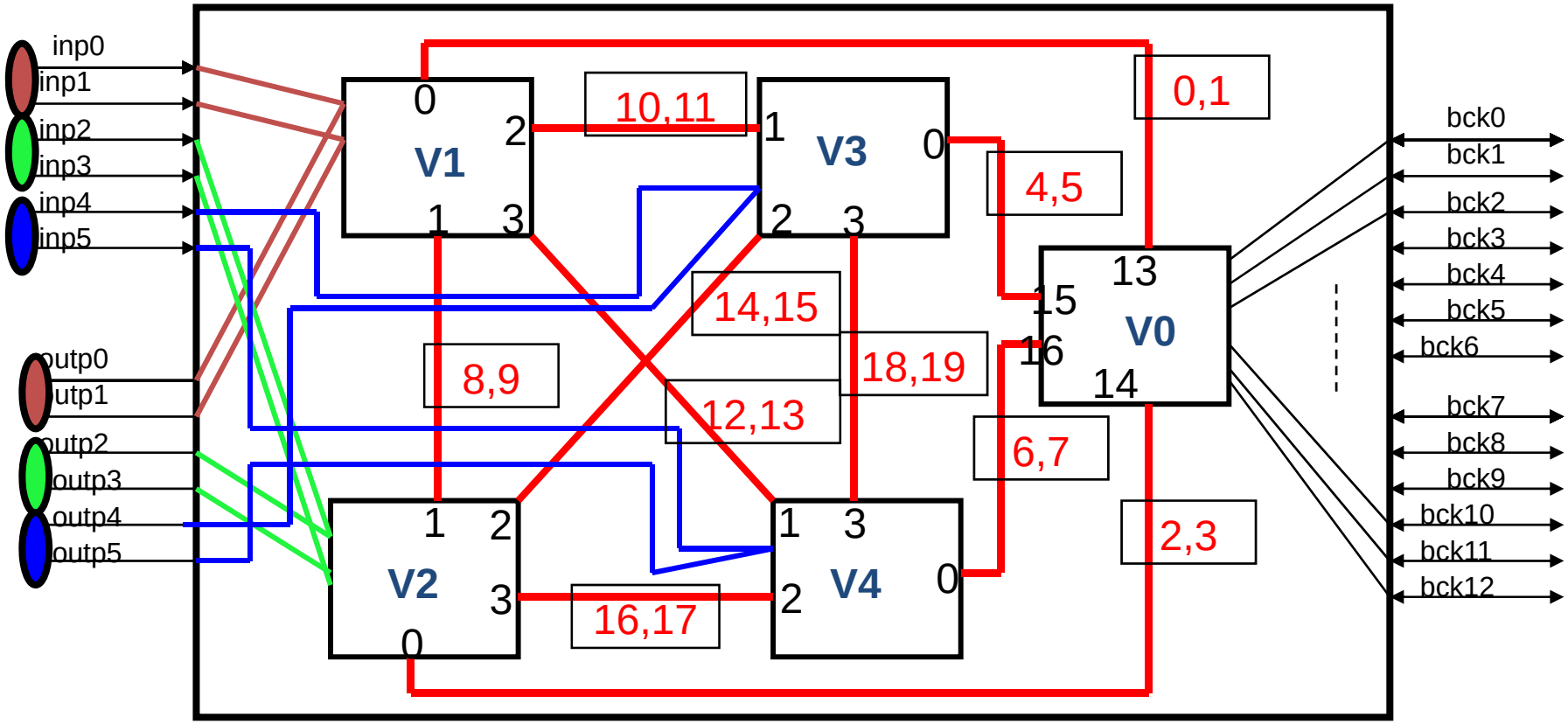
PUSH-ONLY: ComputeNode model



PUSH-ONLY wiring with CN

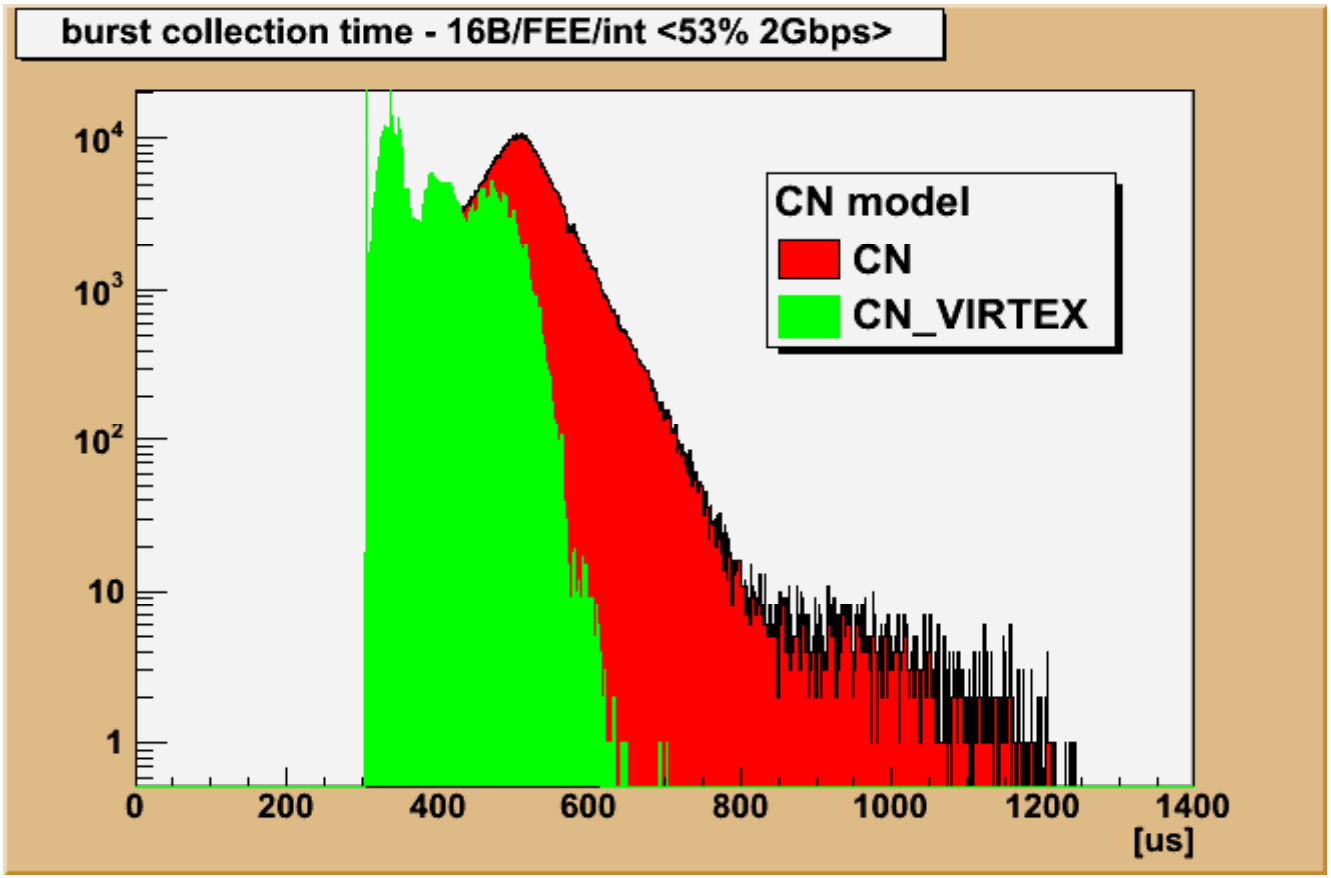


PUSH-ONLY CN internal links



Numbering of Virtexes as original but location changed to simplify wiring diagram

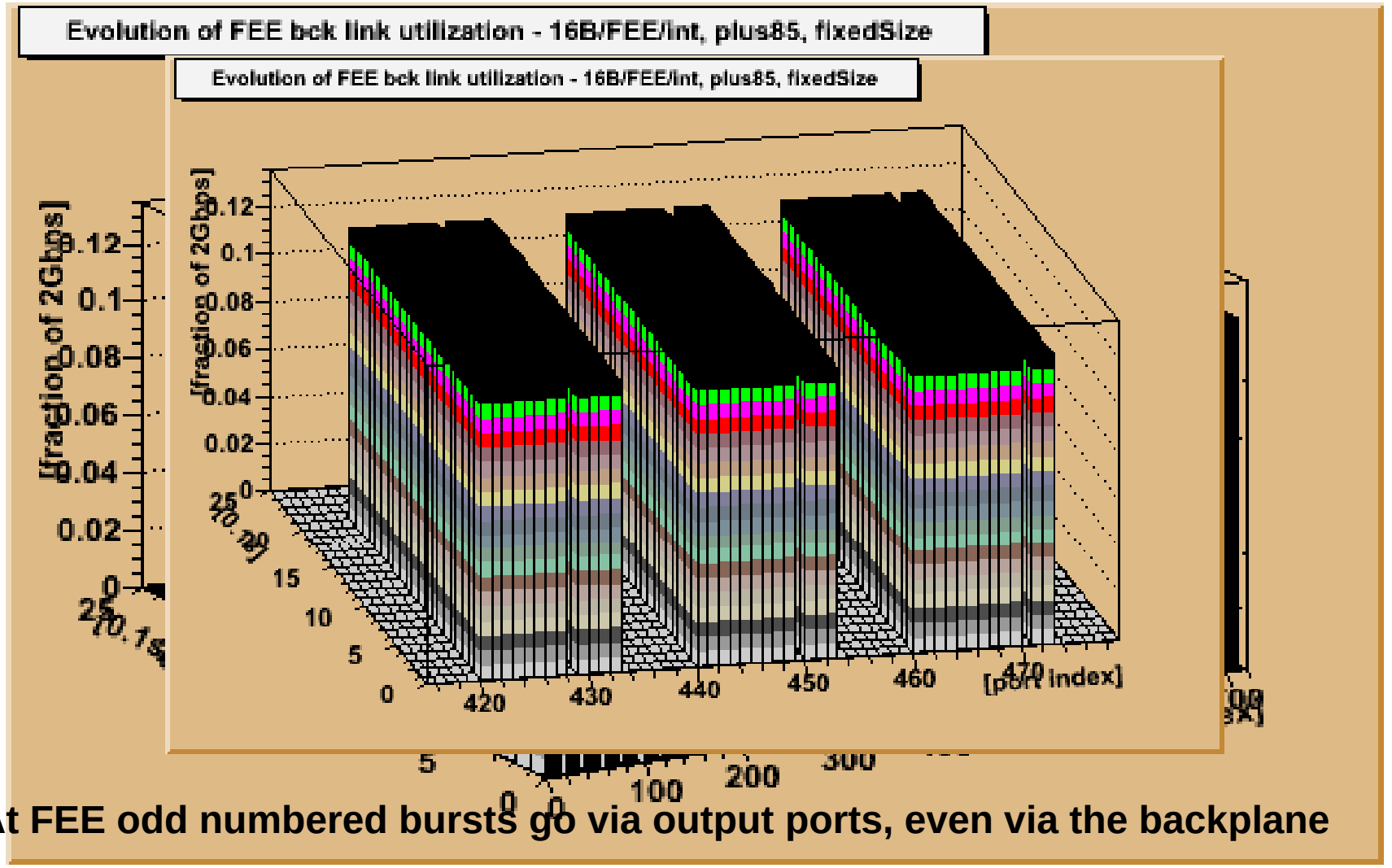
PUSH-ONLY: burst building latency



16 B/FEE/int * 20 interactions * 234 FEE ports = 74880 B / burst

74,9 kB / 2.4 µs = 31,2 GB/s

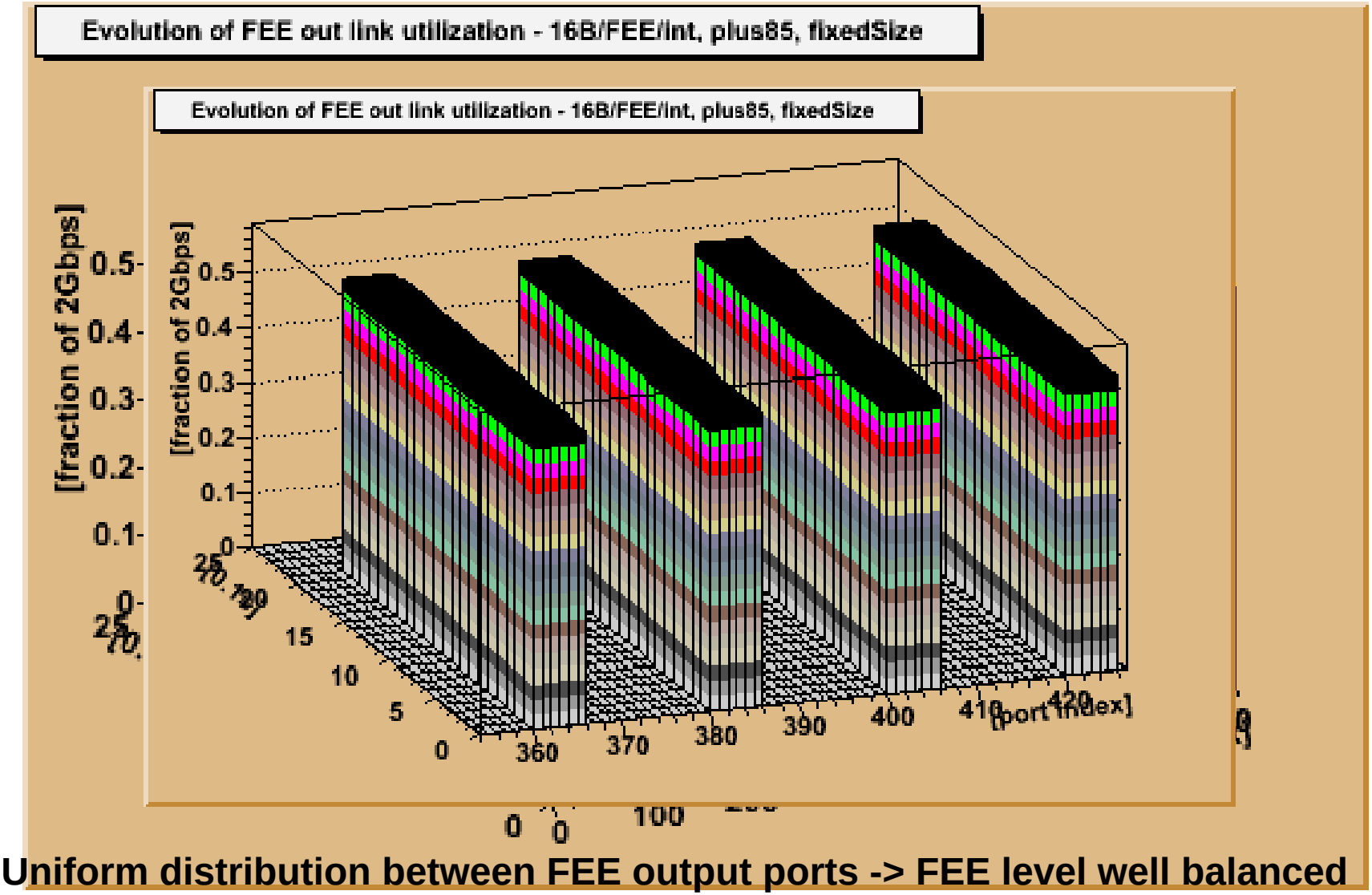
FEE level backplane links utilization



At FEE odd numbered bursts go via output ports, even via the backplane

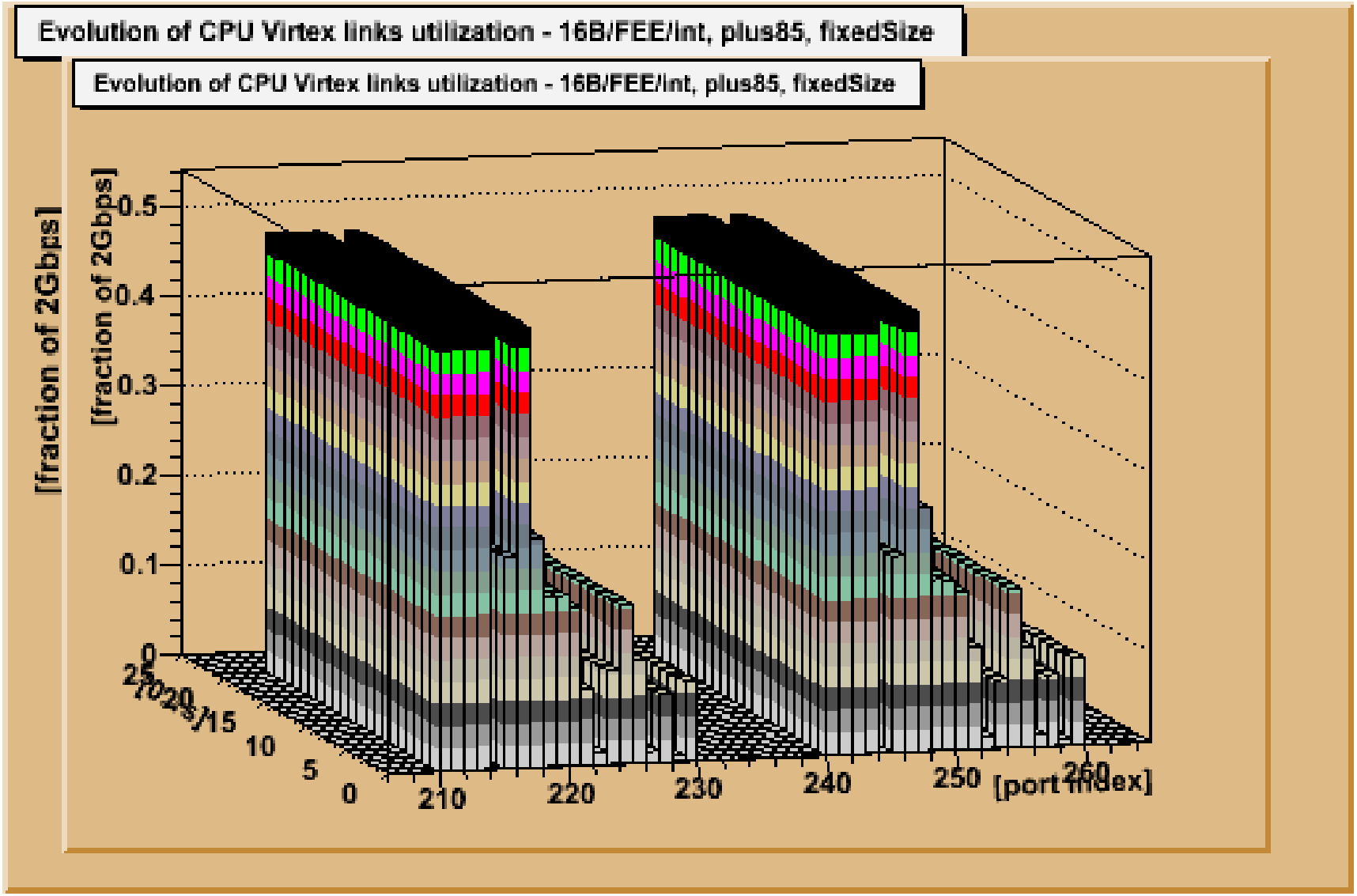
0.53 / 2 (even/odd) = 0.26; 0.26/(12bck/6inp) = 0.13

FEE level output links utilization

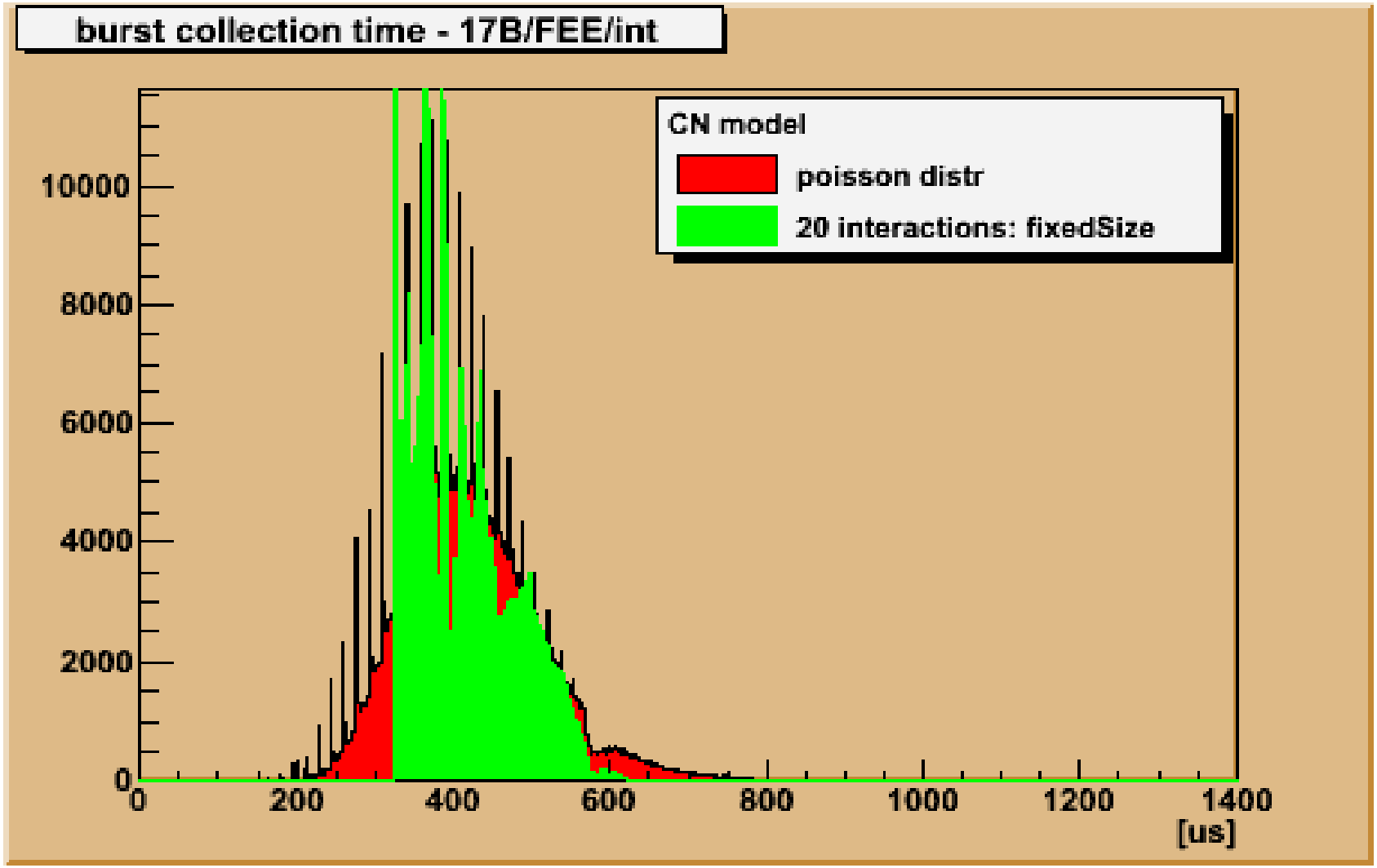


Uniform distribution between FEE output ports -> FEE level well balanced

CPU level Virtex links utilization



Poisson Distr VS fixed size



Conclusions

- Two architecture candidates were investigated and initially simulated

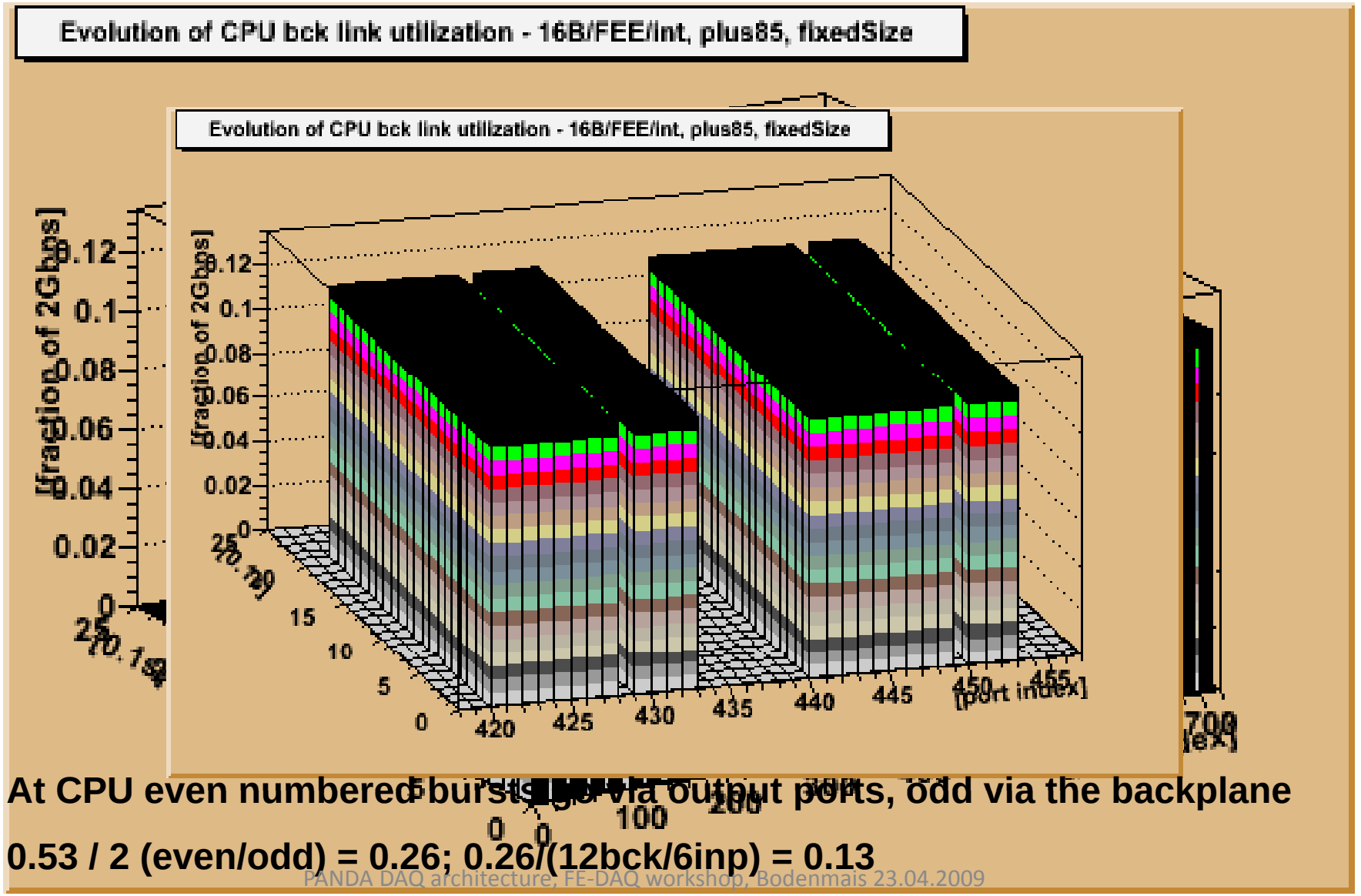
  - PUSH-PULL (burst building + filtering)
    - cheaper (requires smaller resources)
    - depends on filtering efficiency
    - time critical (at L1)
    - L1 filtering decison taken on fragments
    - operates without BURST signal from machine

  - PUSH-ONLY (burst building)
    - more expensive (huge bandwidth installed)
    - offers full flexibility in filtering decisions with access to complete PANDA burst data

Conclusions II

- In order to make simulations more realistic we need more details on FEE from detector groups
  - partitioning
  - fragment size
  - time constraints in producing fragments
  - …

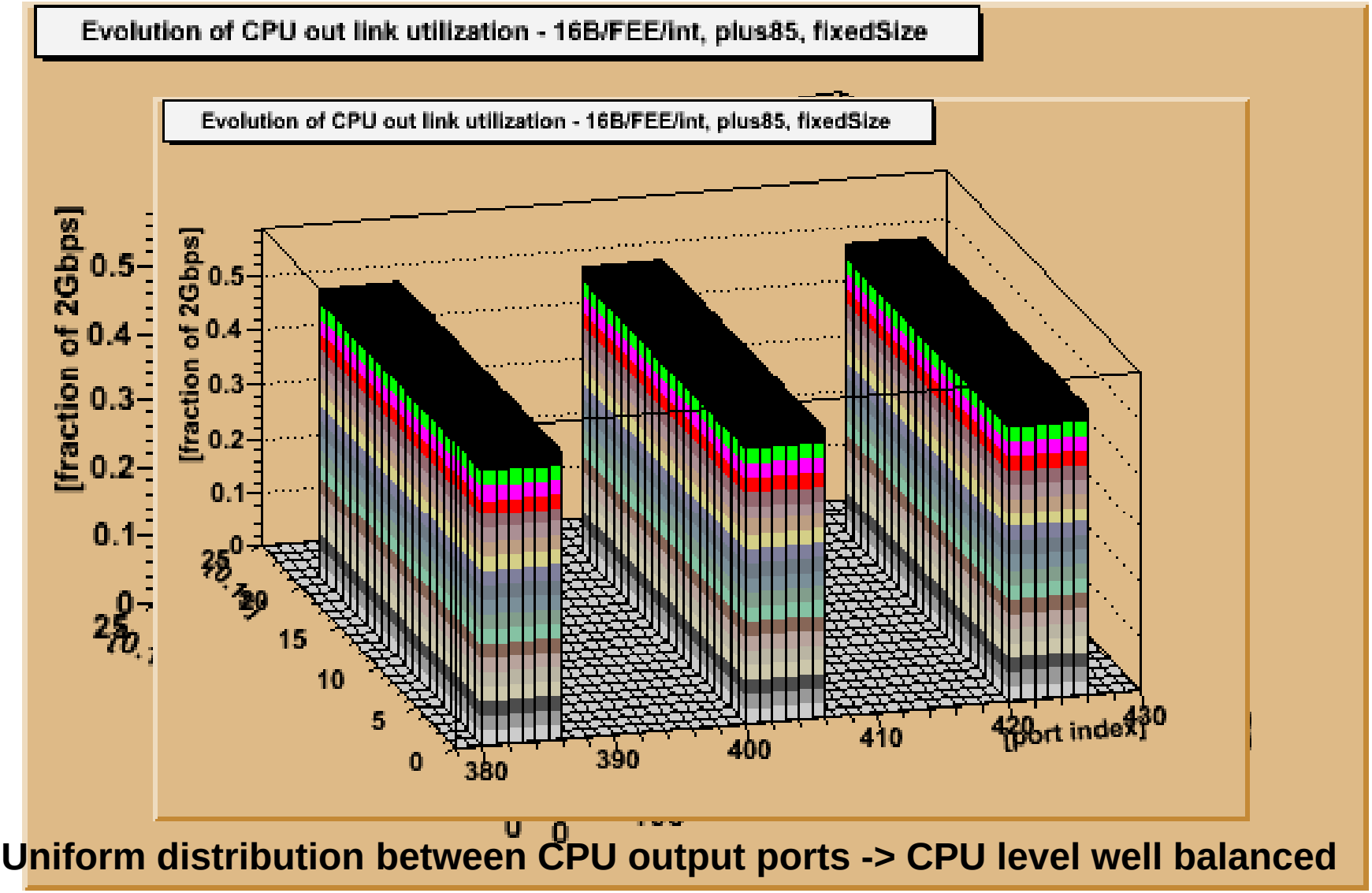
CPU level backplane links utilization



At CPU even numbered bursts, go via output ports, odd via the backplane

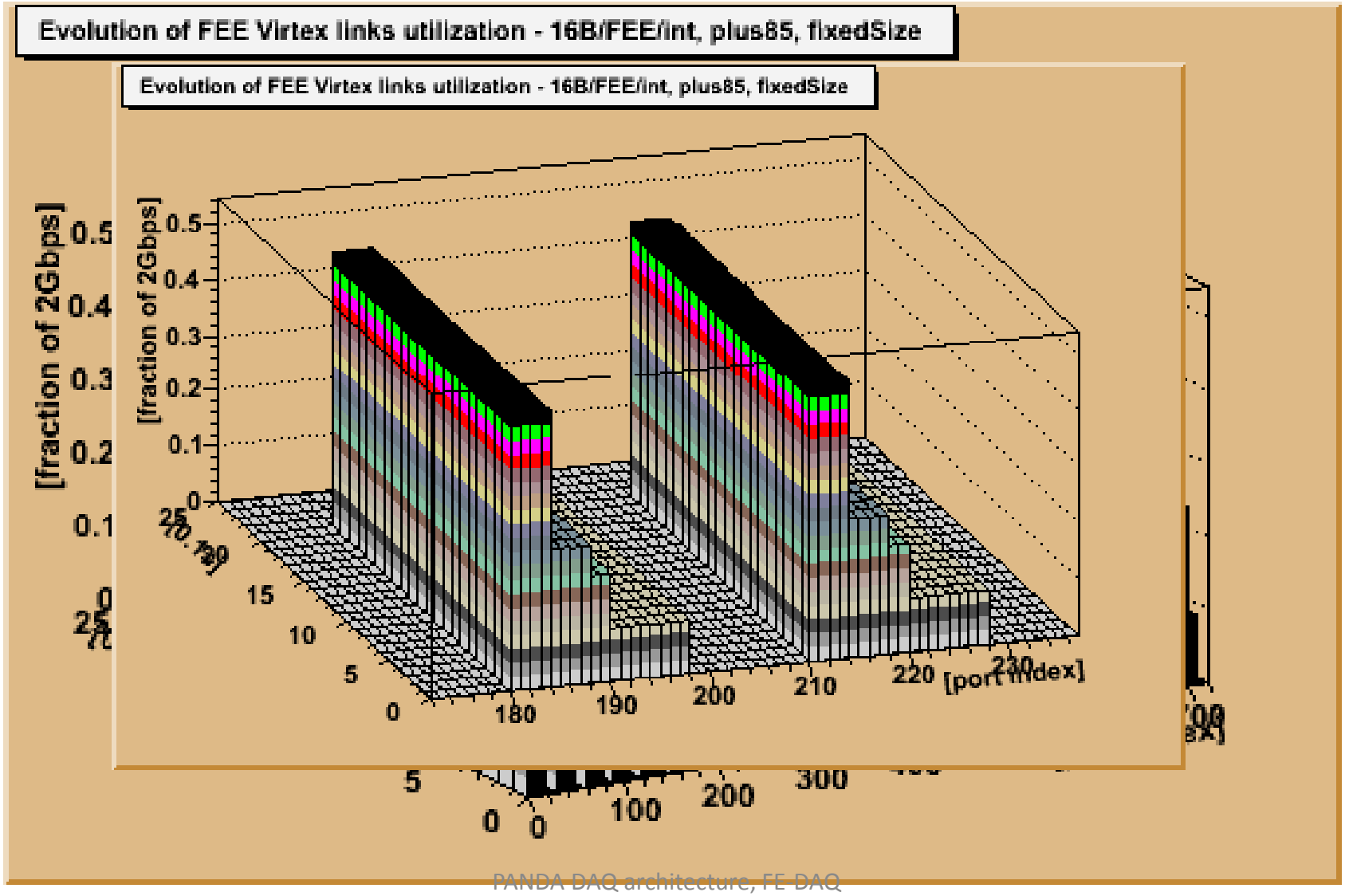
0.53 / 2 (even/odd) = 0.26; 0.26/(12bck/6inp) = 0.13

CPU level output links utilization



Uniform distribution between CPU output ports -> CPU level well balanced

FEE level Virtex links utilization



PUSH-PULL architecture