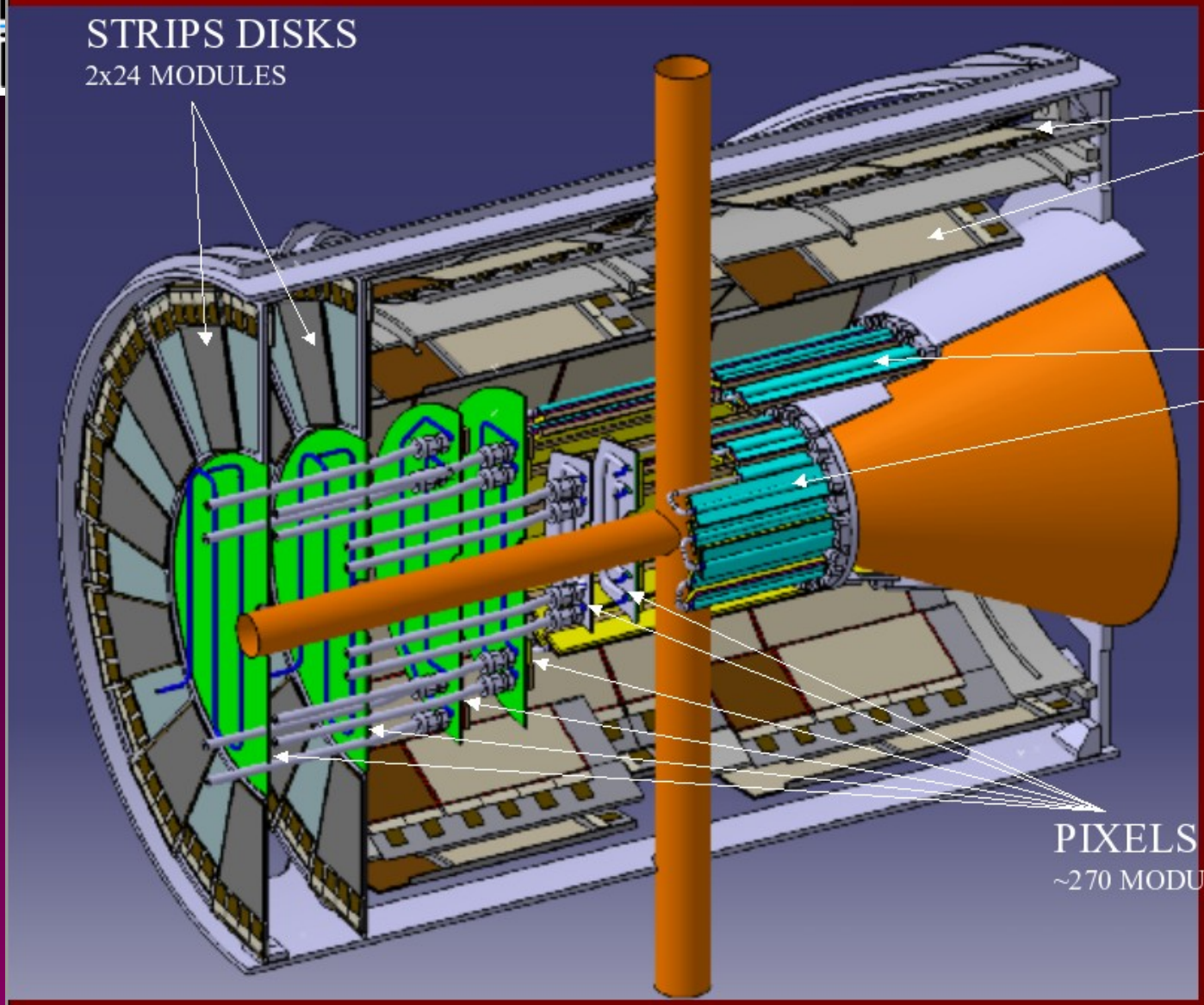
PANDA FE-DAQ Workshop

Sezione di Torino

MVD detector requirements and architecture

UPDATED 3D MVD MODEL (5/12/2008)



G. GIRAUDO

PANDA MEETING 8-12/12/2008 DARMSTADT

Pixel performances - 1

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Parameter	Current value	Other proposal	Status
Pixel size	100 µm × 100 µm	50 µm × 200 µm	To be fixed
Chip active area	10 mm × 10 mm	11.4 mm × 11.6 mm	To be fixed
dE/dx method	Time over Threshold		Fixed
Max input charge	100 fC		Fixed
Clock	50 MHz	100 MHz	To be fixed
Time resolution	5.77 ns rms @ 50 MHz	2.88 ns rms @ 100 MHz	To be fixed
Max event rate	12.3 MHz/cm^2	Ongoing simulations	To be fixed
Data rate per chip	615 Mb/s	815 Mb/s	To be fixed

Pixel performances - 2

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Parameter	Current value	Other proposal	Status
Analog gain	40 mV/fC		~ Fixed
ToT gain	180 ns/fC	90 ns/fC	To be fixed
Max ToT	18 µs	9 µs	To be fixed
Signal polarity	Either n or p		Fixed
Analogue noise	0.032 fC (200 e-)		~ Fixed
Quantization noise	0.032 fC (200 e-)		~ Fixed
Sensor leakage current	< 50 nA/pixel		
Power consumption	< 750 mW/cm^2	< 500 mW/cm^2	To be fixed

Pixel performances - 3

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Parameter	Current value	Other proposal	Status
Total Ionizing Dose (PANDA lifetime)	10 Mrad		To be confirmed
Neutron fluence (PANDA lifetime)	$5 \cdot 10^{14}$ 1MeV n_{EQ}/cm^2		To be confirmed
LET threshold			To be defined
SEU saturation cross section			To be defined

Design considerations

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Mechanical design and physical simulations still ongoing; many specifications still to be fixed

Stringent constraints for space and power

From current design ~450 F/E chips in the barrel and ~470 in the disks.

From current simulations the total amount of data is ~50 Gb/s

Very inhomogeneous event density will lead to a sub-optimal bandwidth occupation

Strip performances - 1

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Parameter	Value	Remarks
Input compliance		
sensor capacitance, full depletion	< 10 pF	rect. short strips
	< 50 pF	rect. long strips + ganging
	< 20 pF	forward disk strips
charge polarity	either	selectable via slow control
input ENC	< 800 e^-	C_{Sensor} = 10 pF
	< 1100 e^-	C_{Sensor} = 25 pF

Strip performances - 2

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Parameter	Value	Remarks
	Signal	
dynamic range	160 ke$^-$	24000 e$^-$ MIPs in 300 µm silicon, guaranteed within liftime
min. SNR for MIPs	12	
peaking time	≈5 .. 25 ns	typical Si drift time
digitization resolution	≥ 8 bits	
	Power	
Overall power consumption	< 1 W	Assuming 128 channels F/E

Strip performances - 3

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Parameter	Value	Remarks
	Dynamic	
trigger	internally generated	when charge pulse exceeds adjustable threshold level
time stamp resolution	< 20 ns	
dead time / ch	< 6 μs	
overshoot recovery time/ch	< 25 μs	baseline restored to within 1% of equilibrium

Strip performances - 4

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Parameter	Value	Remarks
Dynamic		
average hit rates/ch		simulations @15 GeV beam momentum
hot spots	9000 s^{-1}	pbar-p
	40000 s^{-1}	pbar-Au
average occupancy	6000 s^{-1}	pbar-p
	30000 s^{-1}	pbar-Au
Interface		
Slow control	Any	
Data	Sparsified digital	

Readout scheme - - first ideas

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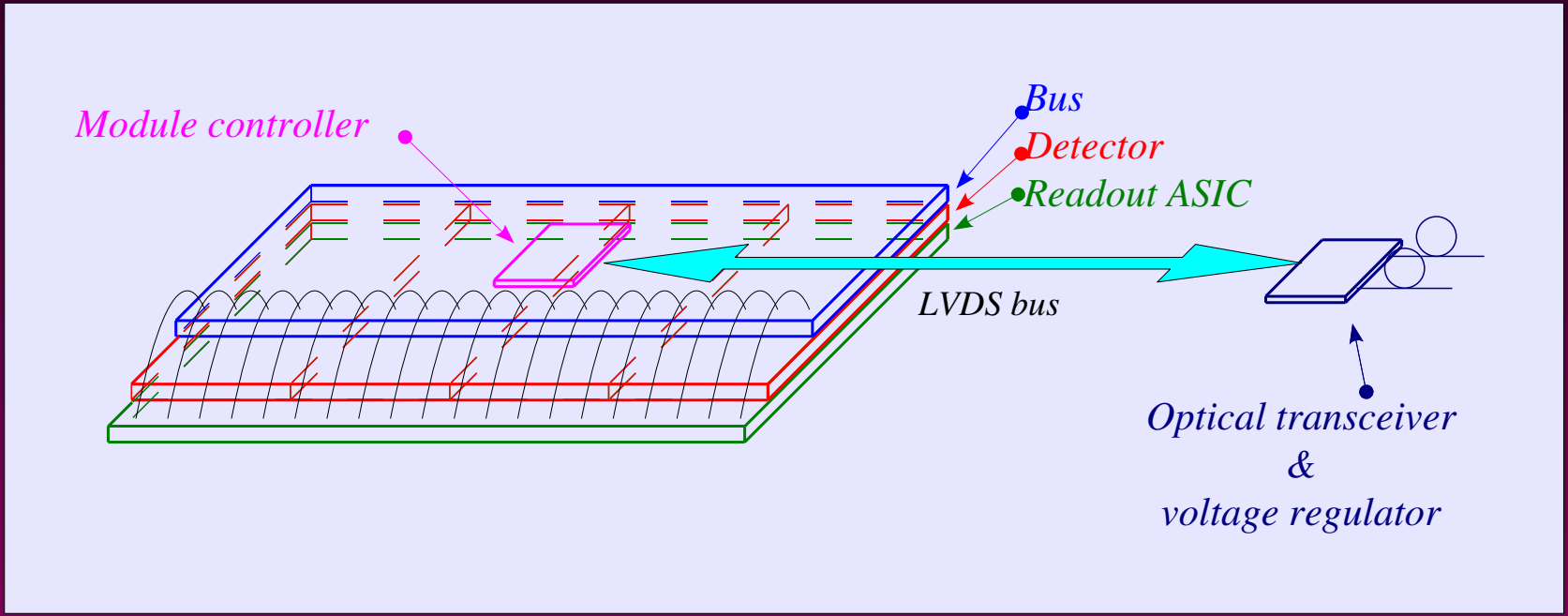

Readout concept - 1

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Modules with different size required (2,4,5 and 6 F/E chips)

1 controller per 2-3 F/E chips

Custom F/E and controller ASICs development in CMOS 0.13 μm technology

Radiation tolerance issues

Voltage regulation and electrical to optical conversion as close as possible to the F/E

Readout concept - 2

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The cabling of the disks is extremely difficult...

...cables have to forward in order not to interfere with the strip detector...

...and then backward to the only accessible side

Optical transceivers will probably require radiation tolerance → we are looking at solutions in the HEP community (CERN's GOL, GBT13)

Data transmission

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- ToPiX to module controller : up to 5 × 200 Mb/s electrical links
- 2 or 3 ToPiX chips per module controller
- Module controller to service board : up to 2 × 1 Gb/s electrical links
- Module controllers can be chained
- Up to 6 F/E ASICs per service board
- Service board to counting room : 3.2 Gb/s optical link

Strip design parameters

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DSSD – Sensor Sizes :

rectangular 6×3 cm^2, 0.13 mm pitch, 6 FEs

rectangular 3×3 cm^2, 0.13 mm pitch, 4 FEs

trapezoidal, 6×3.6 cm^2, 15°, 0.07 mm pitch, 8 FEs

different module size (1/2/3 sensors)

total ~1600 F/E, 200 kChannels

~6 MHz maximum hit rate per FE

Data rate 240 Mb/s per FE

The ToPiX ASIC

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Custom development for the PANDA MVD

Provides spatial and time coordinates plus energy resolution measurement (via ToT)

Compatible either with p-type or n-type detectors

Self triggered architecture

Each event has a 12 bits time reference

Data corresponding to a 12 bits counter cycle (40.96 µs) are packed in a frame, with a 16 bits frame counter (2.68 s cycle)

ToPiX prototype

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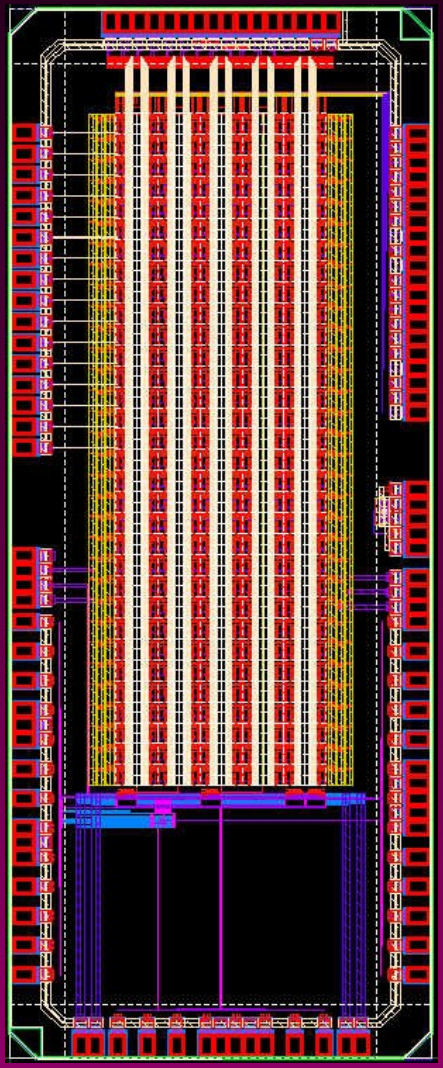

Full pixel cell (analogue + digital)

Two folded columns with 128 cells

Two columns with 32 cells

5x2 mm^2 die area

CMOS 0.13 µm technology

D. Calvo, T. Kugathasan, G. Mazza, M. Mignone, A. Rivetti, T. Stockmanns and R. Wheadon

A Silicon Pixel Readout ASIC in CMOS 0.13 µm for the PANDA MicroVertex Detector

Nuclear Science Symposium Conference Record, 2008 IEEE, 19-25 Oct. 2008 Page(s): 2934 – 2939

Data format

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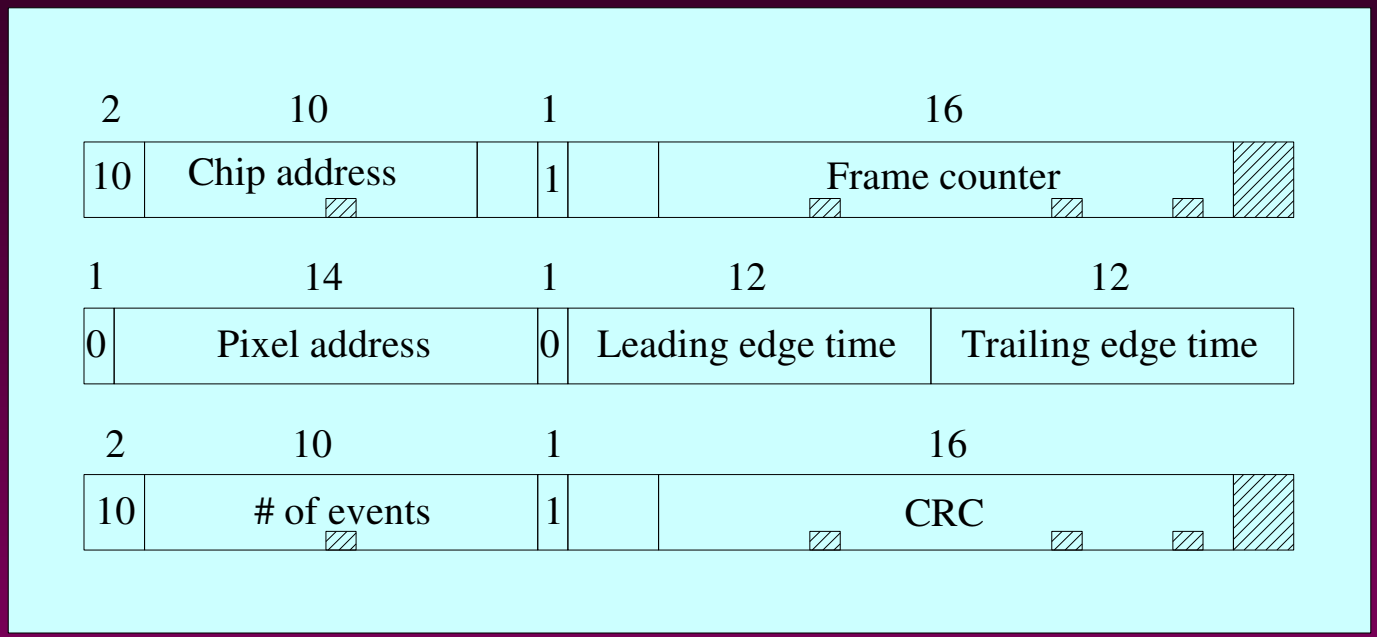

Header

Data packet

Trailer

Strip front-end

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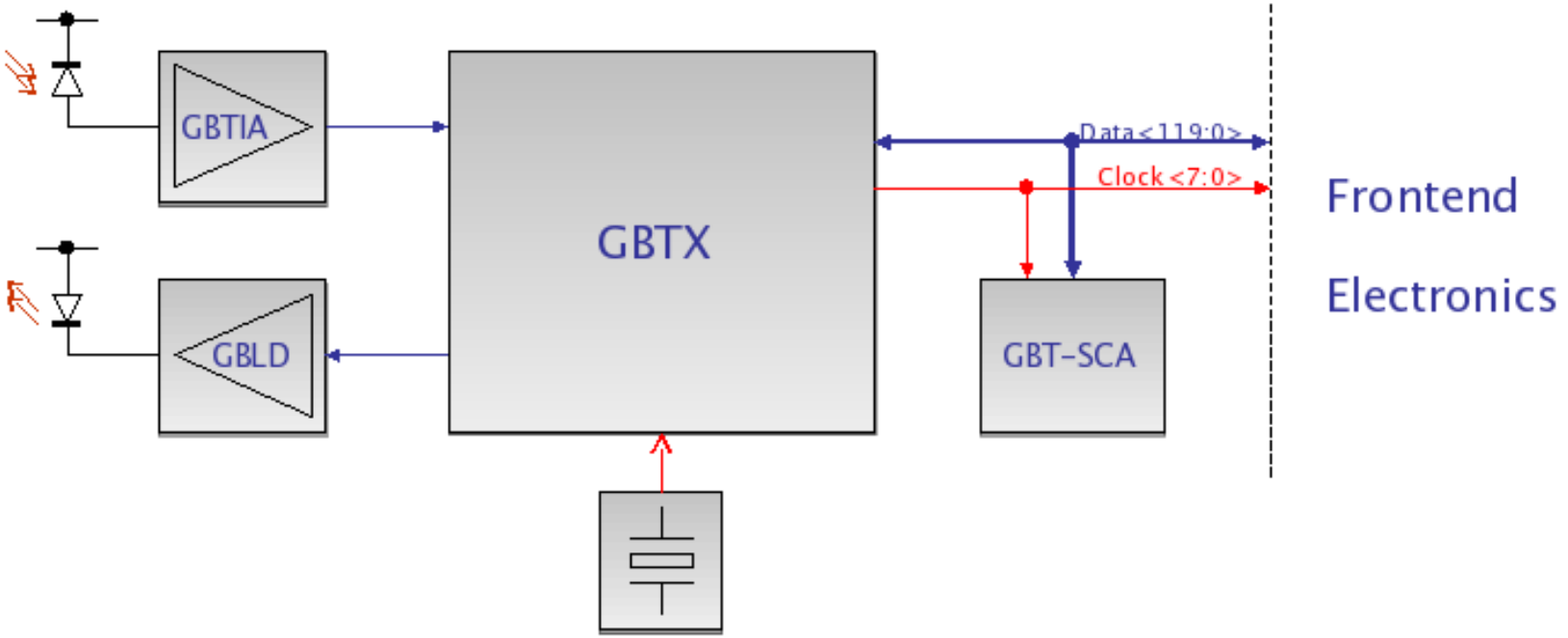
target front-end : CBM-XYTER ASIC developed at GSI

Development not fixed yet; digital interface not defined so far

but : PANDA specific design parameters regarded by designers

GBT Chipset

- *Radiation tolerant chipset:*
  - GBTIA: Transimpedance optical receiver
  - GBLD: Laser driver
  - GBTX: Data and timing and transceiver
  - GBT-SCA: Slow control ASIC
- *Supports:*
  - Bidirectional data transmission
  - Bandwidth:
    - Line rate: 4.8 Gb/s
    - Effective: 3.36 Gb/s
- *The target applications are:*
  - Data readout
  - TTC
  - Slow control and monitoring links.
- *Radiation tolerance:*
  - Total dose
  - Single Event Upsets



GBT13 data format

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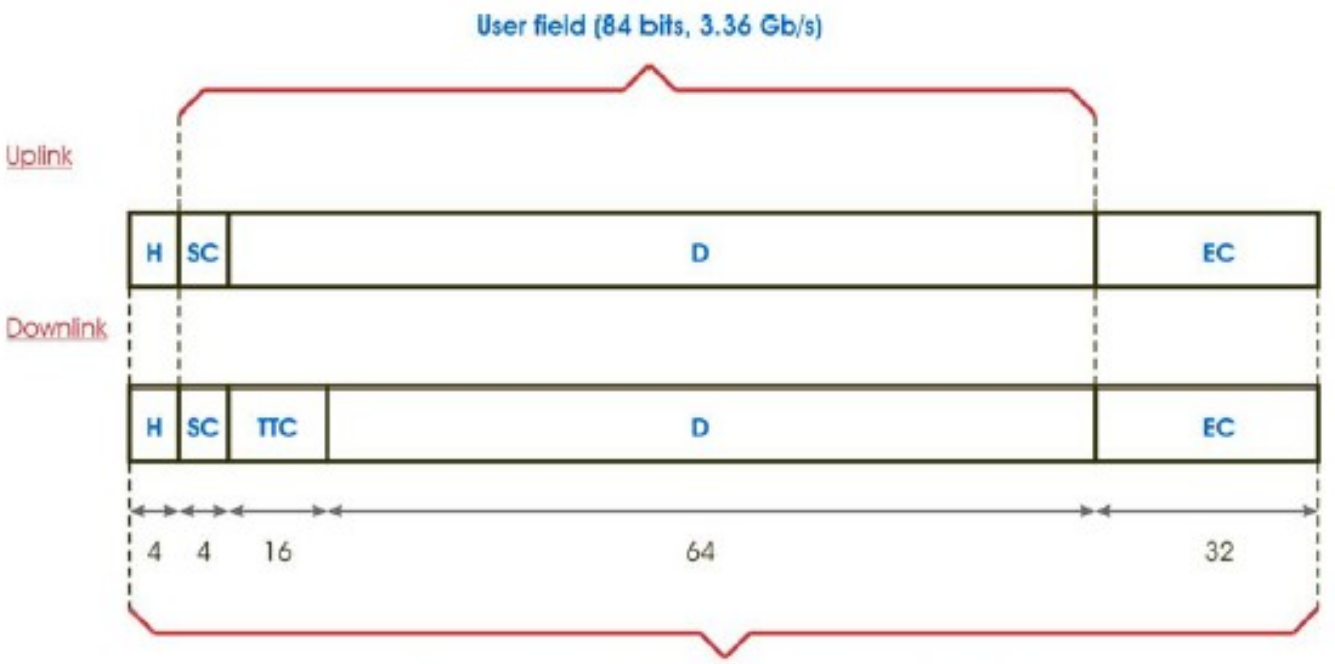
2.1 Frame structure



Frame: 1 SLHC Clock Cycle (120 bits, 4.8 Gb/s)

H - Header

SC - Slow Control (160 Mb/s)

TTC - Timing Trigger and Control (640 Mb/s)

D - Data (2.56 Gb/s)

EC - Error correction

Data processing

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On the front-end

gain and threshold calibration

inherent zero suppression

Low level data processing foreseen for :

Time Ordering (interface panel / counting room?)

Clustering (interface panel)

Tracking/Vertexing (compute node)

DCS

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Monitor :

- Sensor voltages and currents
- ASICs voltages, currents
- F/E temperature (on chip sensors ?)
- cooling system temperature and pressure
- Mechanical deformation ?

Calibration :

- gain, threshold

Conclusions

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MVD design ongoing; some specs still to be fixed

Very tight space and power constraints; cable routing is a real nightmare !

Custom ASICs for the pixel F/E (ToPiX) and the module controller under development in Torino. Reduced scale prototype successfully tested; new version foreseen for 4Q2009

Custom ASICs for the strip F/E (NXYTER) under development at GSI

Looking for common solutions for the optical links