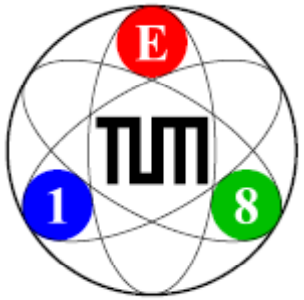


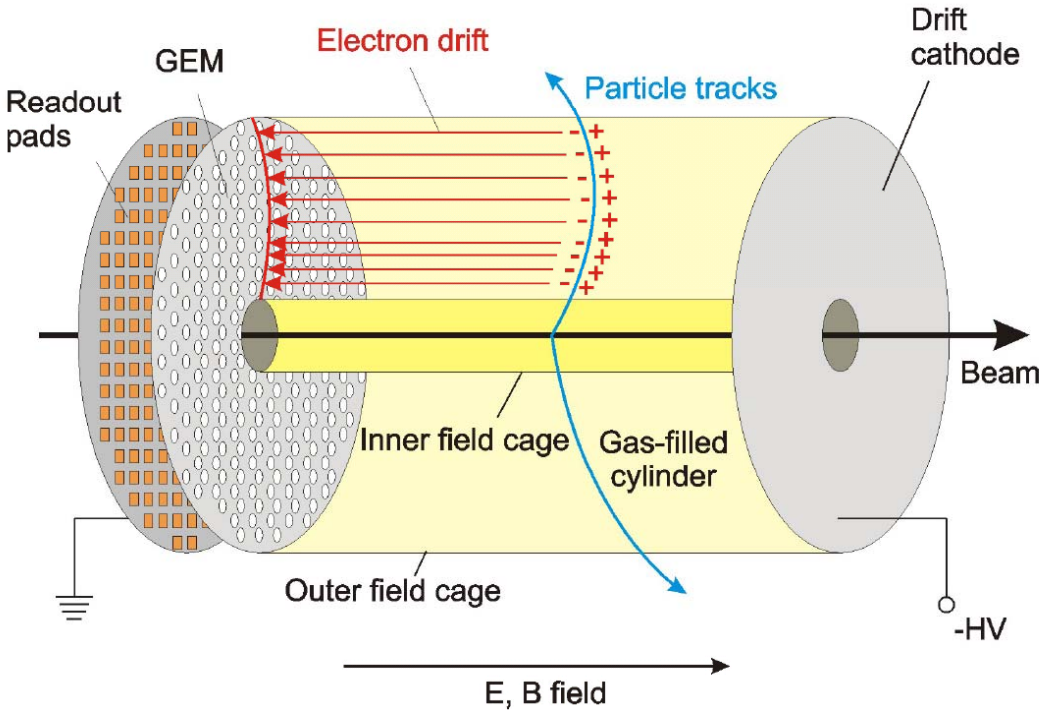
Front-end electronics for Time Projection Chamber

I.Konorov

Outlook:

- TPC requirements
- TPC readout options
- Options for TPC FE chips
- Prototype TPC readout system

Time Projection Chamber



TPC@PANDA:

- no gating
- no triggering
- Hexagon pads Ø 3 mm
- 60 000 channels
- 100-250 kHz hit rate/pad @10^7

Extracted information:

- X, Y coordinates
- T -> Z coordinate
- dE/dX

Requirements for FEE:

- Noise 500 e- - low ion feedback
- Amplitude resolution 8 bits
- Time resolution 3-5 ns
- Double cluster resolution 200 ns
- Self triggering FEE
- Radiation tolerant electronics

Readout options for PANDA TPC

Options:

- N-xyter ASIC
- Super ALTRO
- Hit detection ASIC
- AFTER ASIC – only for TPC prototype

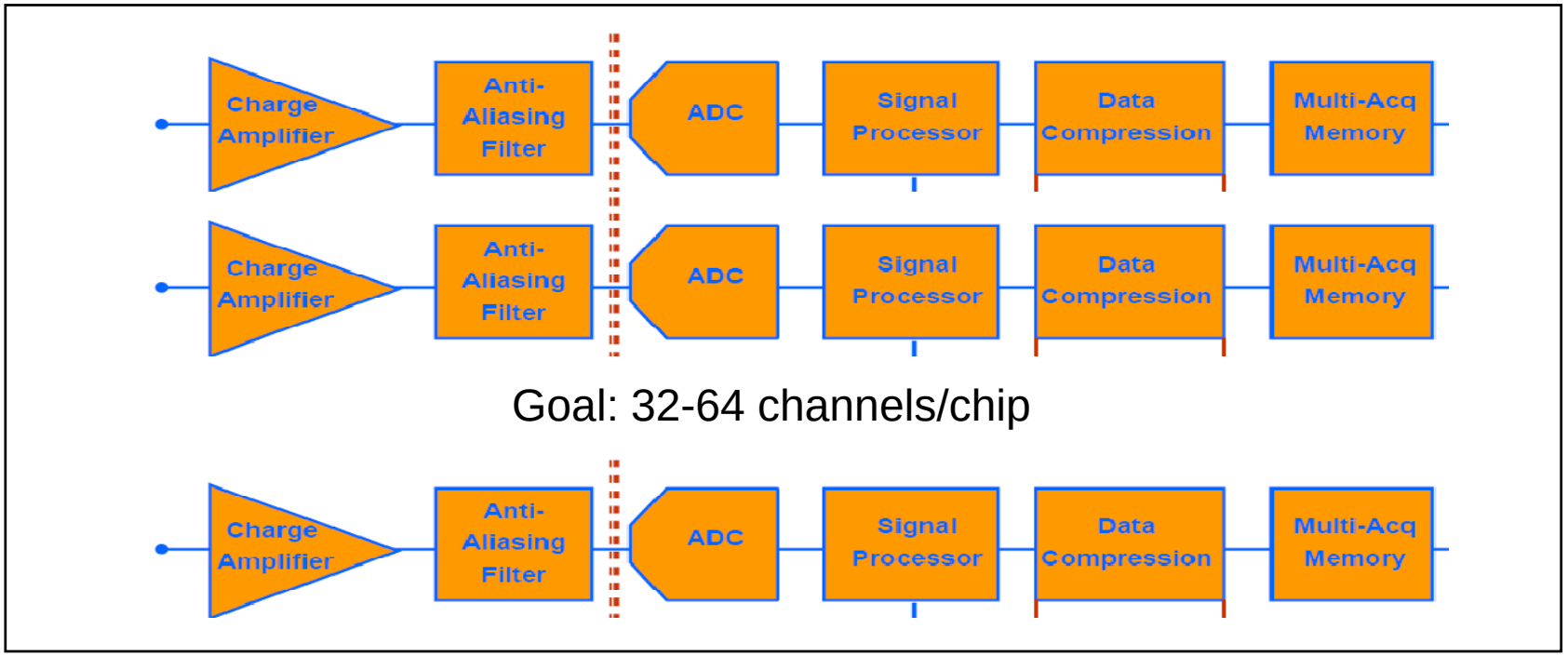
SUPER ALTRO readout architecture

Advantage:

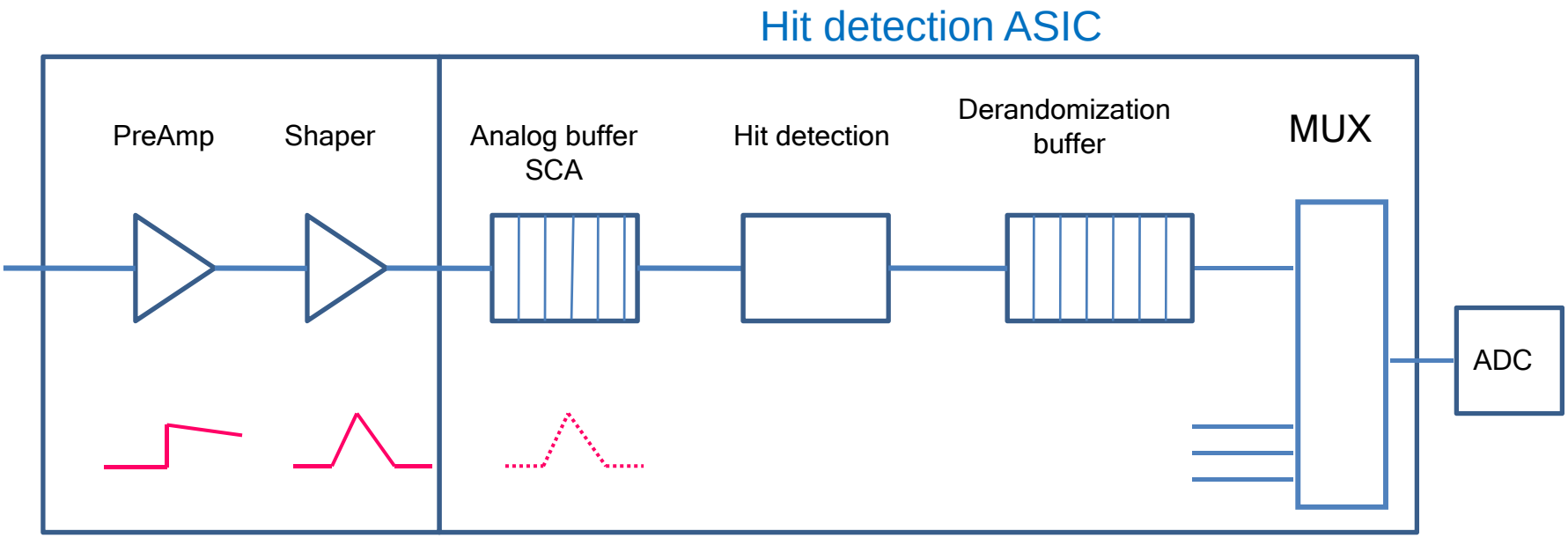
- Complete signal shape information
- Best quality feature extraction : Amplitude and Time
- Advanced da
  - Common mode noise correction
  - Pile up detectio

Disadvantage:

- Low density
- High power consumption
  - SUPER ALTRO 32mW/channel @40Mhz
- Expansive



Optimized readout architecture analog zero suppression



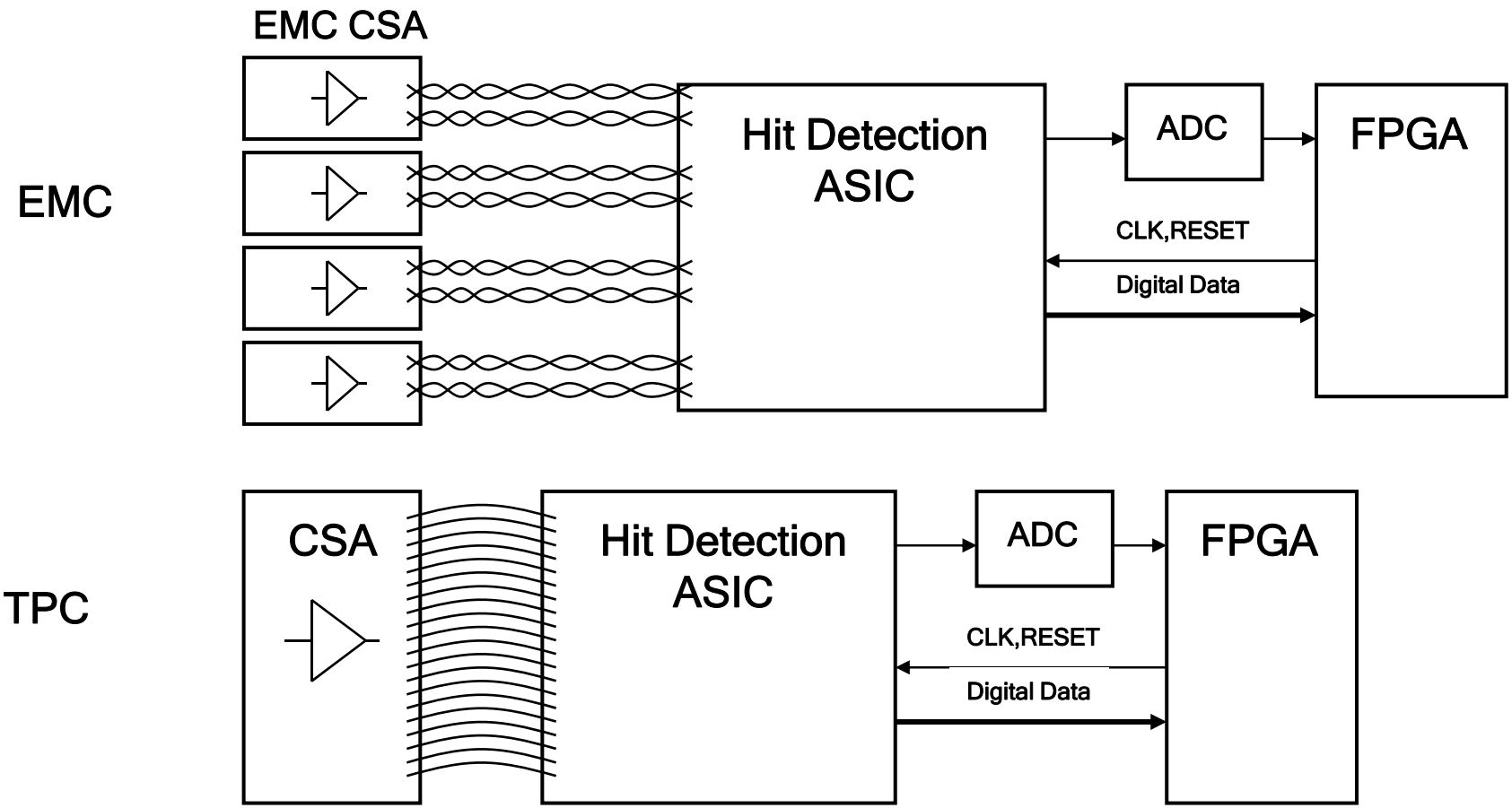
Advantages:

- low cost per channel
- low power
- many applications

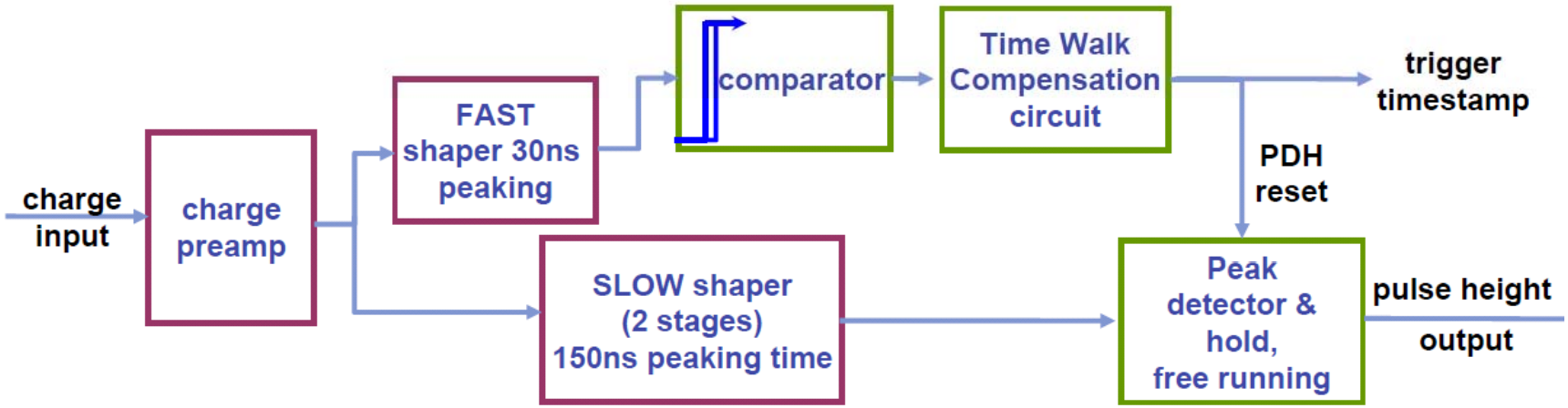
SCA Clock : 40 MHz - TPC, EMC, Silicon
100 MHz - Straw, Muon
200 MHz - Barrel DIRC, Forward

EMC

Read out scheme



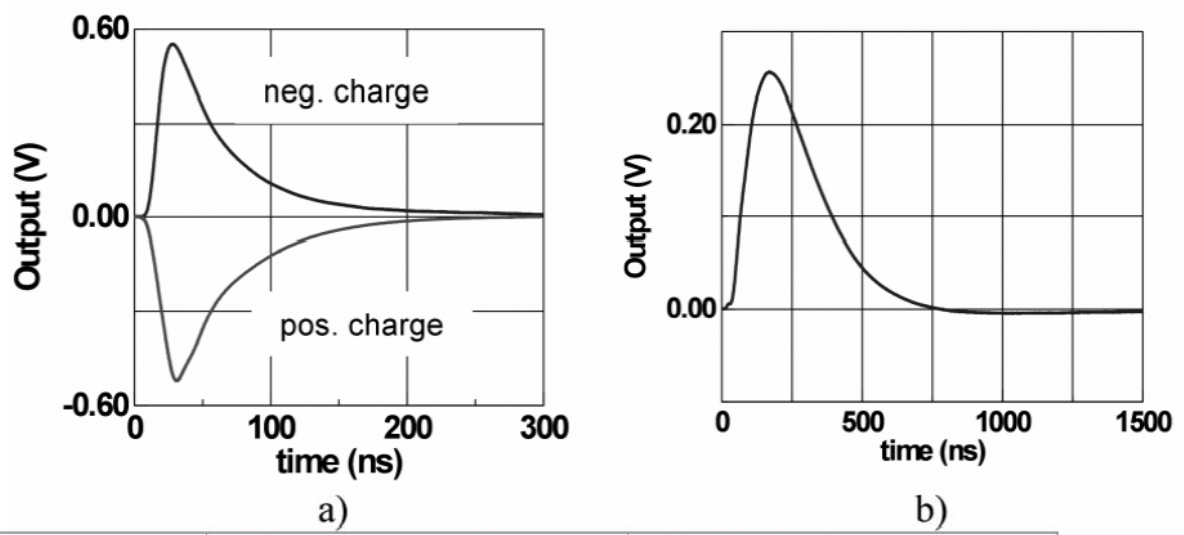
N-XYTER ASIC



Features:

- Self triggering , hit rate upto160kHz/channel
- Charge sensitive amplifier, peak detector
- Time stamping with 1 ns LSB, 2ns resolution
- Hit information: Amplitude(analog) + Time(digital)
- Derandomizer buffer for 4 hits
- 128 channels
- 128:1 multiplexer , 32MHz readout
- 13 mW/channel

N-XYTER expected performance



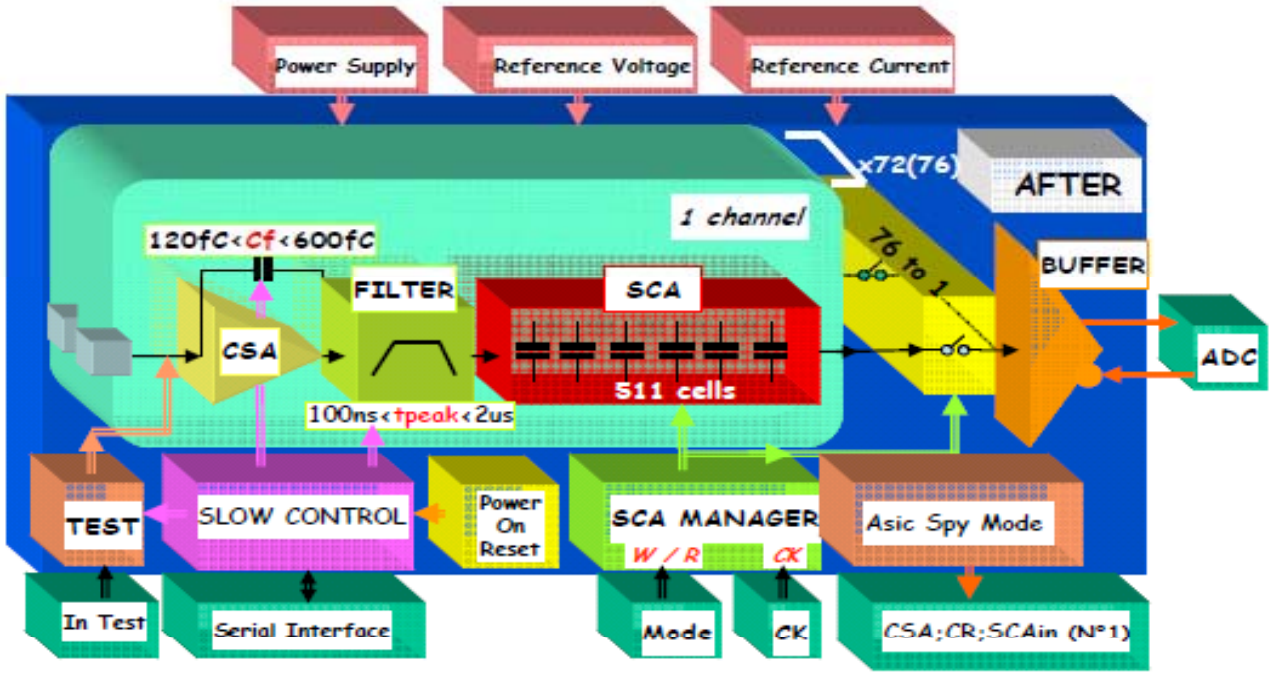
	FAST channel	SLOW channel
ENC	26.9 e/pF + 200 e	12.7 e/pF + 233 e
peaking time[a] (1% to 99%)	18.5 ns	139 ns

Engineered for 30 pF, giving 1000 e 600 e

Performance parameters are not confirmed yet!

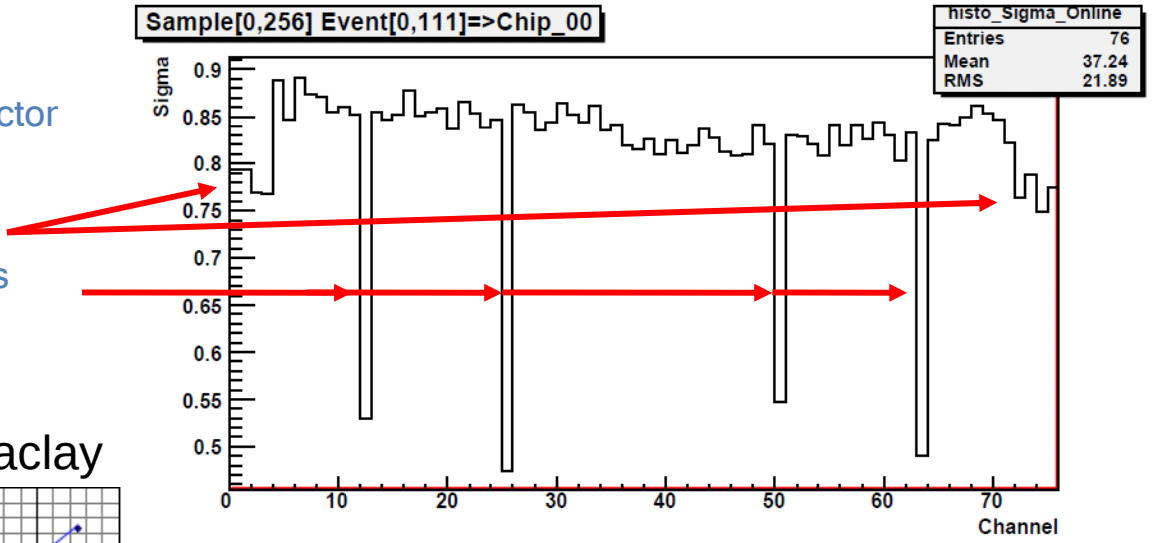
AFTER chip block diagram

- developed by Saclay for T2K experiment
- 72 detector channels
- 4 Fixed Pattern Noise channels
- programmable charge sensitive amplifier from dynamic range 120fC to 600fC
- programmable shaper: peaking time from 116÷2000 ns
- analog memory: switched capacitor array, 511 cells, frequency 1÷50 MHz
- readout : multiplexing 511x76 20 MHz

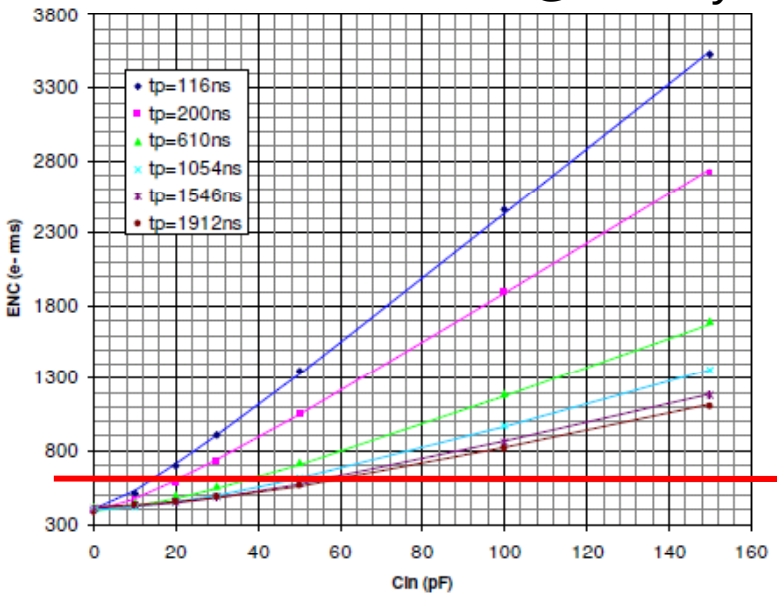


Measured chip performance

- Noise performance
  - Board is not connected to detector
  - 1 ADC unit = 0.12 fC or 700e-
  - 4+4 unconnected channels
  - 4 Fixed Pattern Noise channels



T2K noise measured @ Saclay



Noise of connected channels: ~600 e-

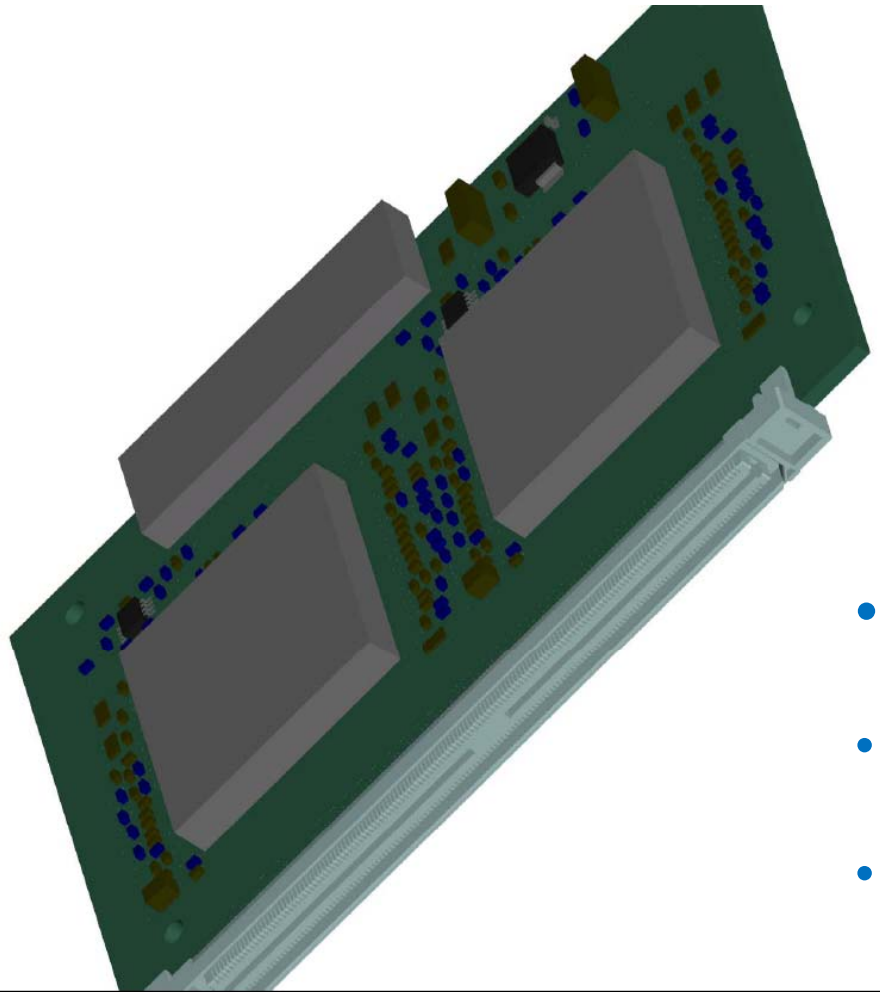
Test chamber front-end board

Front-end board:

- 4xAFTER chips
- 256 channels

- L-shaped to place chips outside of beam

Final design of AFTER FE card



- **4 AFTER chips, 256 Channels**
- **Power Supply +3.3V**
- **Power consumption < 1.5W**

Conclusions

- Not yet fully working solution for final TPC
  - Super-Altro – high power consumption, first prototype will be submitted in fall 2009
  - N-Xyter – not yet measured, higher noise than expected
  - Hit Detection ASIC – no manpower for development
- AFTER chip fulfills requirements for TPC prototype
  - 500e- noise
  - 100 ns rise time
  - 20-40 MHz sampling