

GSI Event-Driven TDC with 4 Channels

GET4

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Outline

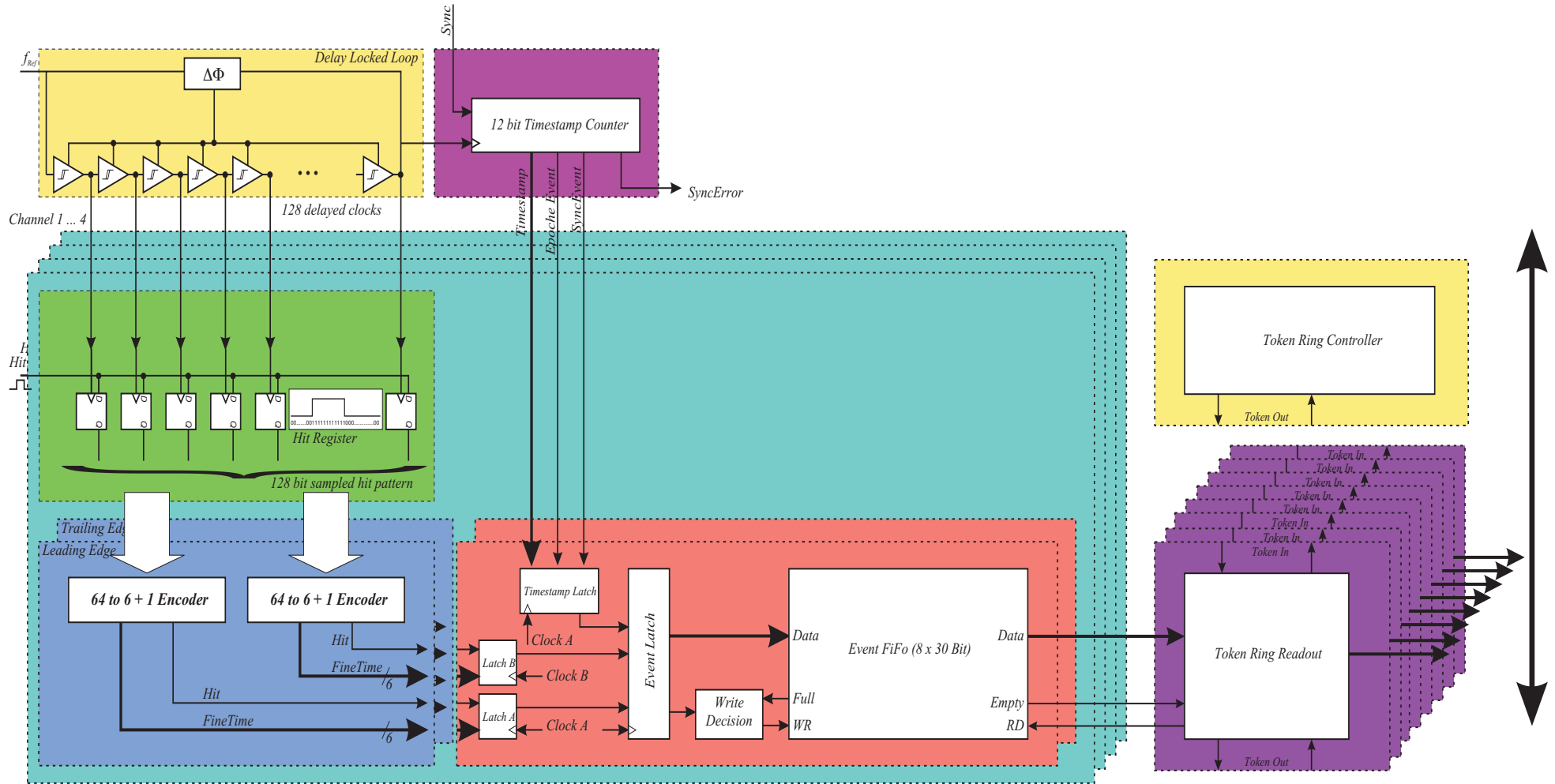


- CBM Time of Flight Requirements
- The GET4 TDC Prototype
- First Measurement Results
 - Serial readout
 - Differential Nonlinearity
 - Time Resolution
- Summary and Outlook

Requirements for the CBM ToF

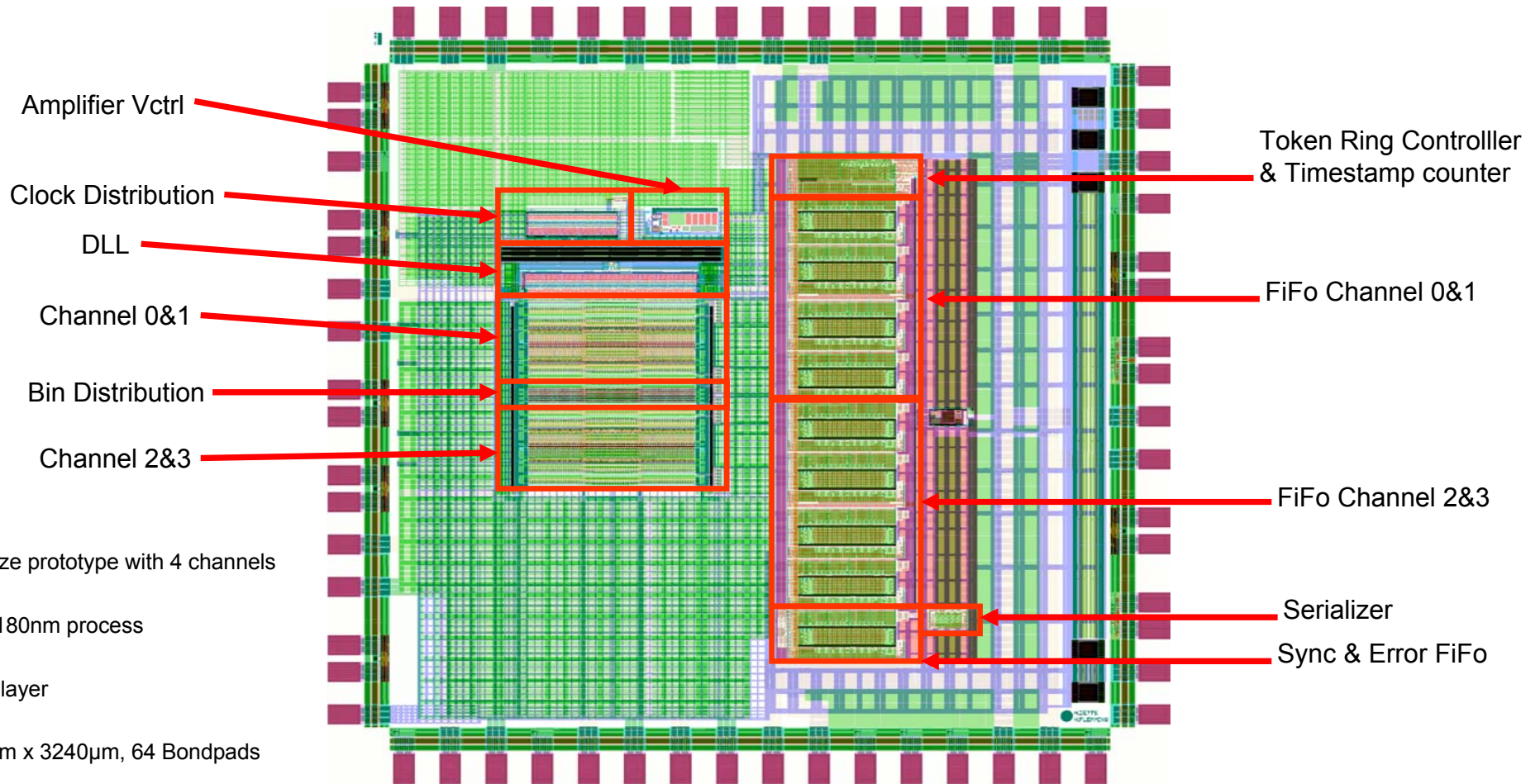
- Very high time resolution $< 25\text{ps}$
- Double hit resolution $< 5\text{ns}$
- Event rate up to 50 kHz per channel
- Capability to measure time over threshold
- Low power consumption with less than 30 mW per channel
- Number of Channels: ~ 65.000
- Triggerless operation:
 - Each event combined with a timestamp
 - Epoche event on timestamp counter overflow
- Timestamp counters of all chips have to run synchronously

Schematic Overview of GET4 Prototype



29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Epoch			Time Stamp														Fine Time B						Fine Time A						
Sync			Hit B														Hit A												

GET4 Layout



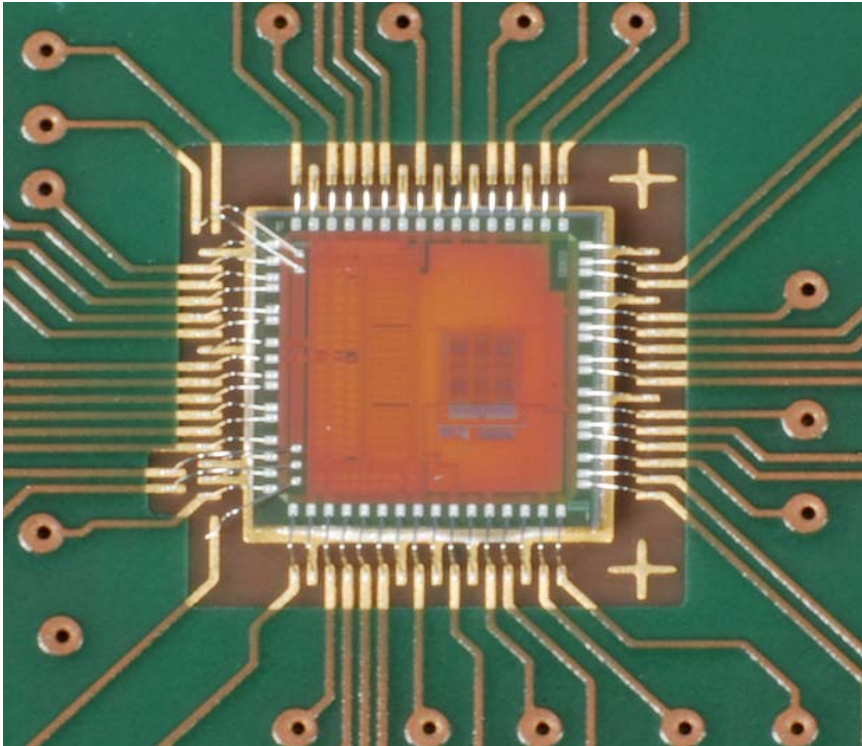
• Submitted in Oct. 2008

Holger Fleming, GSI

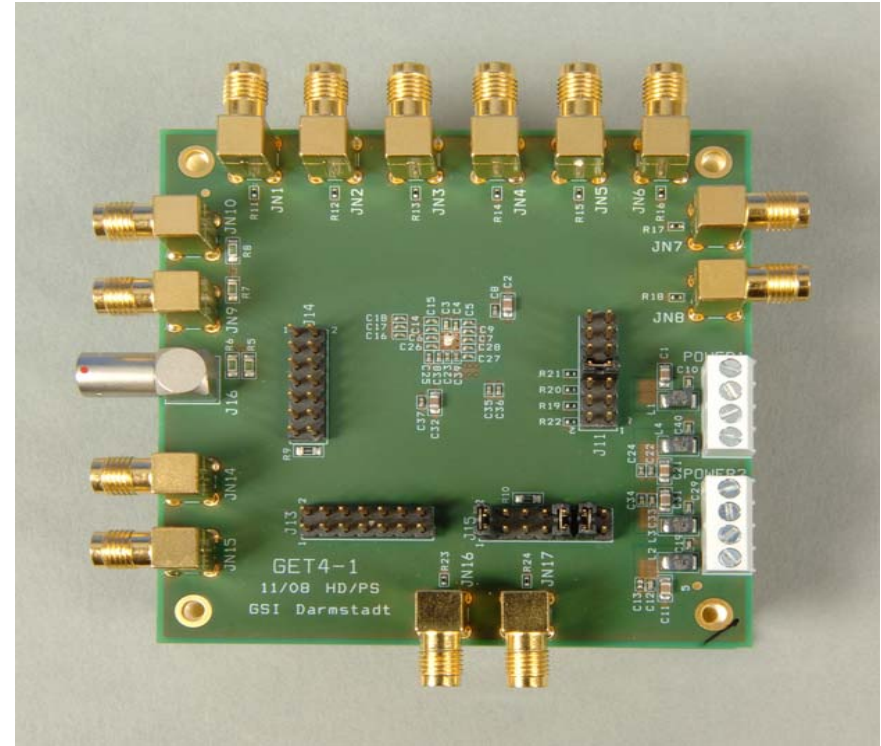
Bodenmais, 2009

GET4 Prototype PCB

Bottom side view

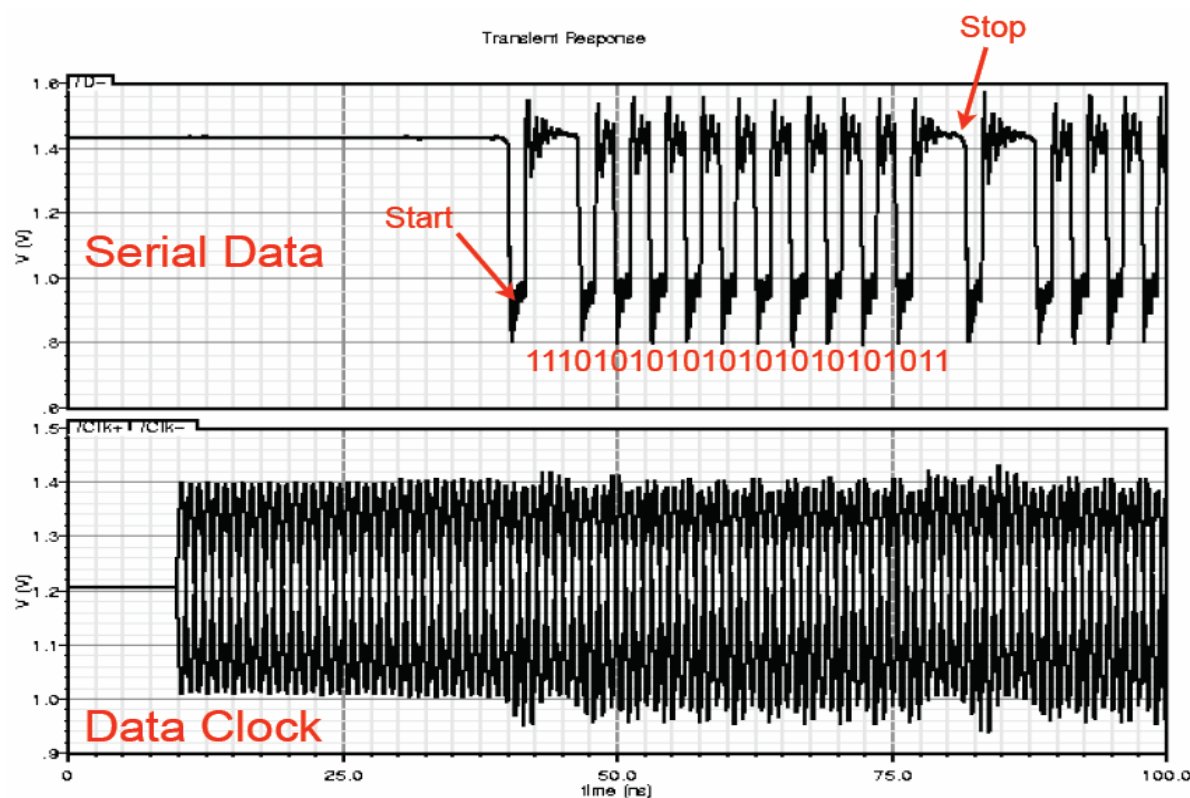


Top side view



Serial Data Transmission

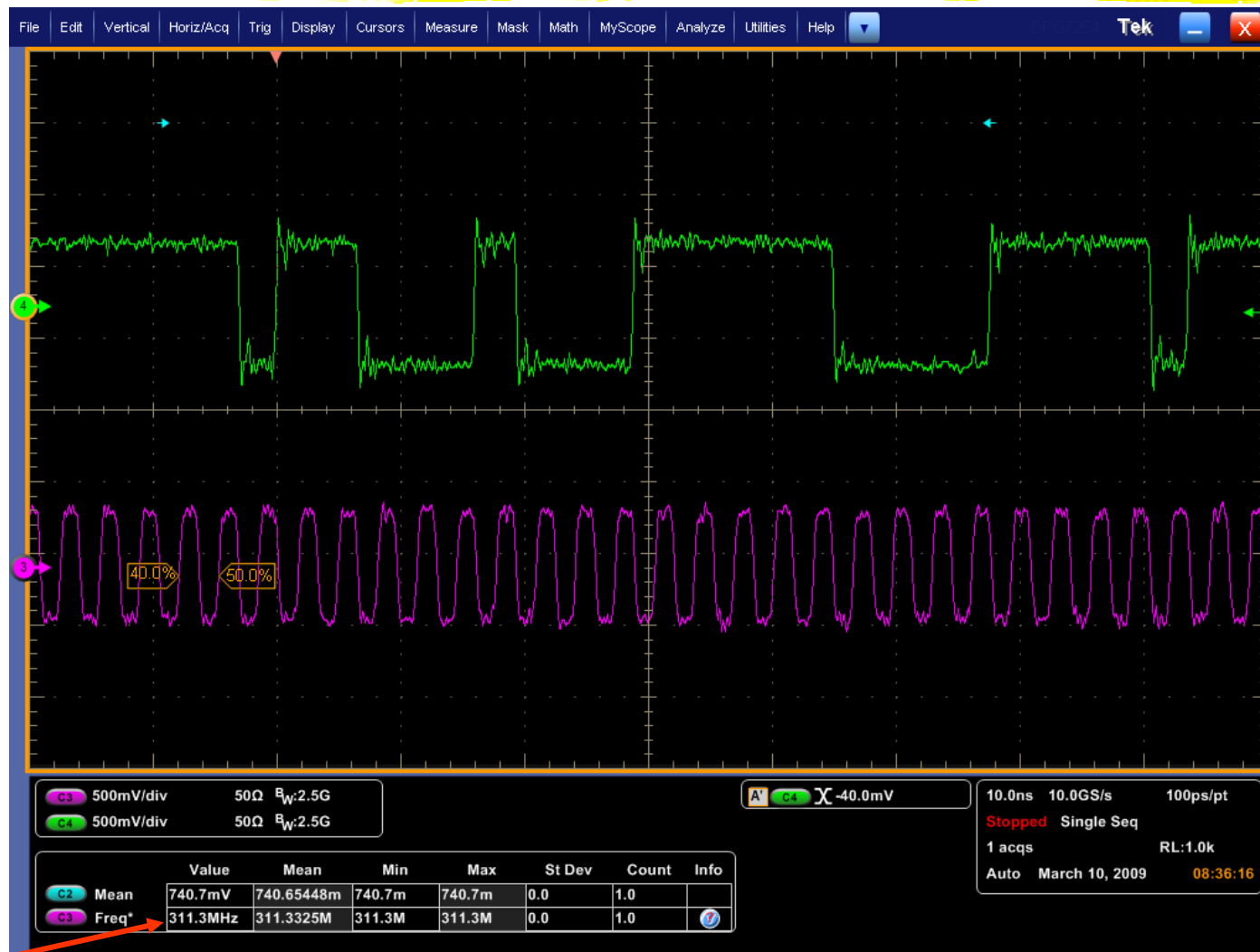
- External Data Clock
 - For 50 kHz/Ch event rate
 - => Min. Data Rate 10.5 MBit/s
- Asynchronous Data format
 - 1 Start Bit (Low)
 - 24 Data Bits
 - 1 Stop Bit (High)
 - no Parity
- LVDS Clock input
- LVDS Serial Data Output



Serial Data Transmission

Serial Data

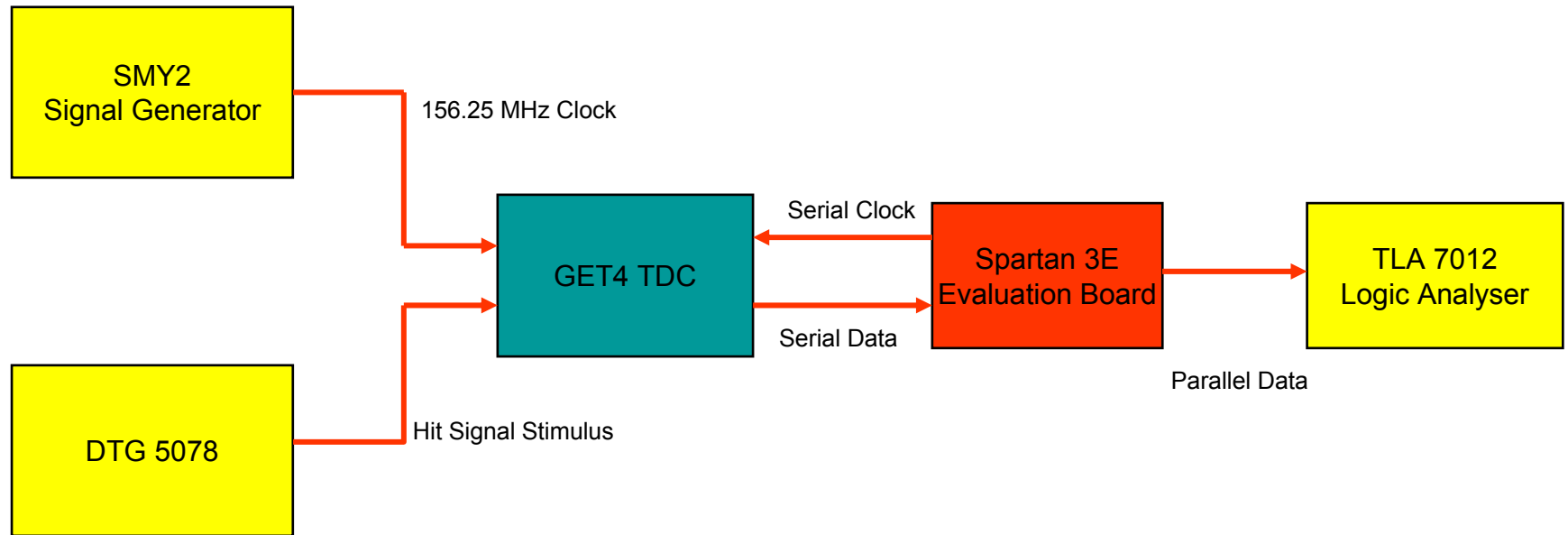
Serial Clock



Tested Data Rates: 312.5 MBit/s ~ 1.5 MHz/Ch Eventrate

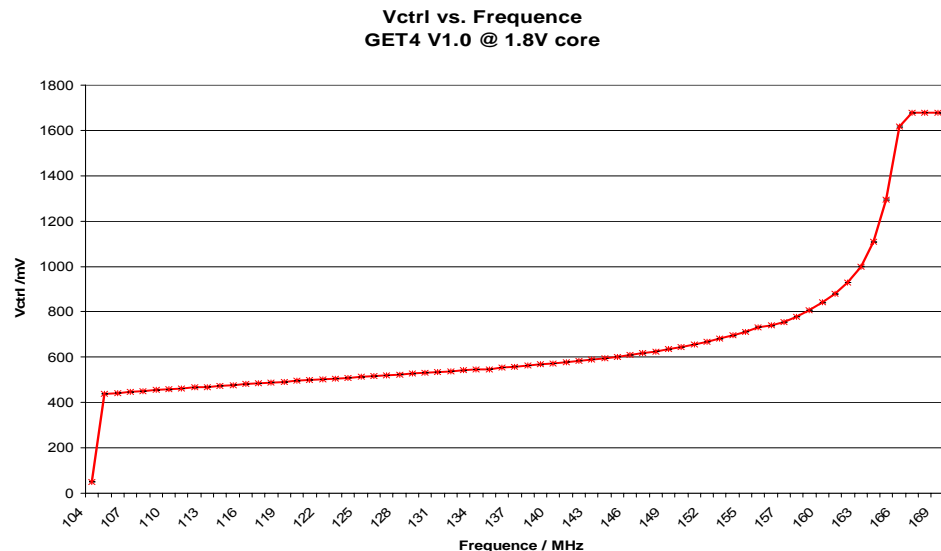
Bodenmais, 2009

Test Setup



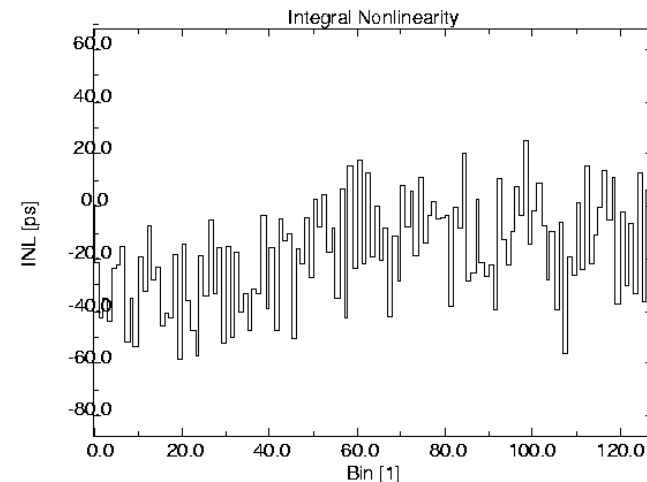
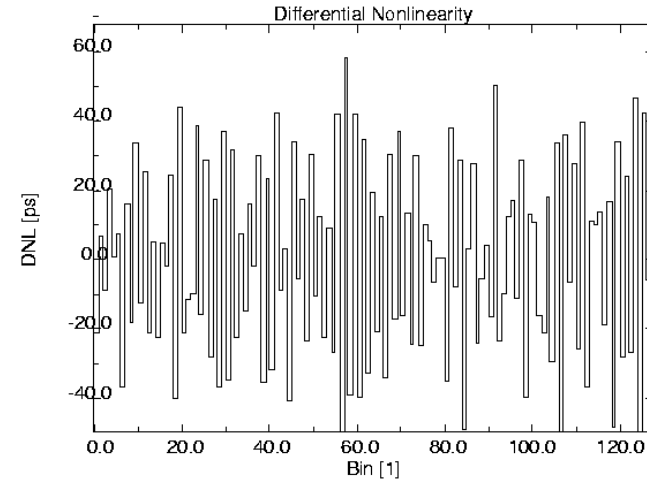
Measurements and Results GET4

- Clock 156.25MHz
- Lock Range 110MHz – 165MHz
- Power consumption:
 - 27mW/Chan @ 150kHz event rate



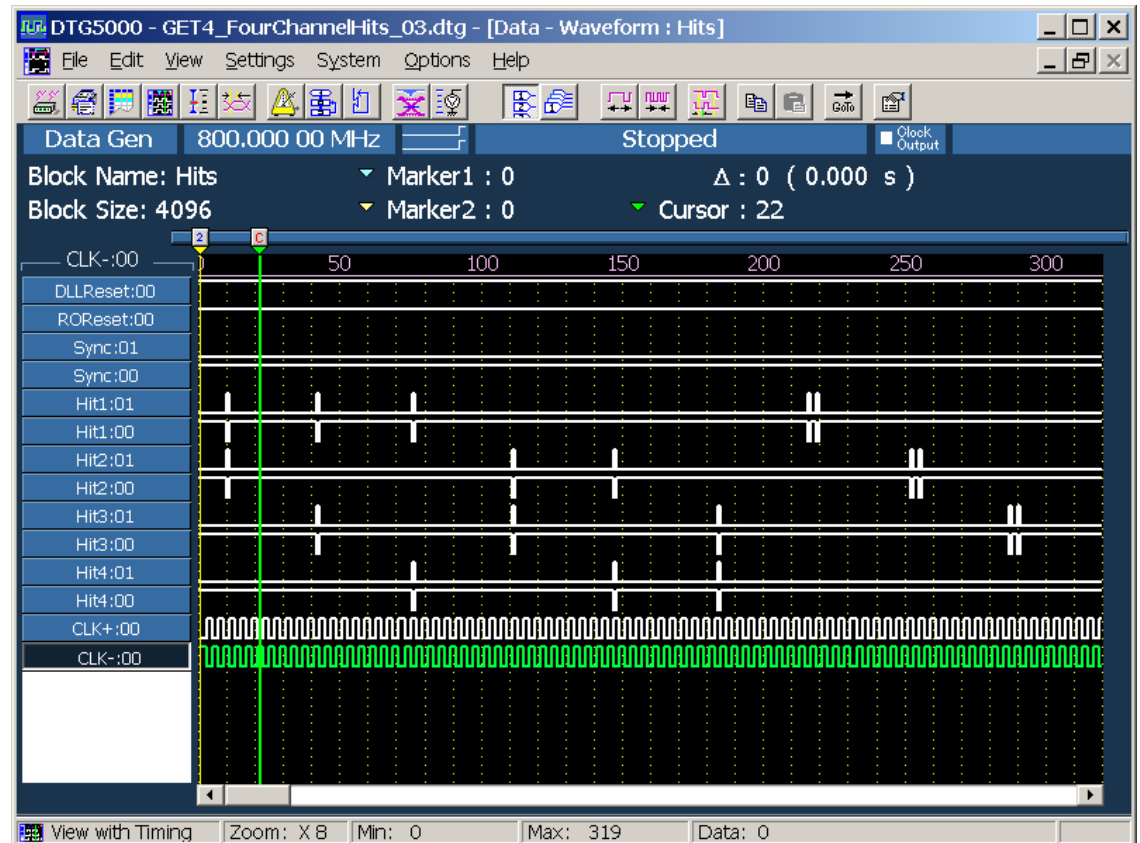
Measurements and Results GET4

- Linearity:
 - $DNL < \pm 60 \text{ ps} = \pm 1.2 \text{ LSB}$
 - $INL < \pm 80 \text{ ps} = \pm 1.5 \text{ LSB}$
- In comparison to DANTE:
 - DNL: $\pm 0.4 \text{ LSB}$
 - INL: $\pm 0.5 \text{ LSB}$
- Reasons for Nonlinearity are still under investigation



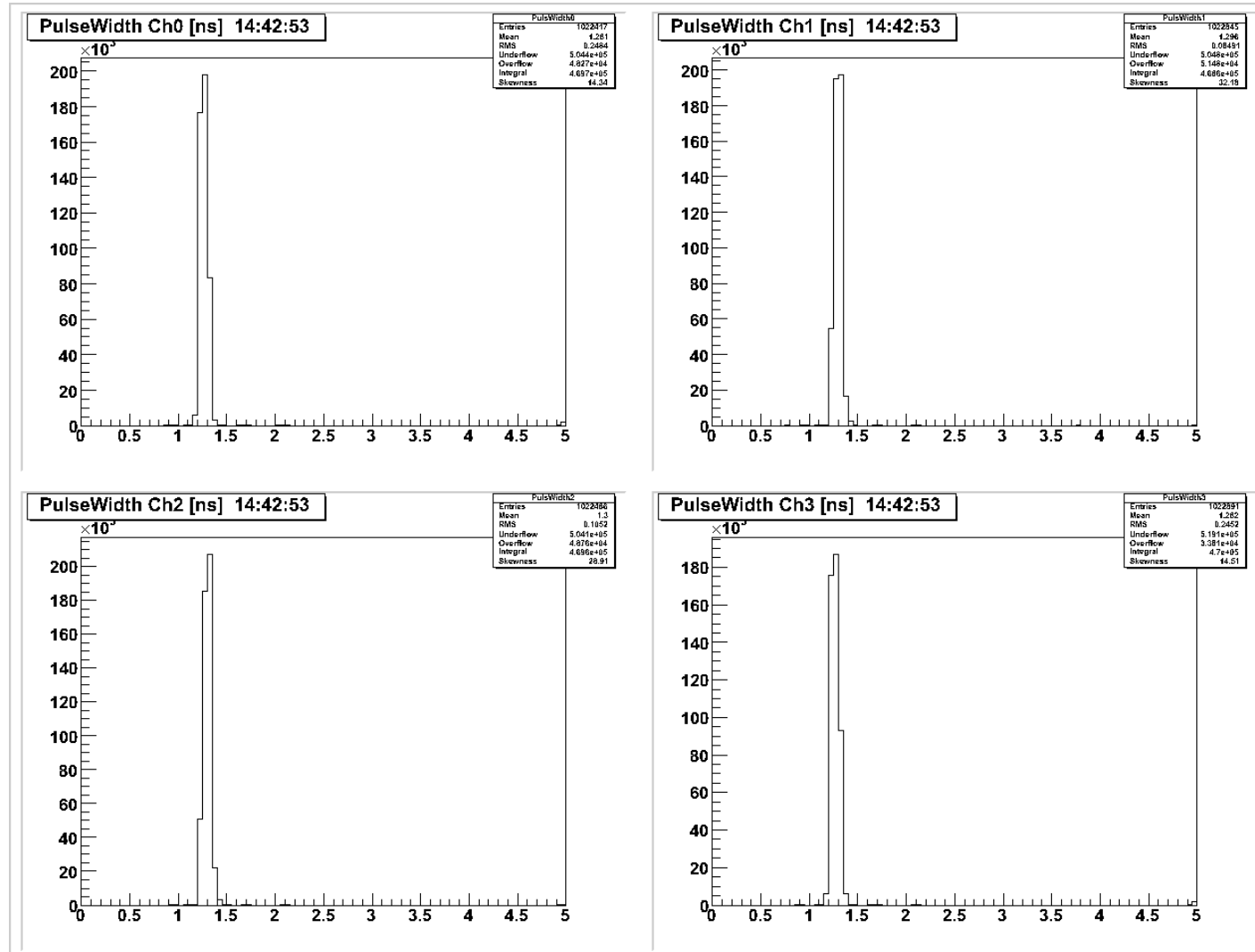
Test Setup: Hit Signal Stimulus

- Puls Width: 1.25 ns
- Synchronous Pulses on two channels
- Double Pulses, 3.75 ns puls spacing



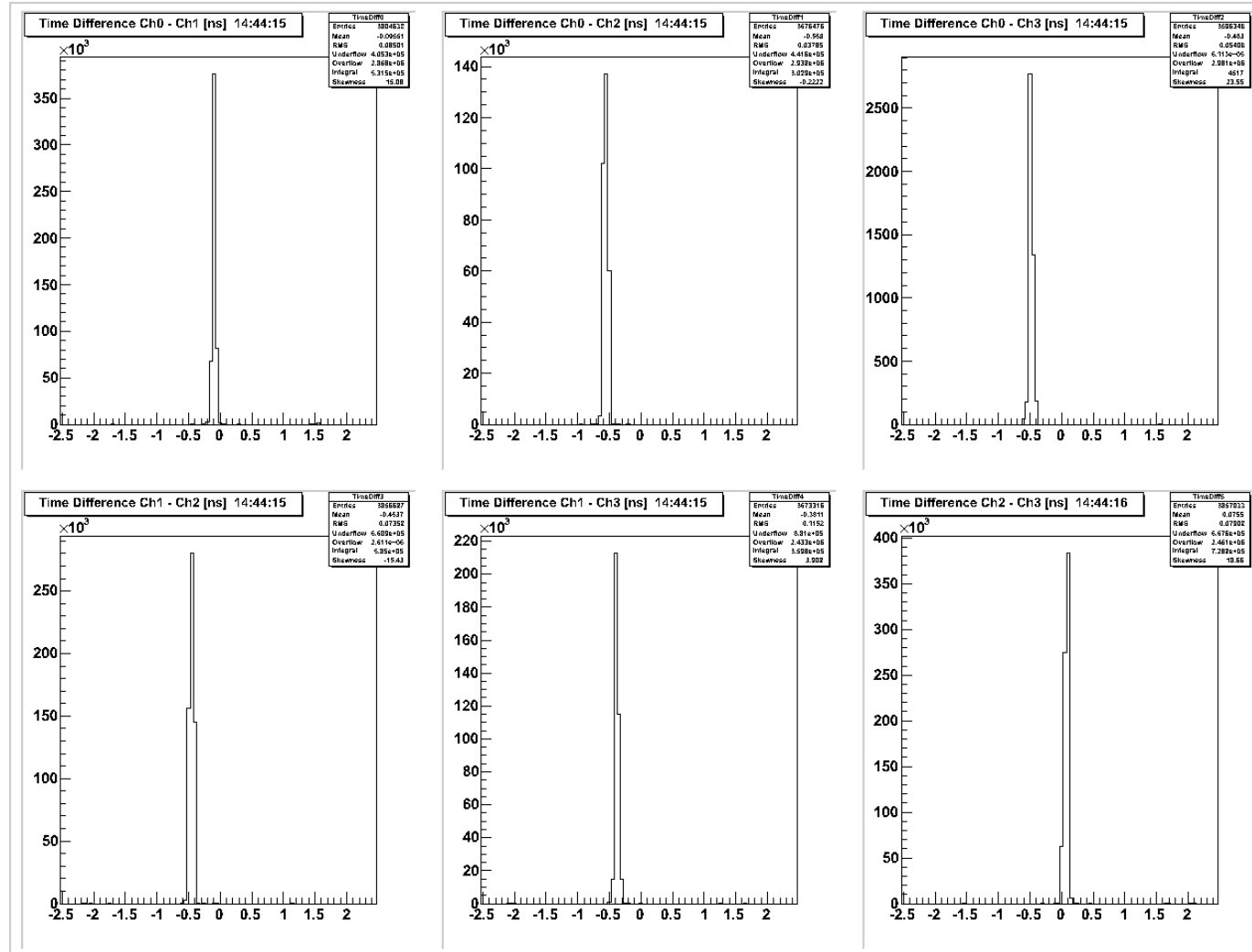
Measurements and Results GET4

- Puls Width Measurements
- μ : 1.283 ns
- σ : 36.7 ps
- Uncorrelated Resolution: 25.9 ps



Measurements and Results GET4

- Time Difference
- σ : 29.1 ps
- Uncorrelated Resolution: 20.6 ps



Measurements and Results GET4

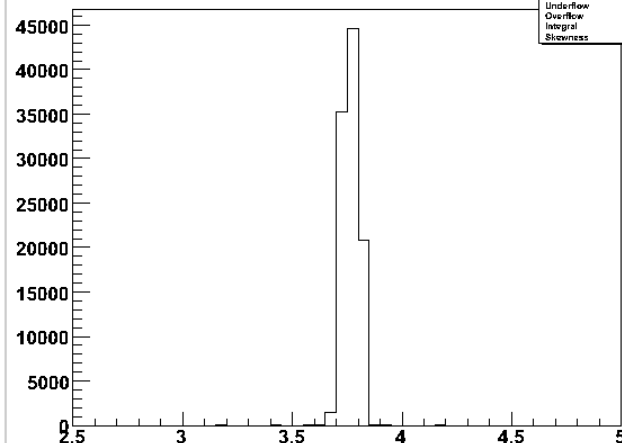
- Puls spacing Measurements

- μ : 3.766 ns

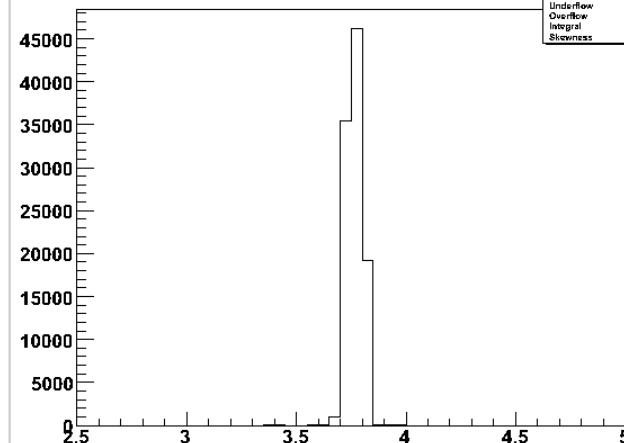
- σ : 33.5 ps

- Uncorrelated Resolution: 23.7 ps

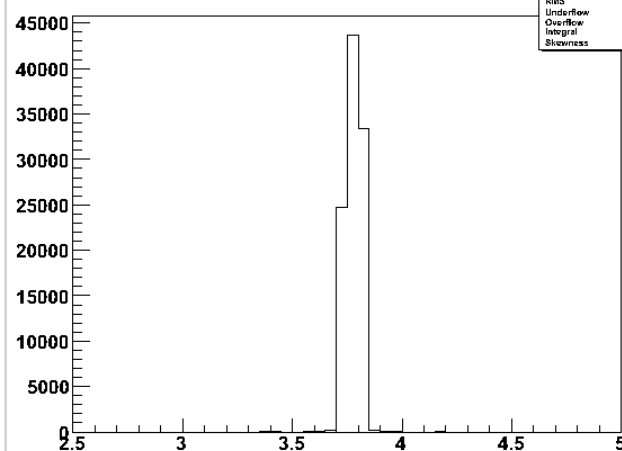
Double Pulse Time Difference Ch0 14:45:30



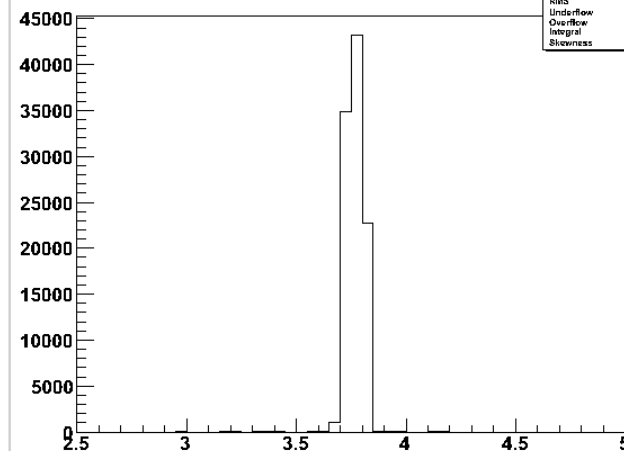
Double Pulse Time Difference Ch1 14:45:30



Double Pulse Time Difference Ch2 14:45:31

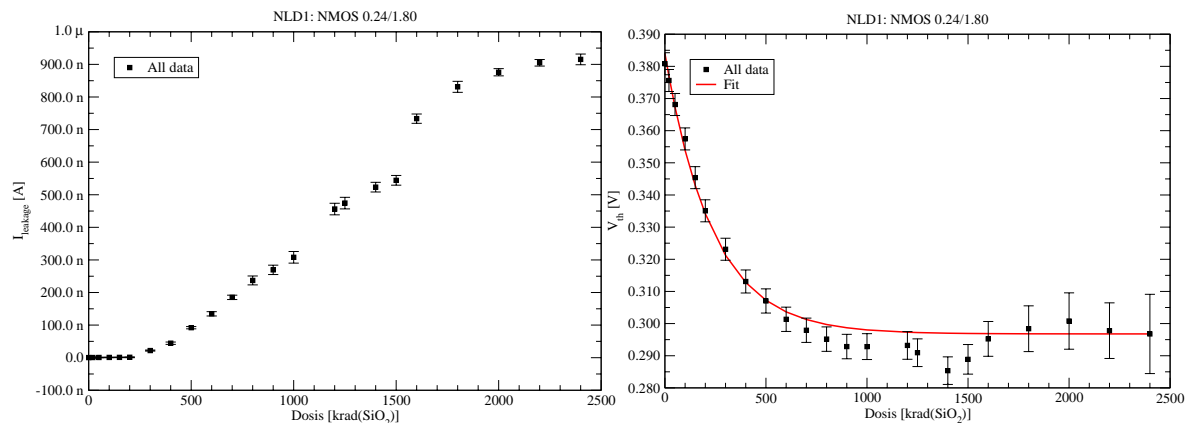
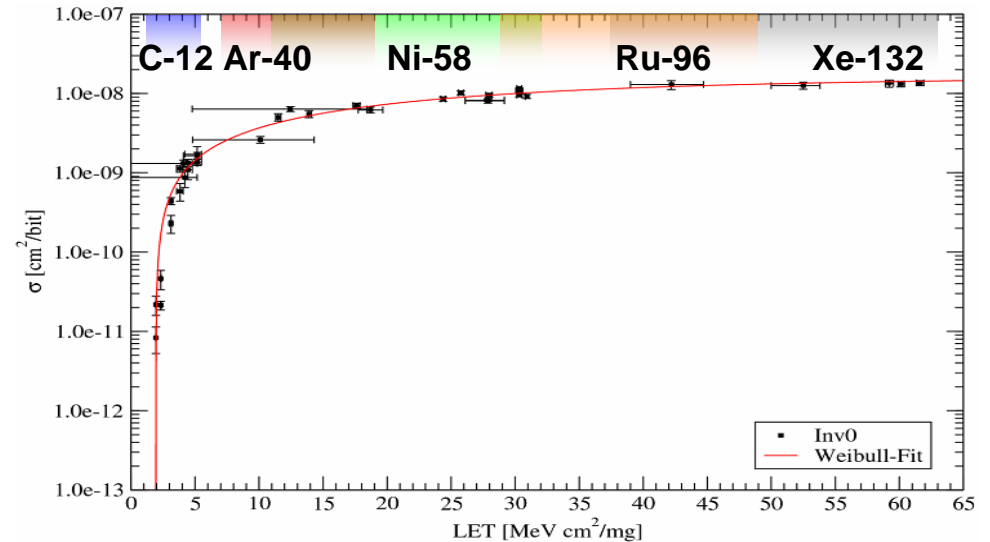


Double Pulse Time Difference Ch3 14:45:31



Radiation Tolerance

- Radiation effects on UMC 180 nm process have been investigated with special testchip GRISU
- Single event effect cross section is well known
- In the CBM-ToF environment problems with total ionising dose effects are not expected
- What is the dose rate in the PANDA environment?



Summary and Outlook

- First full scale TDC Prototype GET4 was submitted In Oct. 2008
 - Token ring readout and serialiser are fully operational
 - DNL of TDC core worse than on DANTE test chip
 - Time resolution: 20 ps ... 25 ps
 - Double hit resolution > 3.2 ns
 - With GET4 a first TDC Prototype for detector tests is available
- Next Steps:
 - 2009:
 - Design and submission of an 1.5 mm by 1.5 mm testchip for Investigation on reasons for nonlinearity
 - 2010
 - Next full scale prototype
 - On chip slow control: DLL Lock detection, error state detection
 - Improving of DAQ Interface

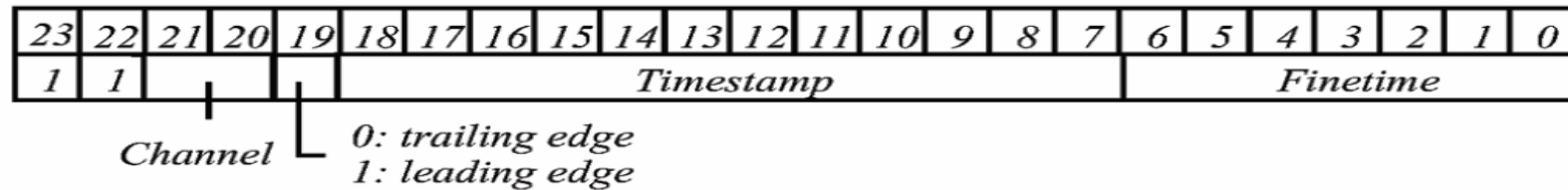
Thanks.....

A thick, horizontal yellow brushstroke with a textured, painterly appearance, spanning the width of the slide.

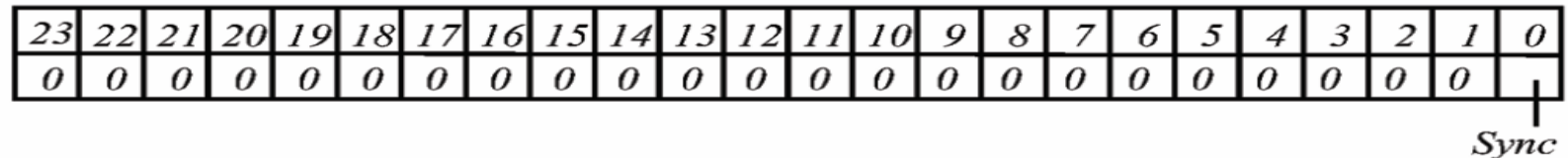
- **for your attention**

Event Format

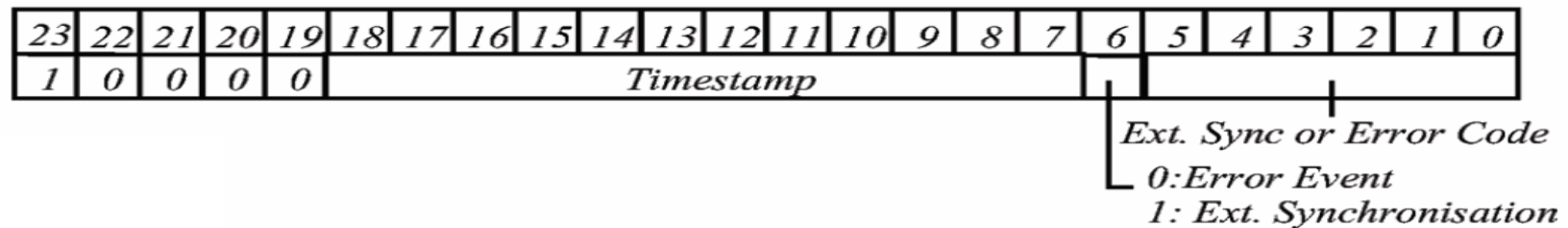
Data Events



Epoche Event



Ext. Sync and Error Event



Timestamp Synchronization

- External Sync signal
- Synchronization on next leading edge of clock after leading edge of Sync signal
- Flagging of Epoche and Sync events

