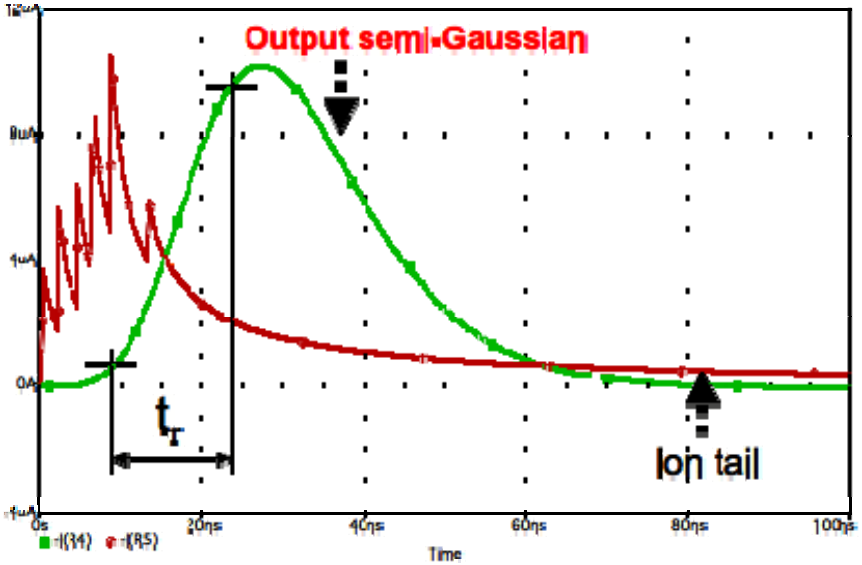
TDC choice

I.Konorov

- STT requirements
- HPTDC architecture and differential nonlinearity
- Summary of PANDA requirements

STT detector

Number of channels	about 5000
MIP signal	0.6pC
Gas gain	$4 \cdot 10^4$
Average hit rate less	7 kHz
Amplifier gain	10mV/fC
Time resolution	0.5÷1 ns
FE chip candidates	Carioca or ASDQ



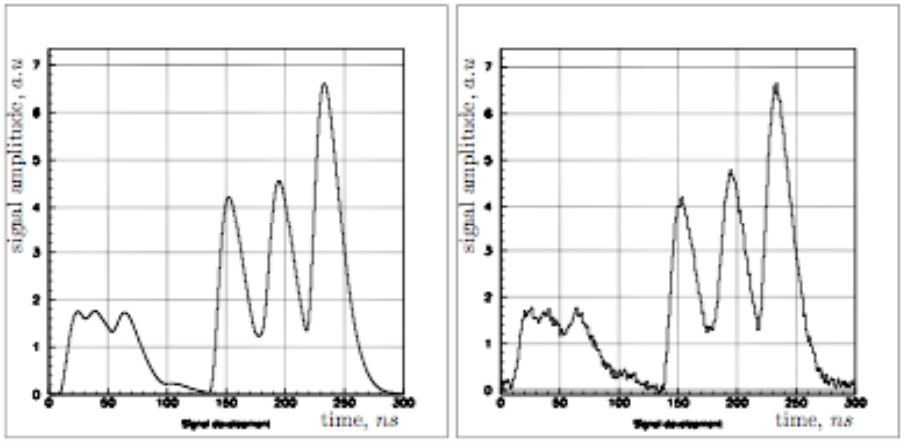
Preamp/shaper

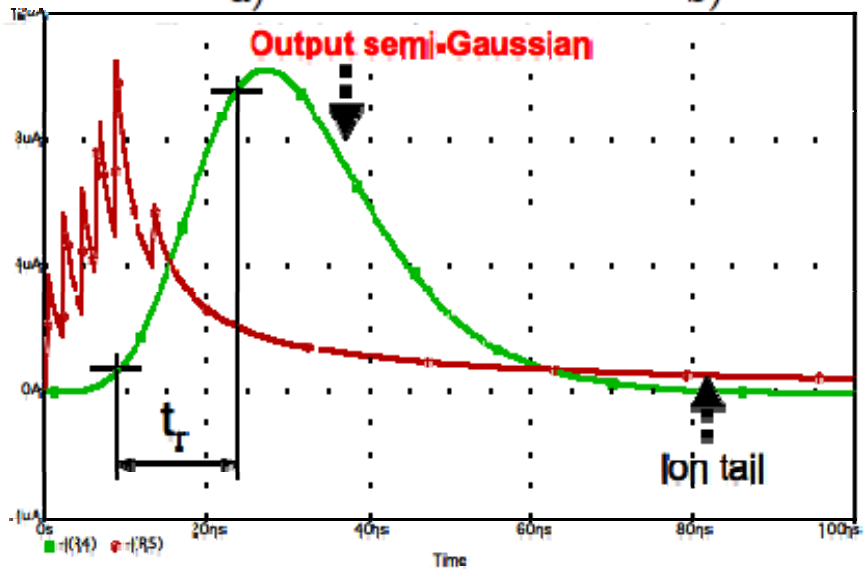
Input and output signals

Peak time 20 ns

STT signal

Raw signal WO amplifier/shaper





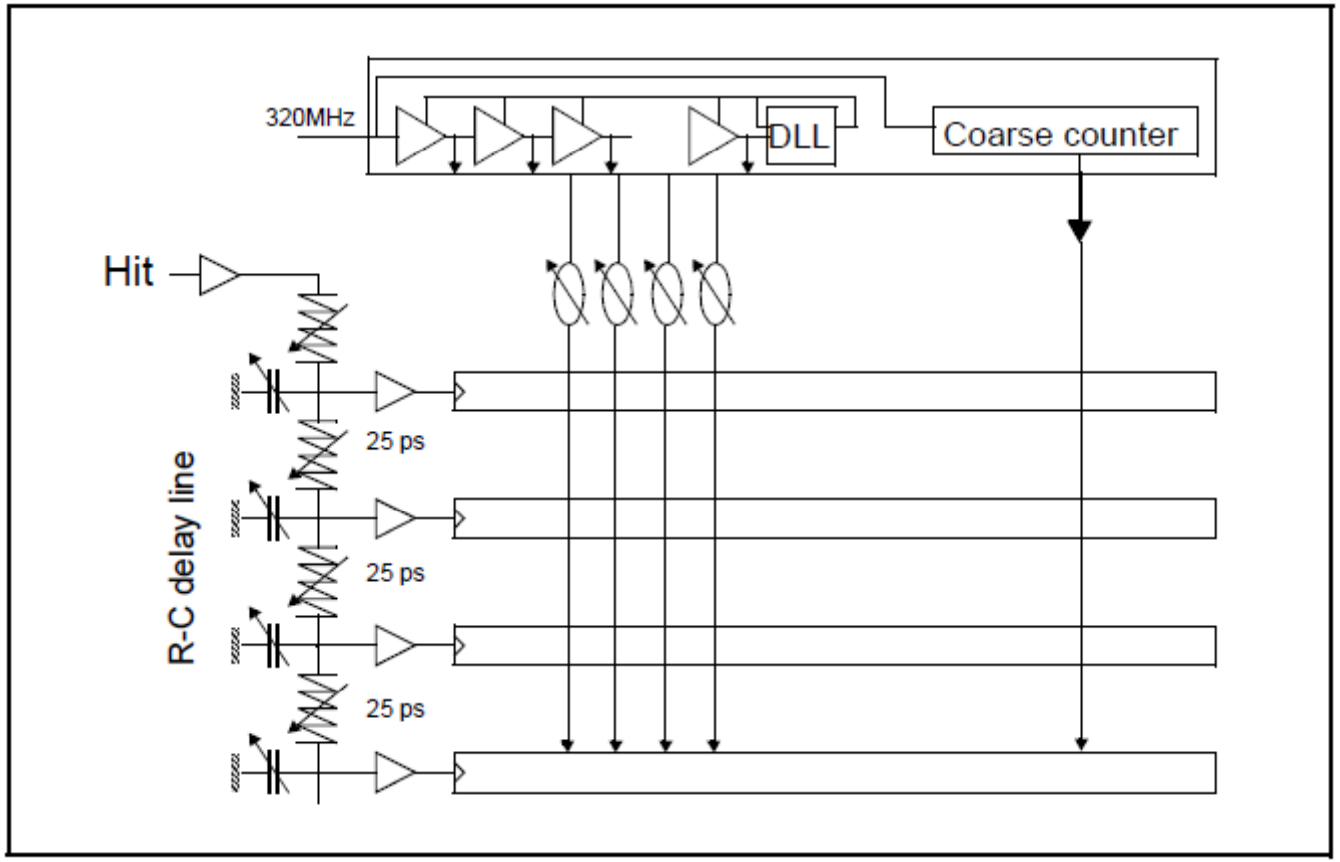
HPTDC

- 32 channels – 800ps, 200, 100 ps bin
- 8 channels - 25 ps bin

Maximum hit rate 2MHz/channels , no hit correlation.

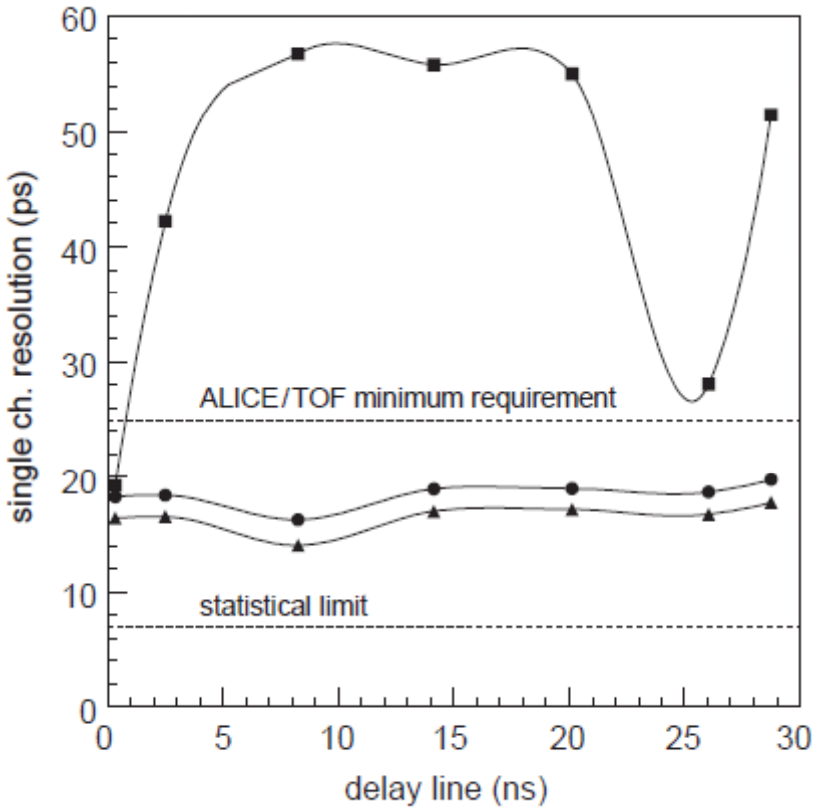
Requires calibration in very high resolution mode

HPTDC high resolution mode



Requires calibration in very high resolution mode

Integral Non linearity ALICE TOF



[3]. The main source of the INL was identified as coming from on-chip crosstalk from the logic part of the chip through the power supply. Despite

INL is stable in time and can be corrected With LUT

System resolution of 20ps is achievable

Short summary of TDC requirements

Number of channels :

Straw, 20000 channels - 0.5-2 ns time resolution , up to 800(1600)kHz hit rate

HPTDC Low resolution mode : about 700 HPTDC chip

Barrel DIRC, 7000 channels - 0.1 ns time resolution, 160kHz

HPTDC medium resolution mode : 250 HPTDC chip

Forward DIRC, 4000/1000 ch - 100/25 ps time res. 1MHz,/2MHz hit rate

HPTDC high/very high resolution mode - 200 chips

Sci TOF, 132+240+192 channels - 25 ps time resolution, 1MHz hit rate

HPTDC very high resolution mode – 80 chips

Muon detector ???

Total number of HPTDC chips 1300

Cost 65 SFr/chip

Chips available