Readout Electronics for LumiCal Detector at ILC

possible applications in PANDA...?

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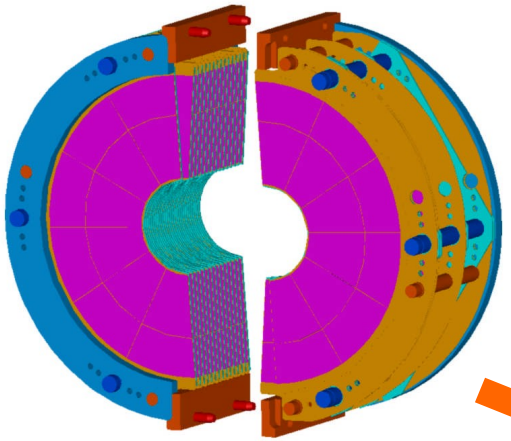
Outline

- LumiCal Architecture and Readout
- LumiCal Front-end electronics
- ADC design and measurements
- General purpose DAC design
- Other designs
- Summary

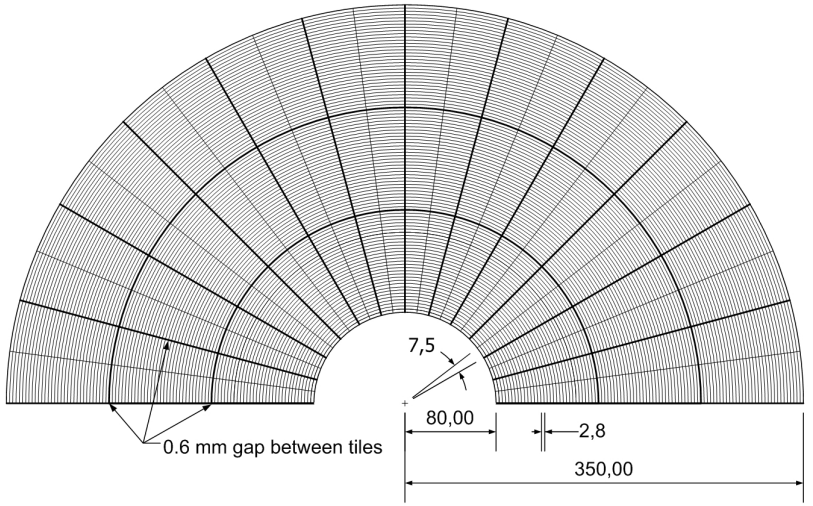
LumiCal architecture

Si/W sandwich calorimeter,
2 half barrels, each 30 layers



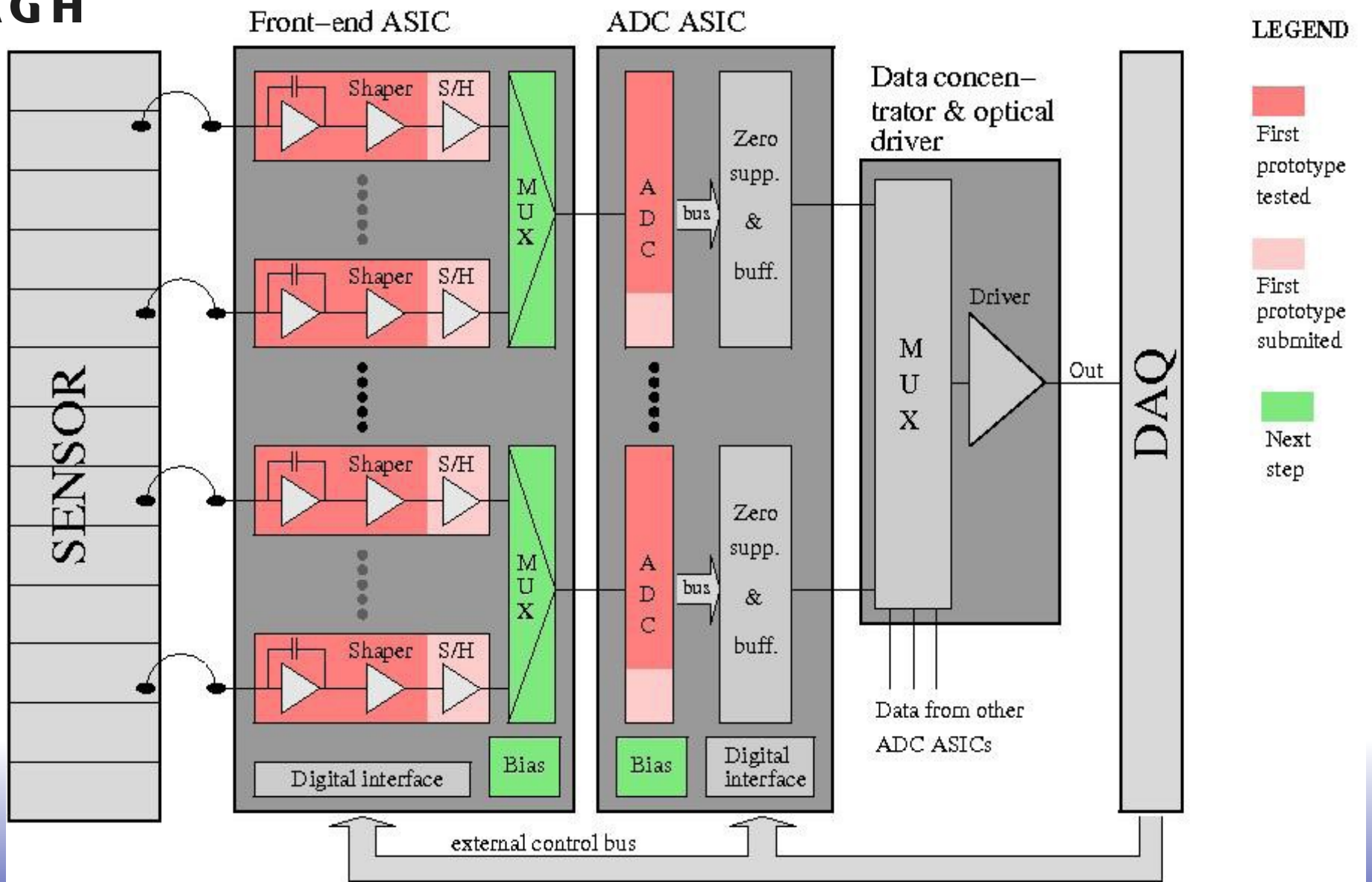
- Signal: from 2 fC - 10 pC
- Occupancy: up to ~20%
- Sensors: C_{det} 10-100 pF
- leakage current ?
- Inter bunch time ~ 350 ns
- Low average power dissipation

Each layer consists
of 0.35cm thick
tungsten
and 300μm thick Si
sensor

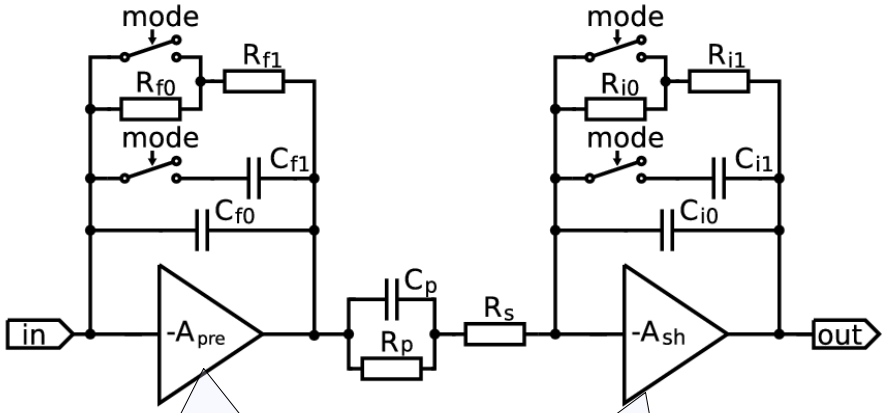


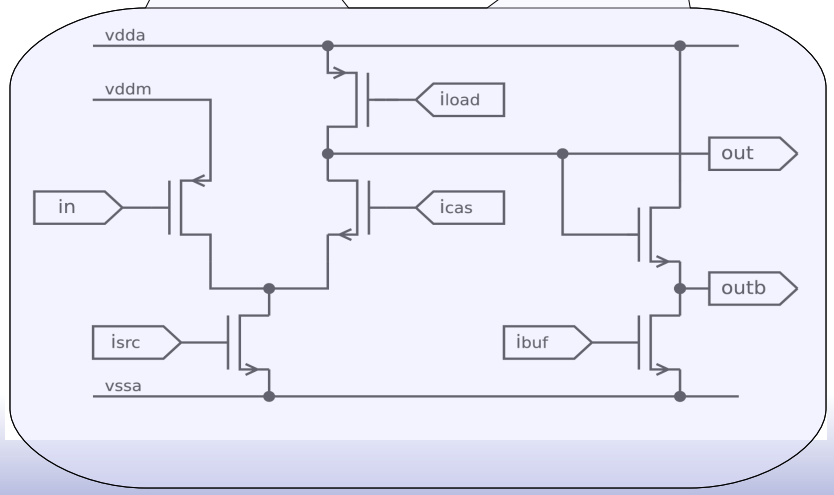
Single detector layer
48 azimuthal sectors,
each sector ~96 radial pads

LumiCal Readout System



Front-end architecture





Components

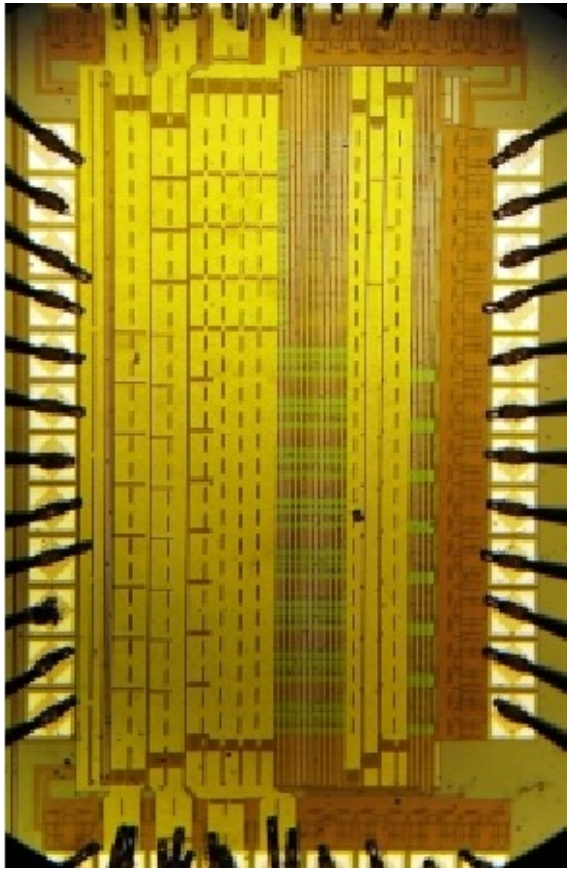
- Charge amplifier
- Pole zero cancellation
- CR-RC Shaper

Specifications (old):

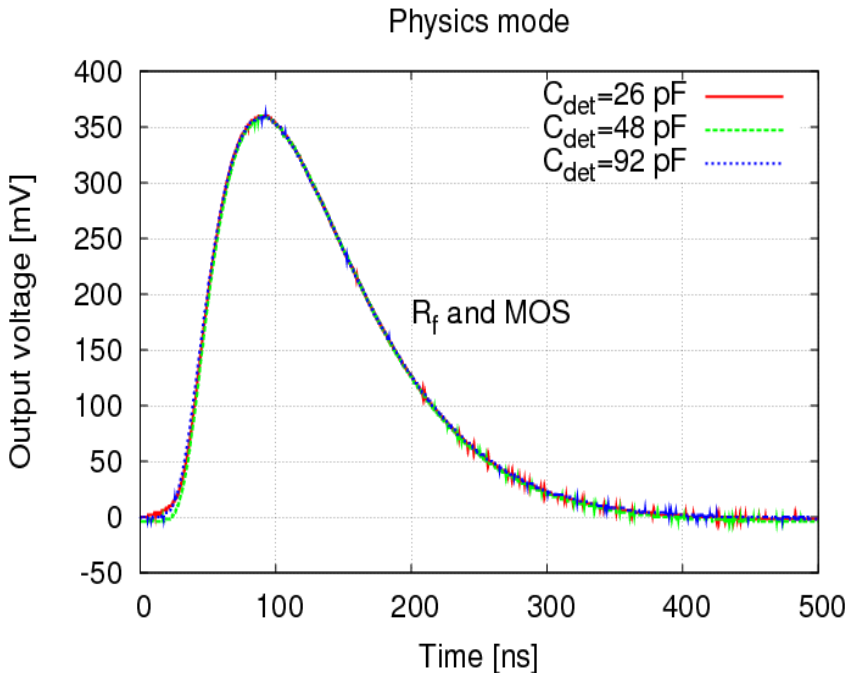
- C_{det} = 10 – 100 pF
- T_{peak} ~ 60 ns
- Variable gain: physics and calibration mode
- Physics mode: Q_{max} ~ 10 pC (C_f=10 pF)
- Calibration mode: S/N > 10 for MIP

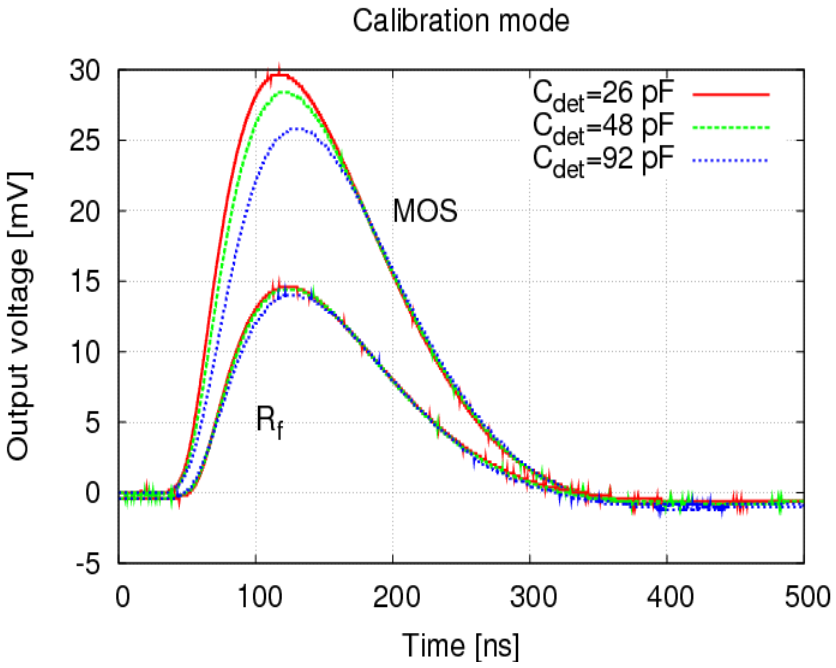
Front-end prototype

- AMS 0.35 μm technology
- 8 channels
  - 4 channels with MOS feedback
  - 4 channels with passive R_f feedback
- Power dissipation < 9mW/channel



Pulse shape

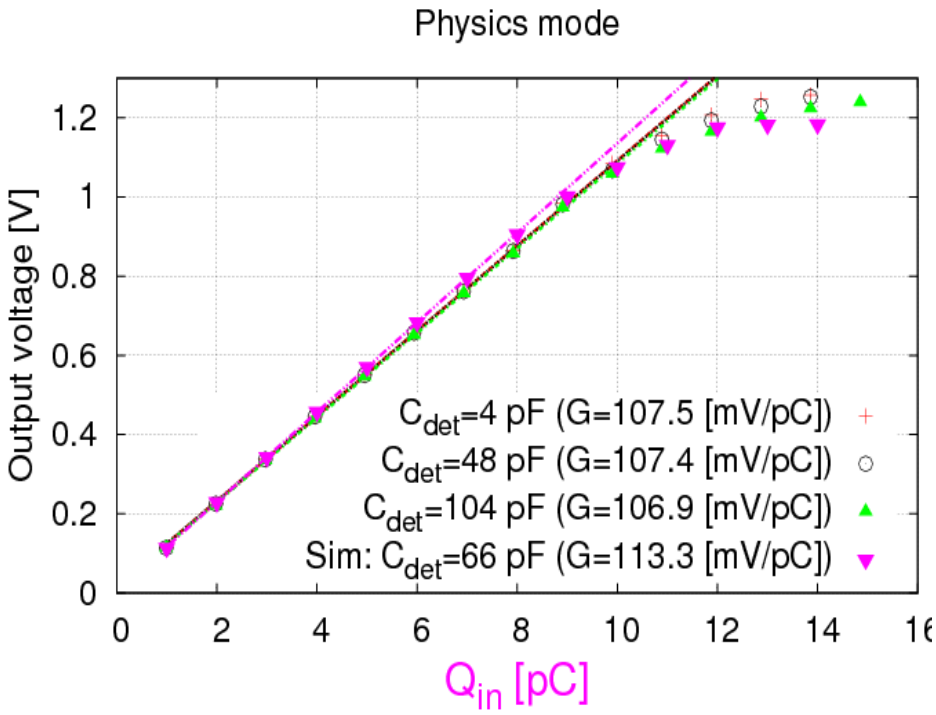


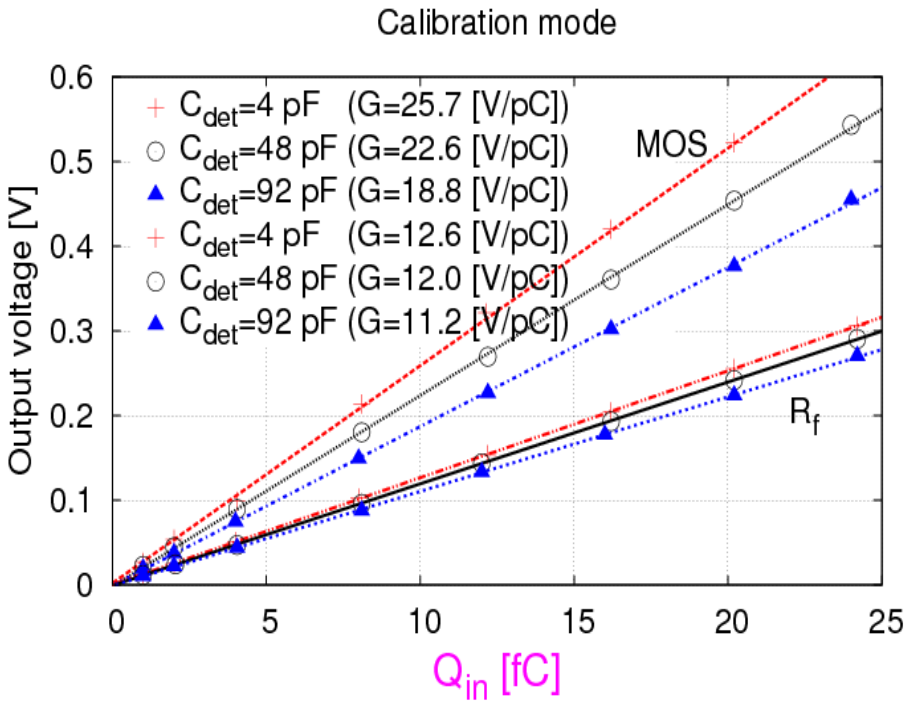


Very good charge sensitivity in physics mode (same for MOS and passive R_f feedback)

Slight sensor capacitance dependence in calibration mode (gain for MOS and R_f feedback different by design)

Gain



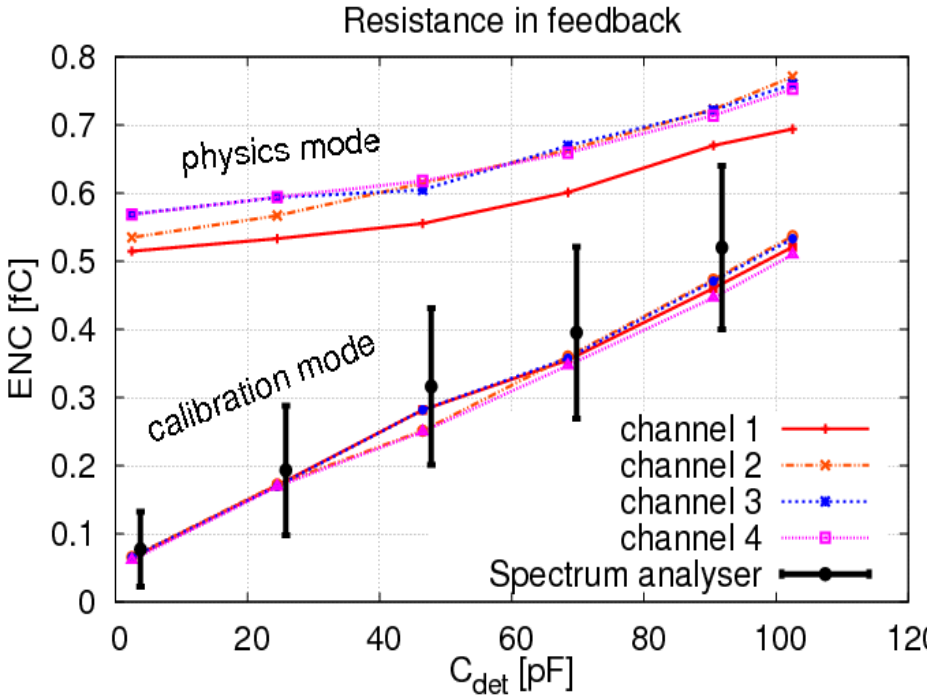


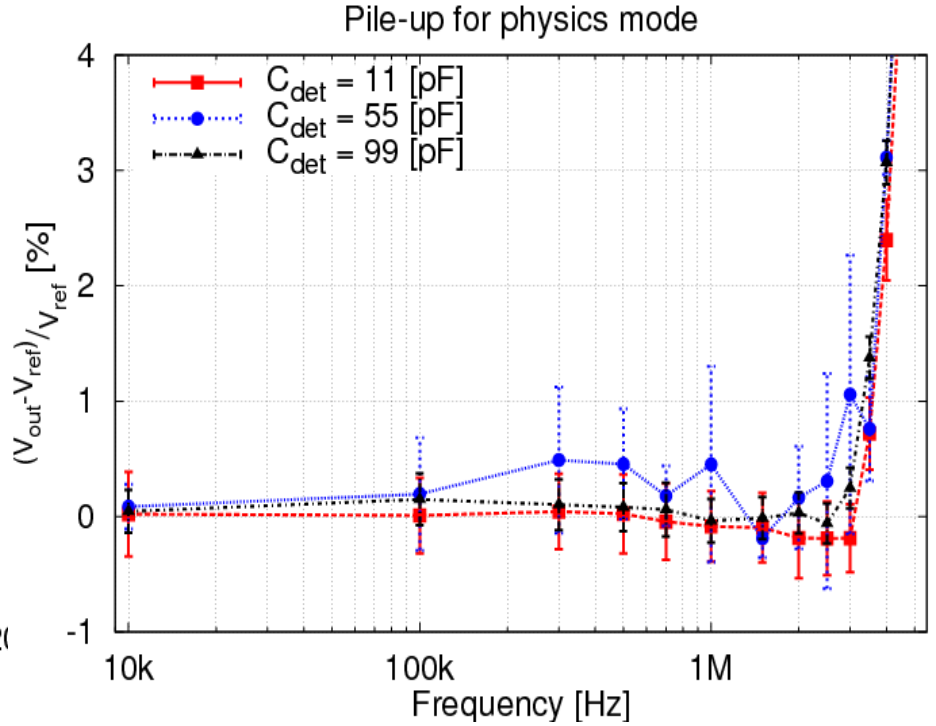
Constant gain in physics mode

Slight gain decrease with growing sensor capacitance in calibration mode

Noise

Pulse rate



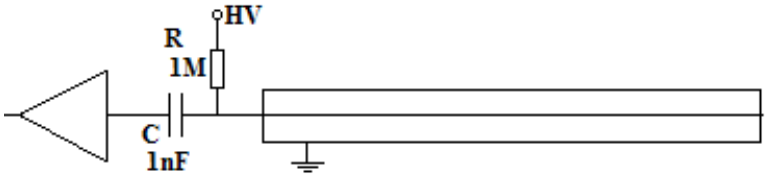


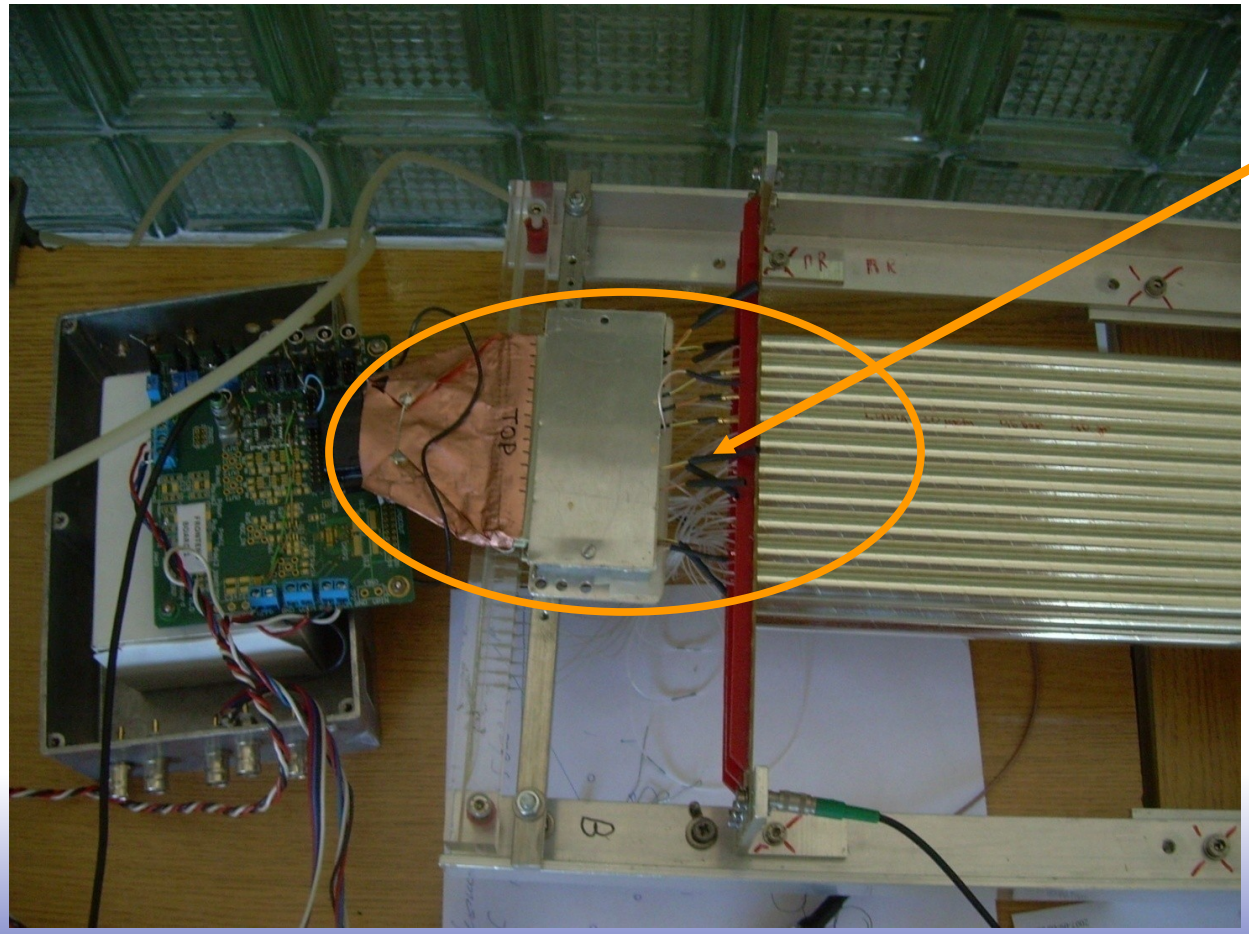
- *Noise measurements done with external capacitance and generator. Need to be confirmed with sensor and particles*
- *In calibration mode noise < 0.4 fC - good MIP sensitivity (SNR > 10)*

- *Front-end works well up to ~3 MHz continuous input rate*

LumiCal front-end with straw tubes

ASIC output connected to external ADC



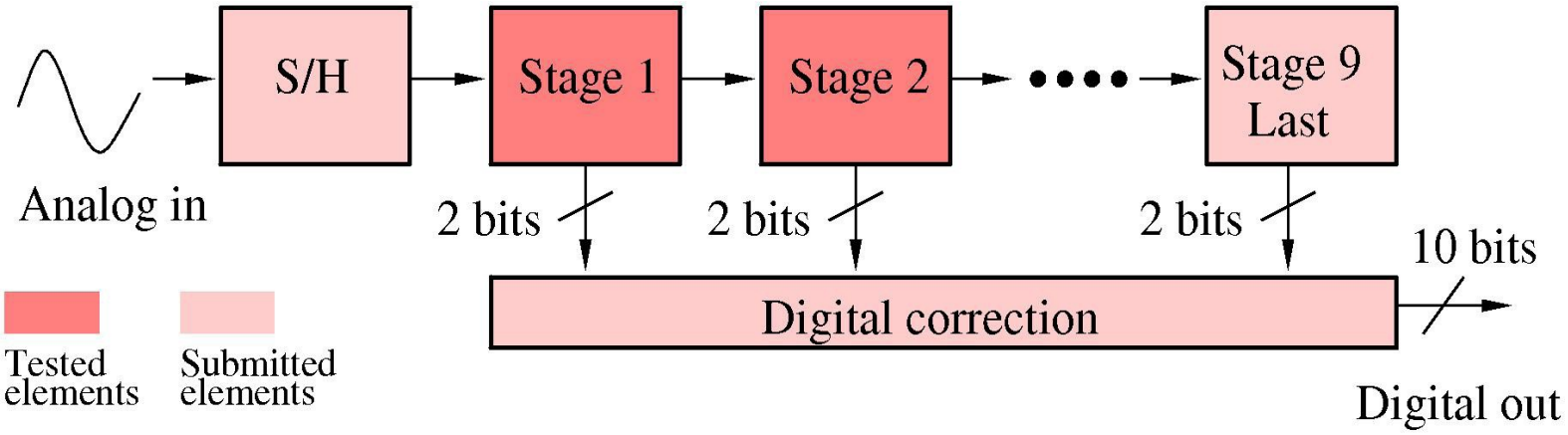


Connection between detector and preamplifier through RC decoupling filter

First Measurements taken by P.Salabura and J. Smyrski Group at Jagiellonian University

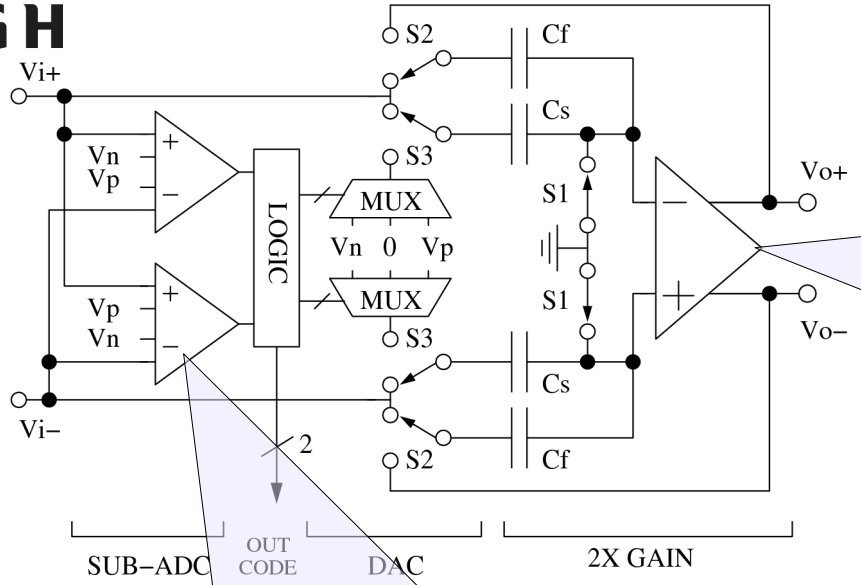
Systematic investigations and comparison with Carioca front-end in progress!

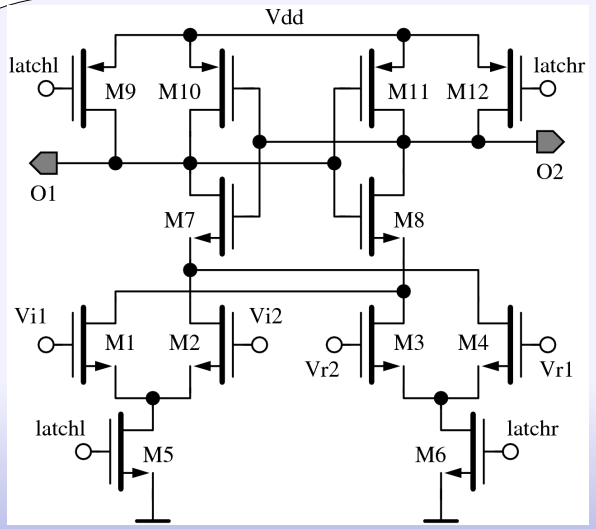
ADC architecture



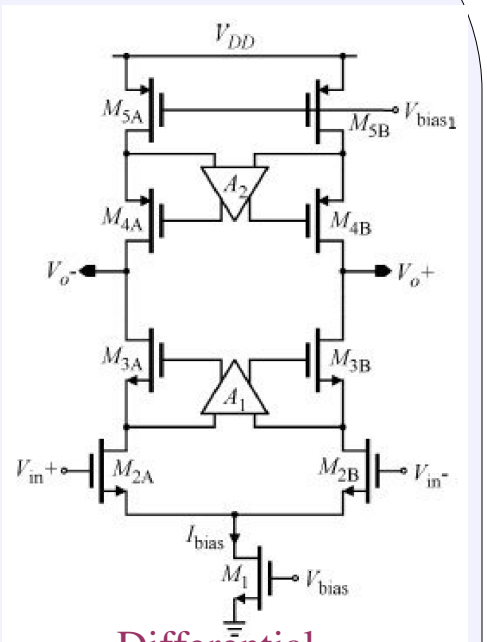
- Pipeline architecture (fully differential)
- 10 bits resolution (1.5 bit per stage)
- Input dynamic range 2 V
- Maximum sampling rate 35 MHz
- Power efficient & small area

1.5 bit stage architecture





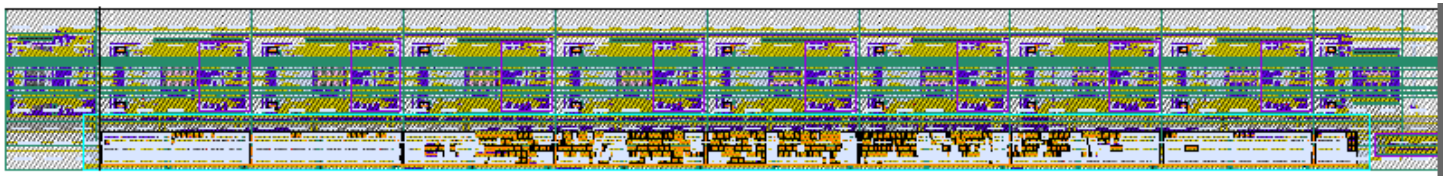
Dynamic latch comparators



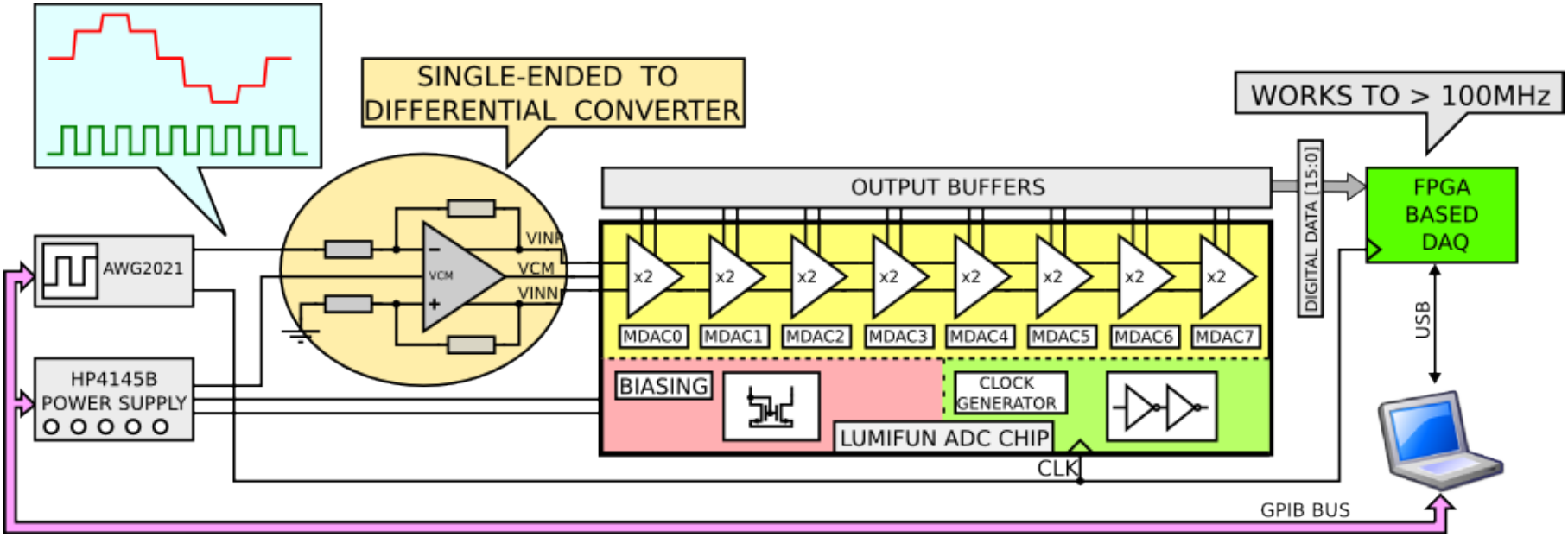
Differential amplifier with boosted gain

ADC 2nd prototype

- AMS 0.35 μm technology
- Channel area about 330μm x 2950μm
- All 9 stages and Sample&Hold
- Digital correction implemented
- Biasing and Reference voltages applied externally

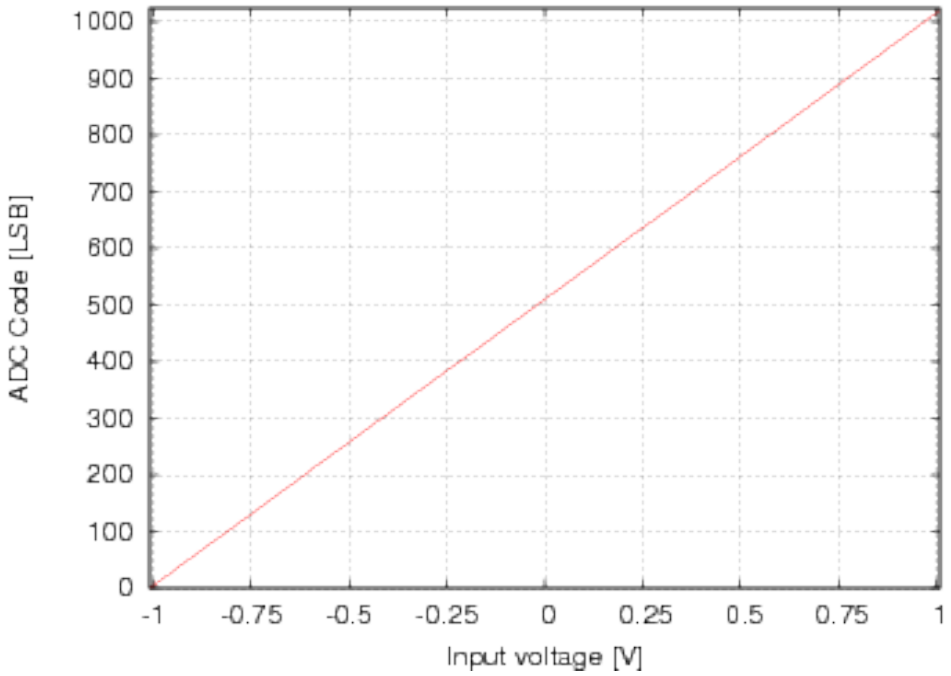


ADC test setup (FPGA based)



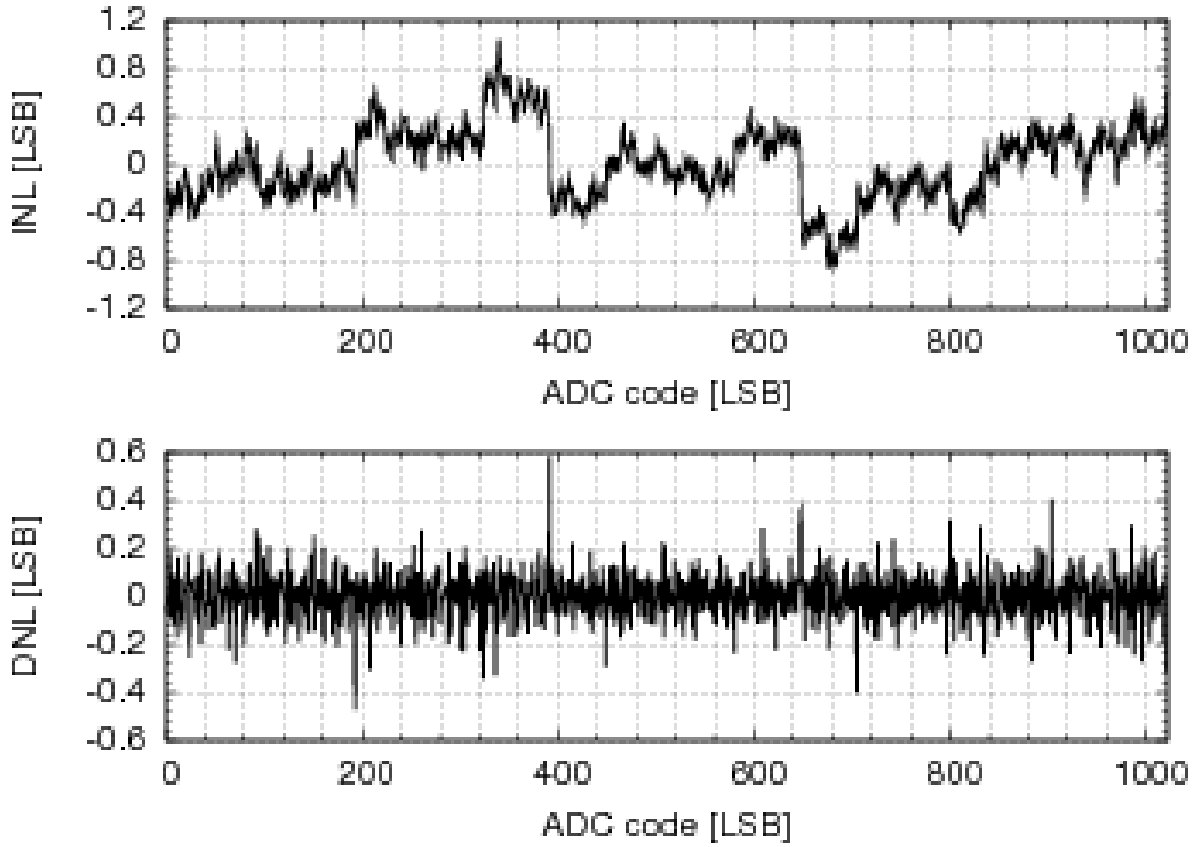
- Static measurements
  - INL, DNL, ENOB
- Dynamic FFT measurements
  - SNHR, THD, SFDR, SINAD, ENOB

ADC measurements
Very preliminary!



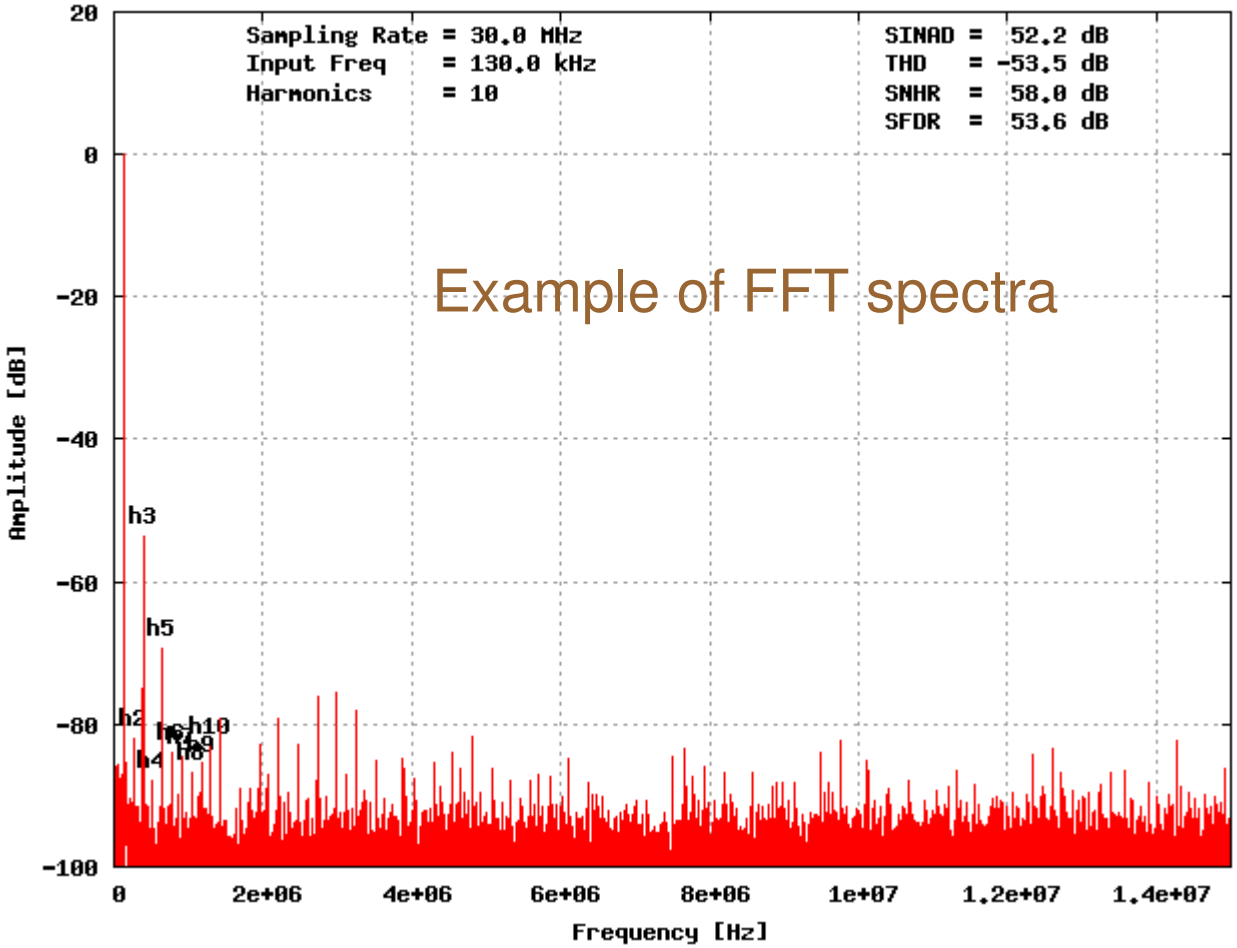
- Power consumption at 30MHz
  - Analog 8-14mA x 3.3V
  - Digital 6mA x 3.3V

Static ADC tests
Very preliminary!



- Maximum Integral Nonlinearity INL < 1 LSB
- Maximum Differential Nonlinearity DNL < 0.6 LSB

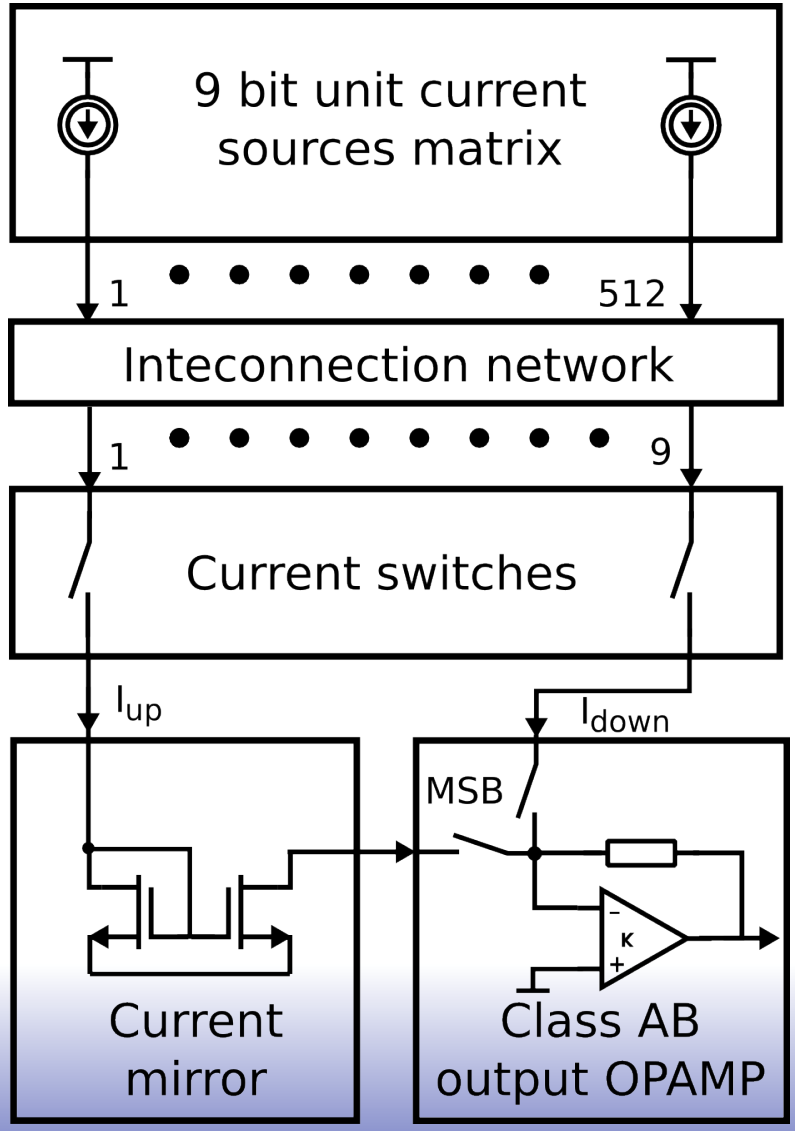
Dynamic FFT ADC tests
Very preliminary!



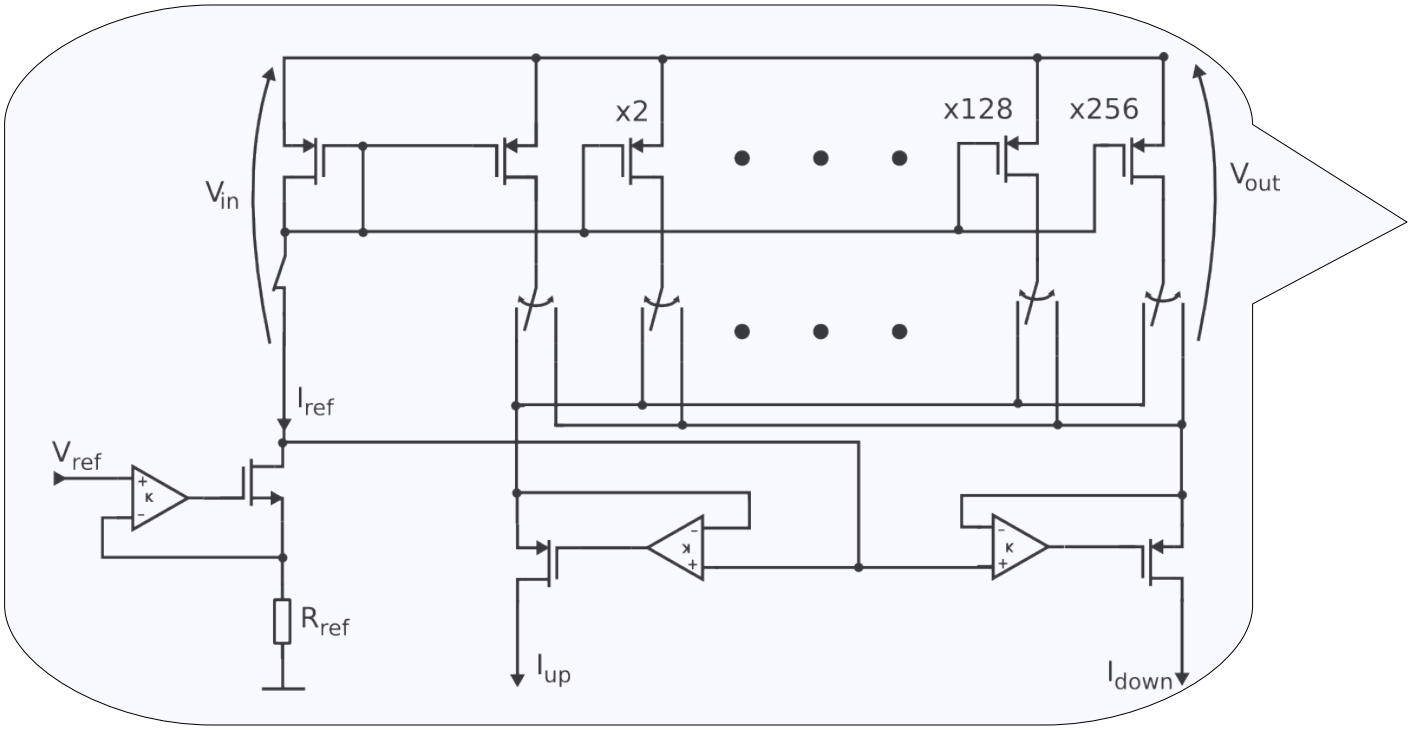
- Good S/N (SNHR), resolution slightly worse than from static measurements, but 3rd harmonic might come from the setup

General purpose DAC

- DAC specifications:
  - 10 bits
  - Voltage output
  - High swing
  - Low power (<1mW)
  - Small area
  - No high rate request

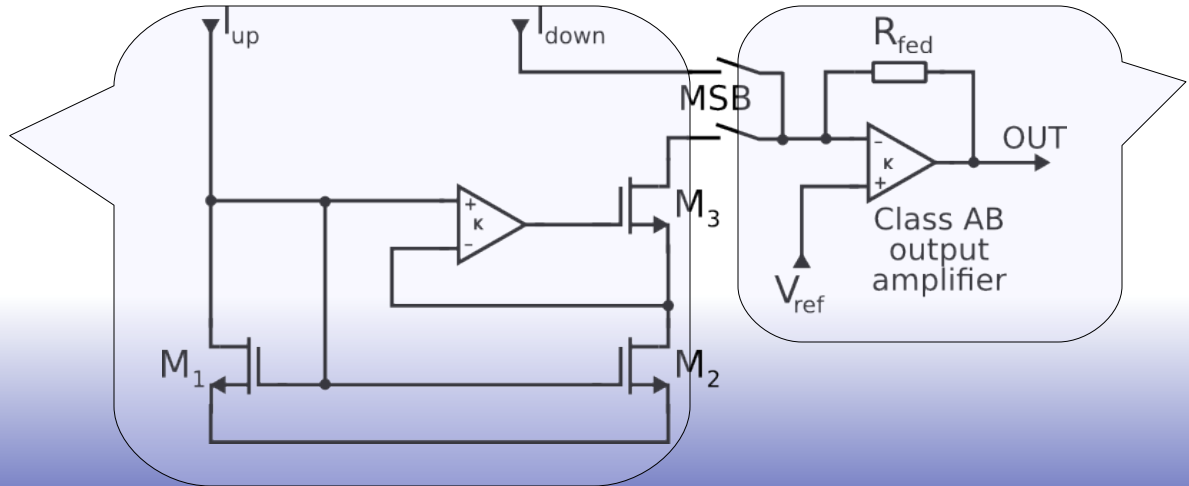


I-steering 10 bit DAC design



9 bit current DAC

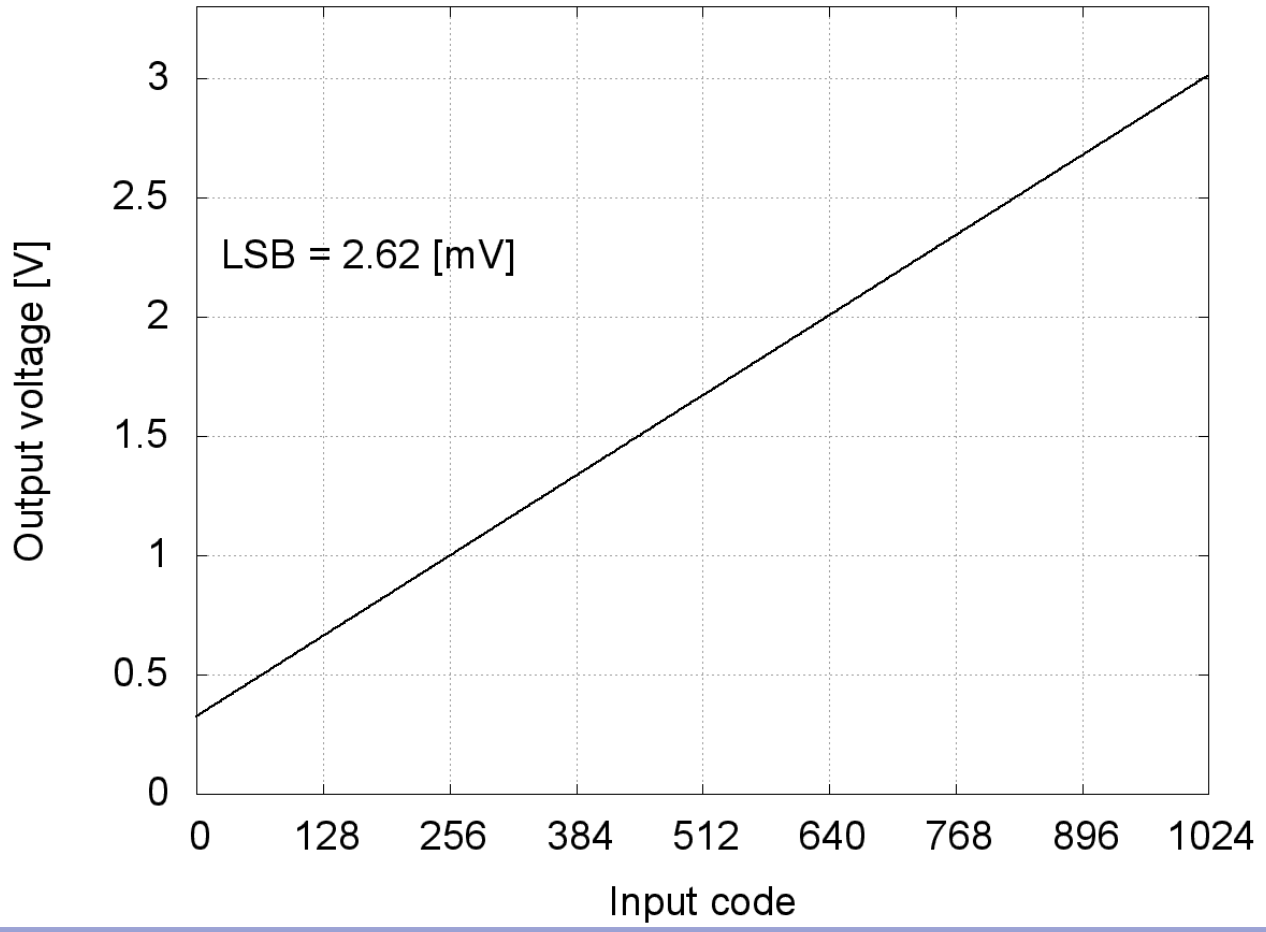
Current mirror

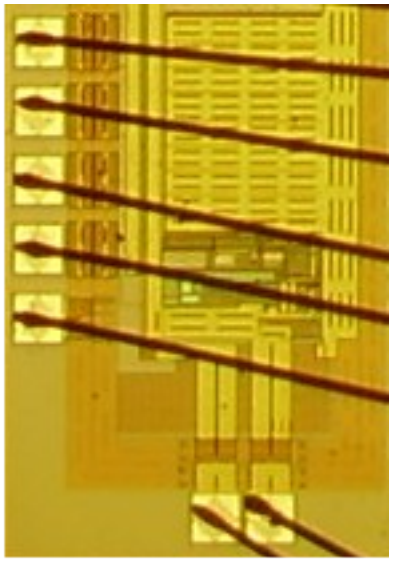


I-V converter with class AB output amplifier

DAC measurements

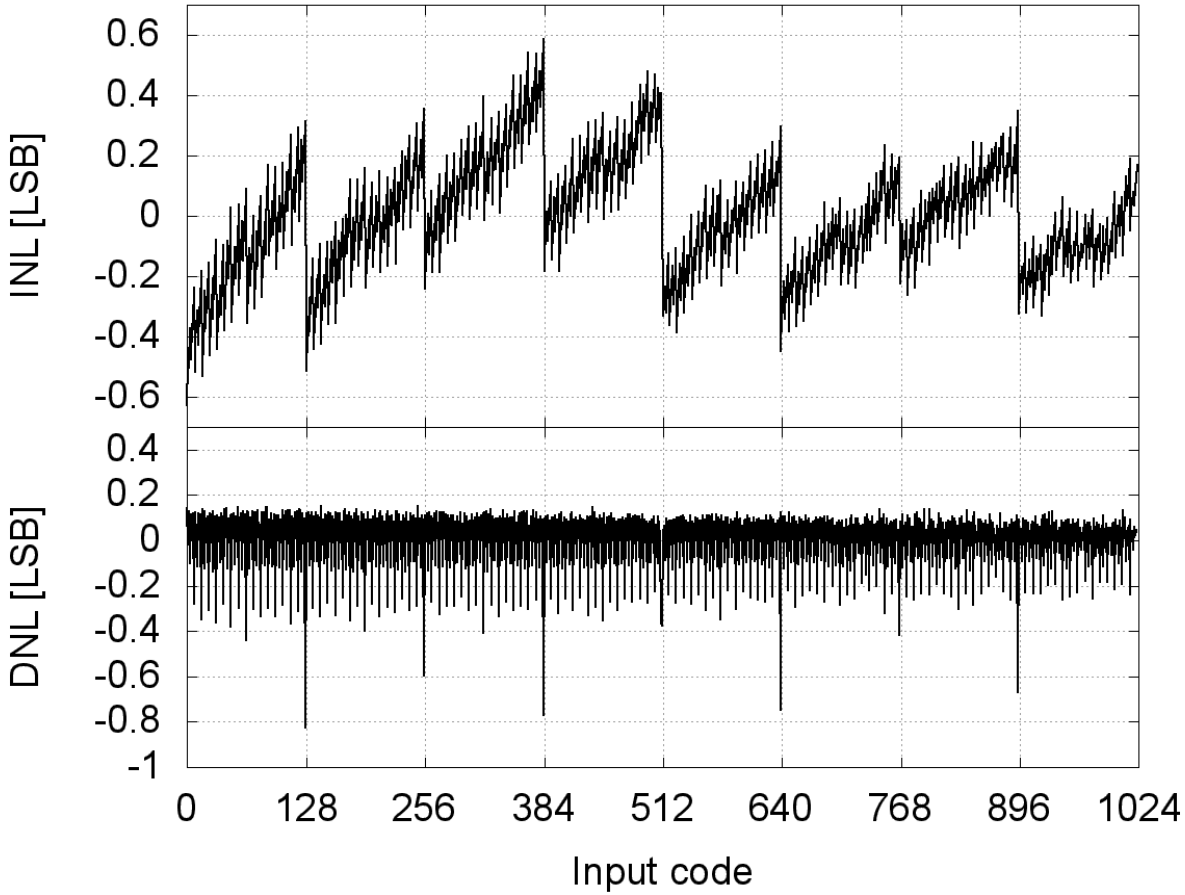
Transfer function





- 0.35µm CMOS
- Area 0.18mm^2
- Power <0.6mW

Static measurements



- INL measurements OK
- DNL generally OK, for few points worse than 0.5 LSB

Other designs in progress…

- Bandgap based reference voltage and thermometer circuits ready for submission
- Fast LVDS driver ready for submission
- Fast LVDS receiver ready for submission

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Summary

- Development of LumiCal Redout electronics in progress
  - Front-end prototypes tested
  - 10 bit ADC prototypes ready, first tests promising
  - 10 bit DAC prototypes tested
  - Other designs (Bandgap, LVDS) ready for submission
- Readout for PANDA straw tubes under study, real design work should start in the second part of 2009
- If possible components of LumiCal readout will be used in PANDA