

RICH Trigger Algorithm and Online Matching with MDC Tracks

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Outline

- Motivation
- The HADES Detector
- MDC- and RICH-Algorithms
- Implementation on the Compute Node
- Conclusion

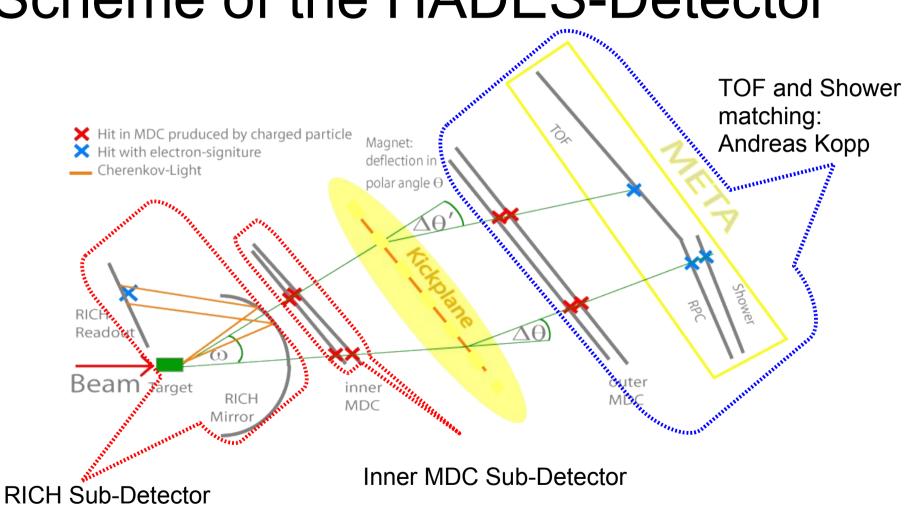


Motivation

- PANDA has lots of new and unforseen requirements
- We should be prepared as good as possible
- Learning from existing and running Experiments
- HADES as a testcase for PANDA (DAQ and Trigger)
- Real data is available
- Test during Beamtime end of 2009
- Learn how to use the Compute Node
- Transform or reuse parts of the algorithms

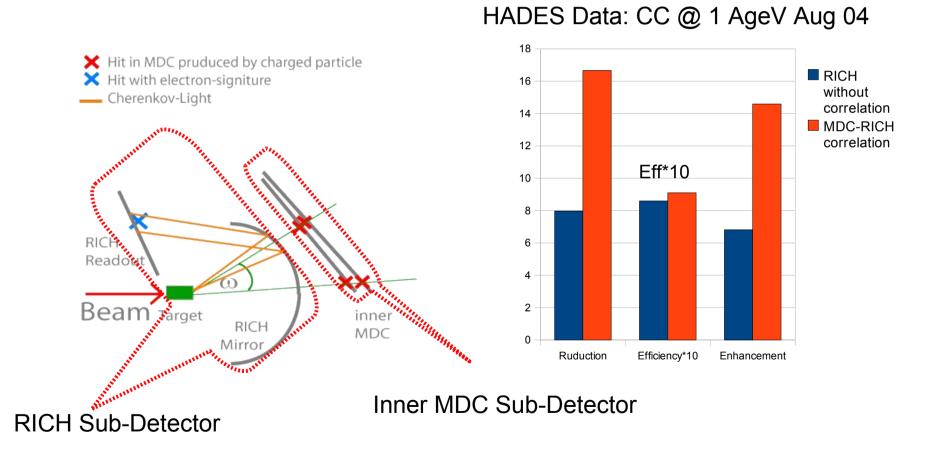


Scheme of the HADES-Detector



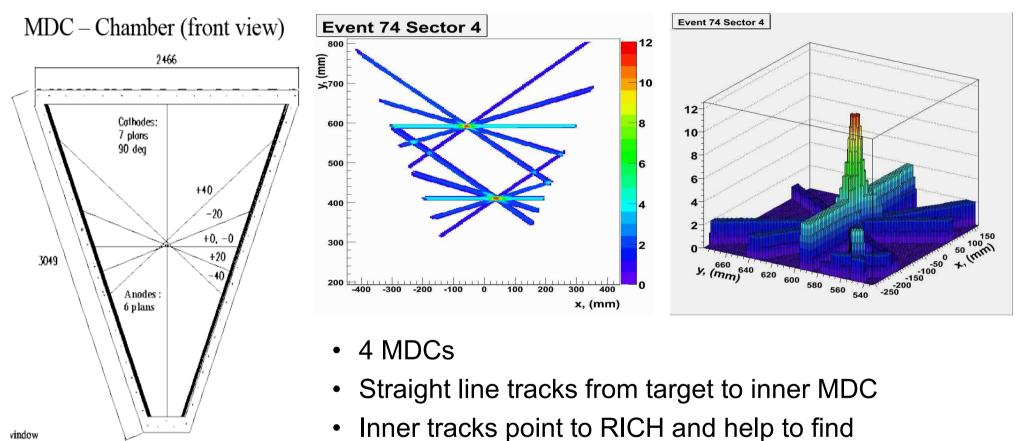


Scheme of the HADES-Detector





MDC Track Finder



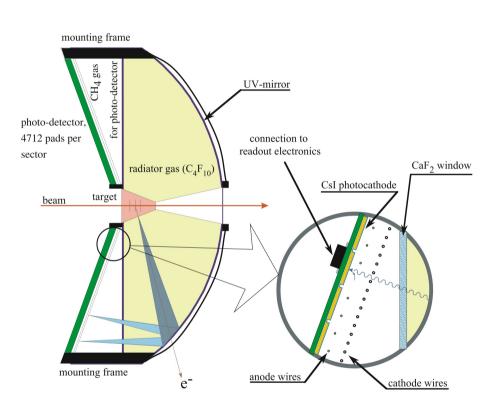
- 6 sectors
- 2110 wires per sector (inner)

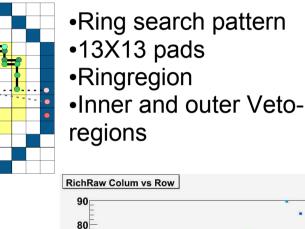
Implemented in Compute Node by Ming Liu

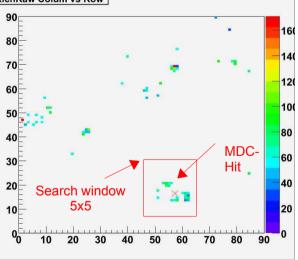
ringpattern



RICH Ring Finder







•Mirror reflects Cherenkov light •96*96 = 9216 pads/sector

- Pads shaped different
- Hadronblind

- •MDC points to a pad
- •Smaler searchwindow
- •Place mask on each pad in the window
- •Every pad in the window can be checked simultaneous

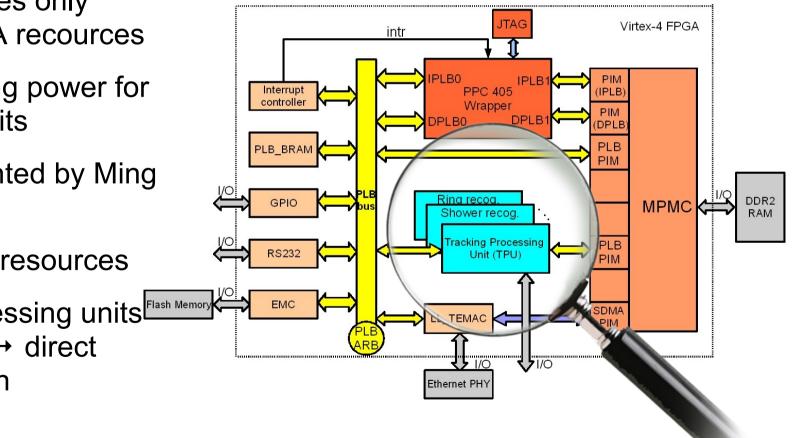


FPGA Design

- peripherals uses only ~22% of FPGA recources
- Most computing power for processing Units
- TPU implemented by Ming Liu

uses <20% of resources

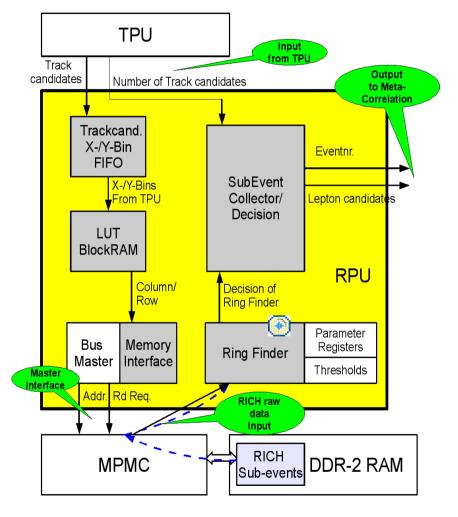
 Different processing units Flash Memory in one FPGA → direct interconnection



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UNIVERSITÄT **Ring Processing Unit**



- To be ported to FPGA (Vertex 4)
- Direct interconnection to Track processing unit and Meta processing unit or Eventbuilder
- RICH raw data bufferd in DDR-2 RAM
- MDC to RICH LUT stored in BlockRAM – maybe DSP-Slices used for calculation
- Many RPUs operate in parallel •
- Implementation work in progress



Conclusion

- Online Matching of subdetectors possible and mandatory for future experiments
- Compute Node provides necessary compute power and high bandwith
- PANDA could benefit from the experience made with HADES



Thanks for your attention