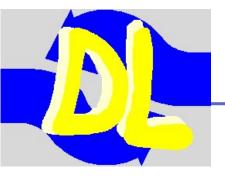
FAIR Facility for Antiproton and Ion Research

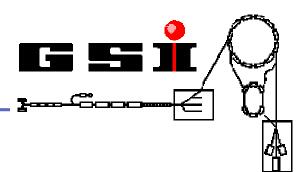
Status of the n-XYTER and CBM-XYTER development line

Christian J. Schmidt et al., GSI Darmstadt



GSI, Darmstadt, Feb. 11th 2009



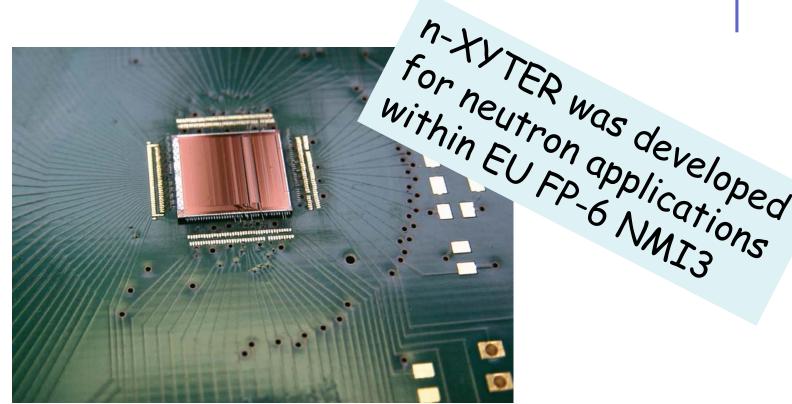


n-XYTER: Novel FE-Chip Architecture Cast in Silicon

Architectural Solution for FAIR CBM and PANDA. Starting point towards a FAIR dedicated XYTER front-end ASIC Our work-horse readout ASIC for detector prototyping

detector readout ASIC for high-density and high statistical rate time and amplitude measurement

- 128 channels @ 50.7 µ pitch
- freely running,
 - self triggered, autonomous hit detection
- 850 (1000) ENC at 30 pF
- dynamic range for 6 MIPs (300µ Si)
- positive and negative signals



- Per channel analogue energy and digital time stamp FIFO (1ns resolution)
- De-randomizing, sparsifying Token Ring readout at 32 MHz



n-XYTER, current workhorse chip for detector prototyping

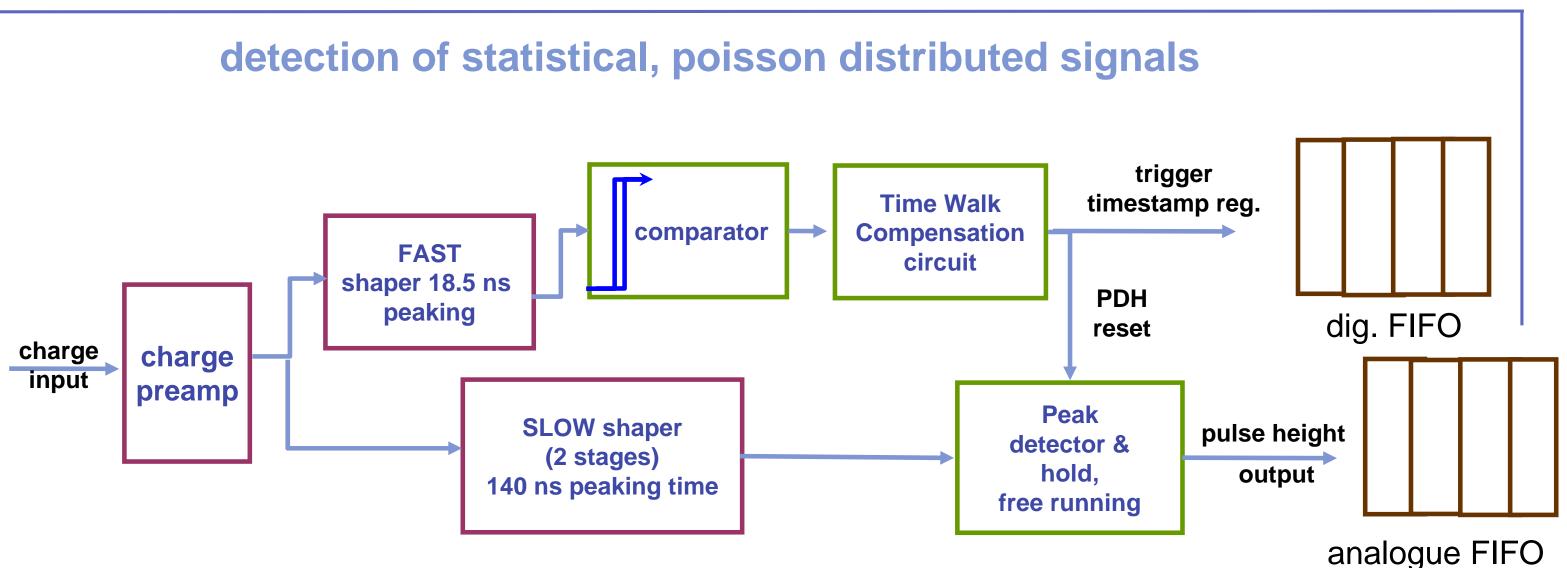
architectural example front-end for DAQ development

- self triggered autonomous hit detection,
- sparcifying, synchronous readout through token-ring
- sample ASIC for technological front-end electronics hybrid developments
 - bonding technology, circuit board technology
 - thermal management, active cooling concepts
 - power management (integrally high currents, low voltage, high B-fields, high rad. environment)
 - very dense mechanical boundary conditions

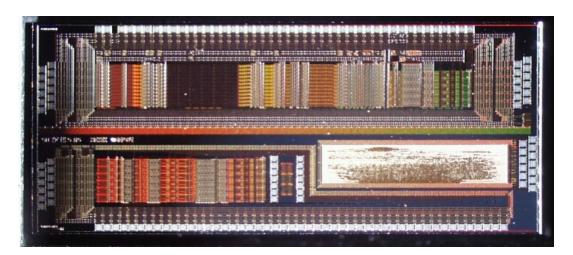




Data Driven Front-End: Asynchronous Channel Trigger



Asynchronous registry and storage in 4-level fifo guarantees data loss < 4 % when read-out through token ring



The DETNI ASIC 1.0, a front-end evaluation chip in AMS 0.35µ

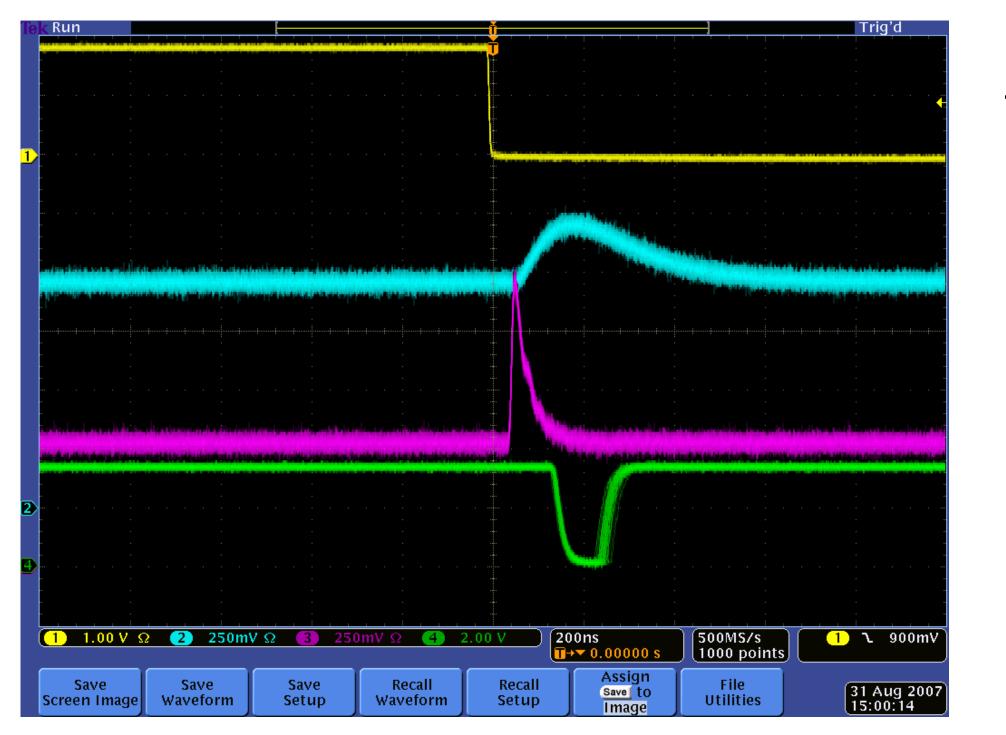


Detectors for Super FRS, GSI, Feb. 11th 2009





Analogue Signal Sequence (Test Channel)



Slow Shaper

Fast Shaper



Detectors for Super FRS, GSI, Feb. 11th 2009



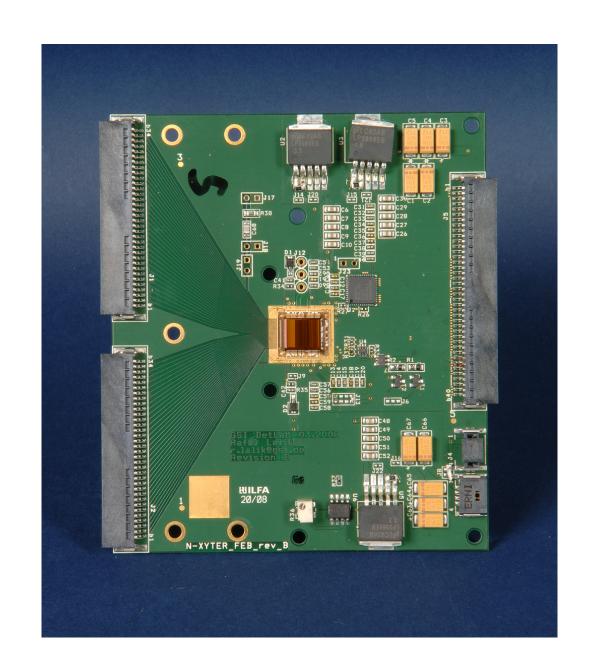
Testpulse Release

Discriminator Output



"Simple" FEB for the n-XYTER Starter Kit

- A simple hybrid PCB with signal fan-in, ADC and interconnect to SysCore DAQ chain
- Allow development of the DAQ chain
- Allow the readout of various detector prototypes
- Allow to explore the challenges of hybrid development



The September beam time has shown the whole signal chain operative!

Silicon Strip / GEM Gas Detectors --- n-XYTER --- SysCore DAQ System



Currently 10 FEBs available!

Detectors for Super FRS, GSI, Feb. 11th 2009

ative! Core DAQ System

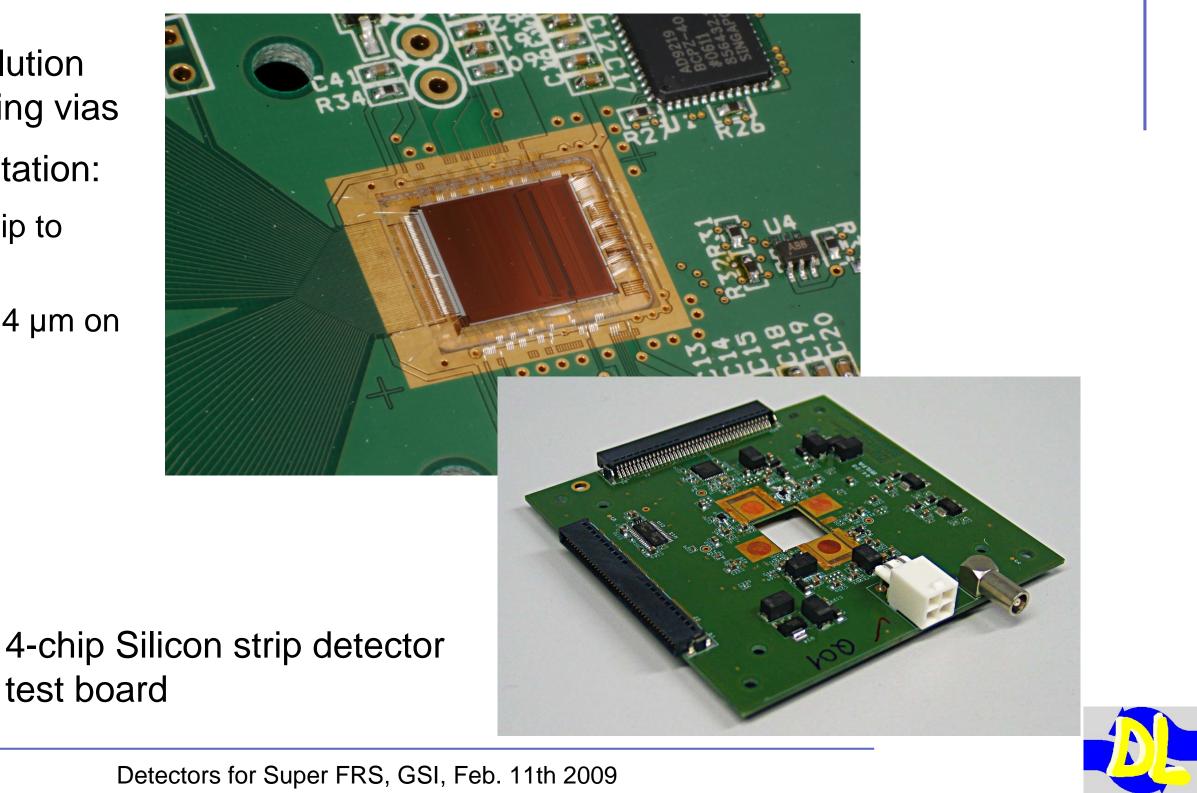


n-XYTER FEB: At the limits of PCB-technology

Interference point of several technologies,

each imposing limiting boundary conditions:

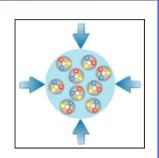
- Chip-In-Board solution avoids space eating vias
- allows pitch adaptation:
 - 50,7 µm on chip to
 - PCB side 101,4 µm on two levels





Detectors for Super FRS, GSI, Feb. 11th 2009

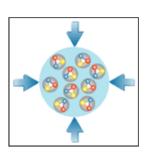




STS specific hybrid developments

- Hybrid for STS Silicon Detector Ladder Modules
- Combined challenges of
 - high density chip assembly needs
 - sensitive micro-cable detector interconnect
 - integrated cooling
 - integrated powering scheme in high magnetic fields and rad. env.
 - Tentatively, a completely different technology comes into play:
 - Silicon based circuit board
 - flip-chip assembly of XYTERs
 - high efficiency cooling contacts and hybrid stackability
 - tap-bonding for micro-cables (V. Pugatch, Kiev)







Activities in Heidelberg: Preparation of n-XYTER engineering run

An Engineering Run of the n-XYTER will supply us with chips for detector prototyping activities!

Towards this production, some issues may be addressed.

- n-XYTER prototype showed a large temp. coeff. due to unmatched circuitry assembled from different labs (DETNI collaboration). The correction of it is the major modification currently realized.
 - A process more suited for mixed signal designs will be employed
 - Rearranged bond-pad lay-out will facilitate bonding
 - Enhanced on-chip shielding will inhibit cross-talk and inter circuit feed-back
 - two versions of dynamic range (120 000 e, 1000 000 e) will widen scope of applications



Hans K.Soltveit, Physik. Inst. Heidelberg

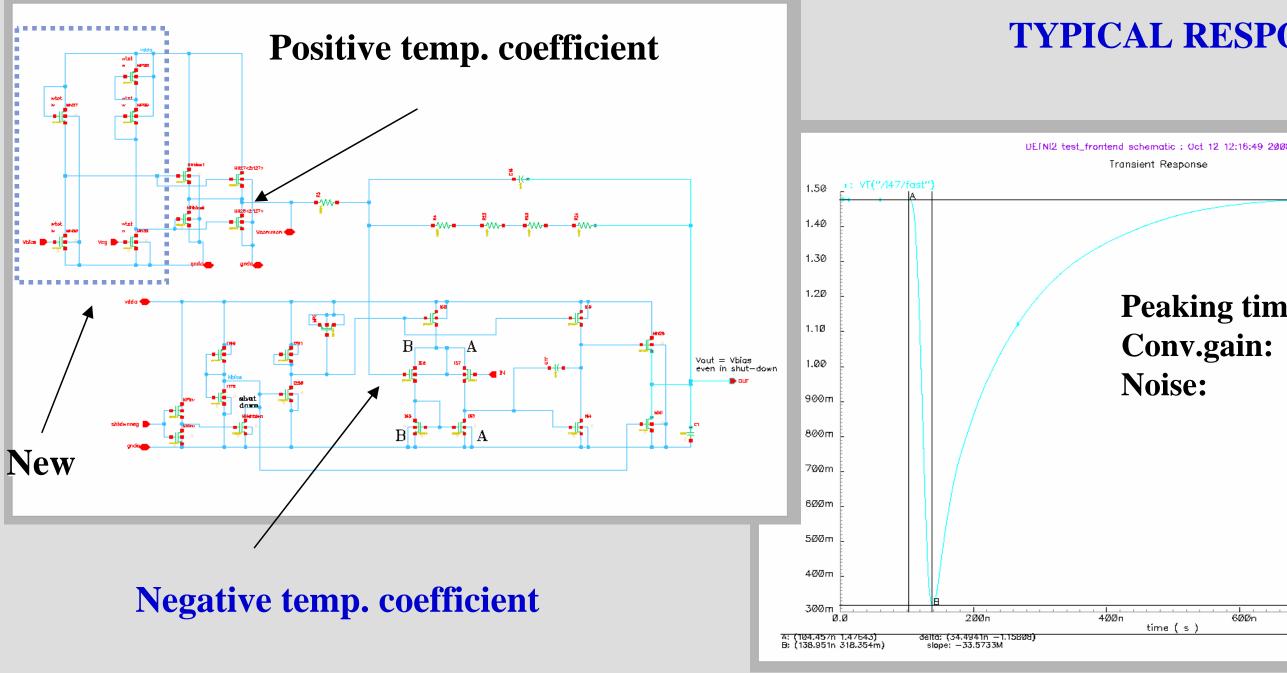
Detectors for Super FRS, GSI, Feb. 11th 2009



TEMPERATURE SENSITIVITY

Additional compensating circuitry added to undo former TC-mismatch

FAST SHAPER Reworked (preliminary)





Hans K.Soltveit, Physik. Inst. Heidelberg

Detectors for Super FRS, GSI, Feb. 11th 2009

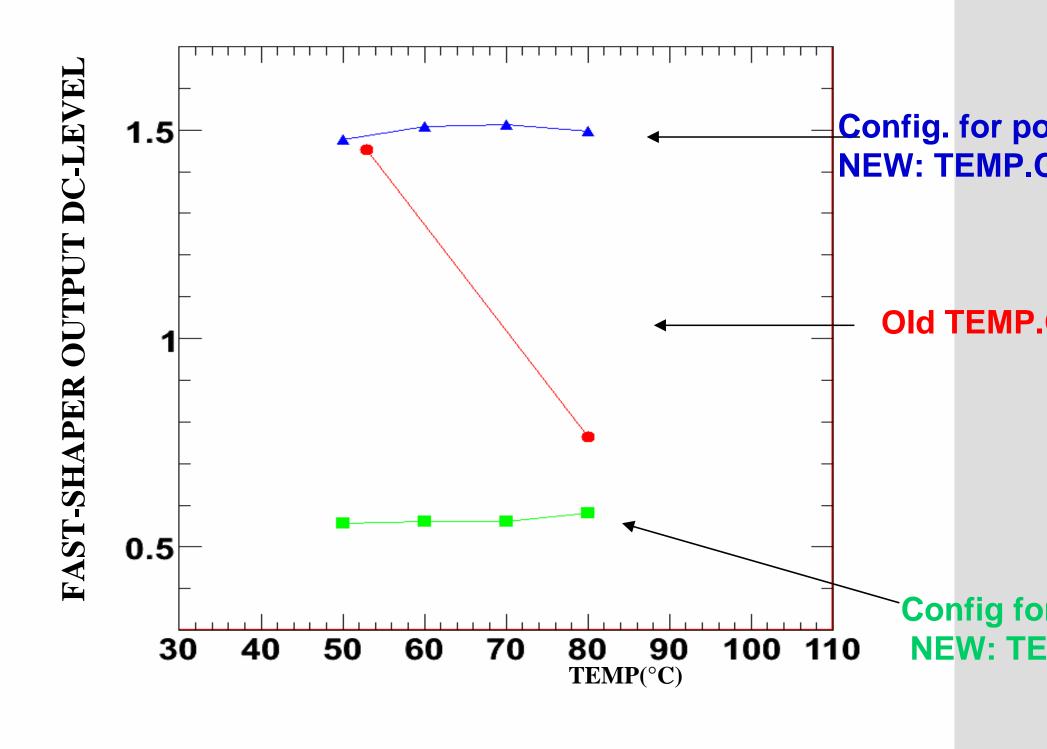
TYPICAL RESPONSE

П

Peaking time: ~35ns **Conv.gain:** 59.7mV/fC 766e@30pF

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TEMPERATURE SENSITIV



Hans K.Soltveit, Physik. Inst. Heidelberg

Detectors for Super FRS, GSI, Feb. 11th 2009





Config. for positive input signals NEW: TEMP.COEFF. ~0.5 mV/°C

Old TEMP.COEFF. ~29 mV/°C

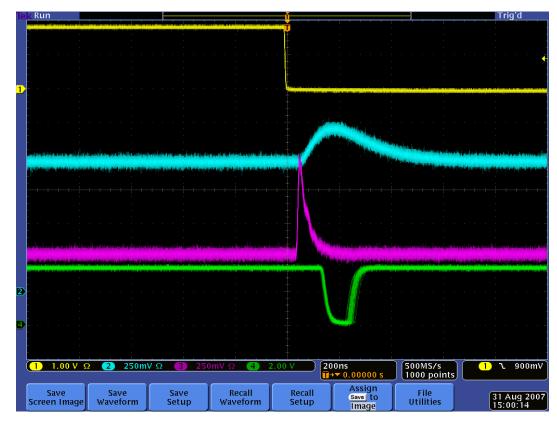
Config for negative input signals NEW: TEMP.COEFF. ~0.7 mV/°C

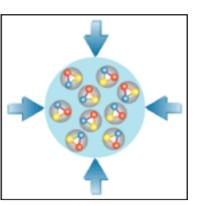


Midterm and Beyond, the CBM-XYTER

A dedicated CBM-XYTER development gets on its rails...

- Exploit detector prototyping experiences
- Self triggered architecture
- Rates adapted
- Radiation hard
- On chip energy conversion
- Efficient, low lead-count serialized data transfer
- DC-coupled double-sided Silicon readout







Dedicated XYTER Development for FAIR

Generic n-XYTER architecture finds broad applications within FAIR: CBM Silicon Strips STS, PANDA High Rate GEM TPC as well as large area gas detectors (micro structures or wire chambers)

Twin chip development with XYTER architecture and diversities for:

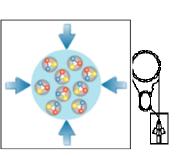
Silicon Strip MIP detection with time over threshold analogue architecture

TRD electronics:

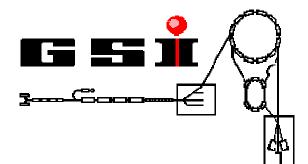
Larger dynamic range,

ion tail cancellation specialties

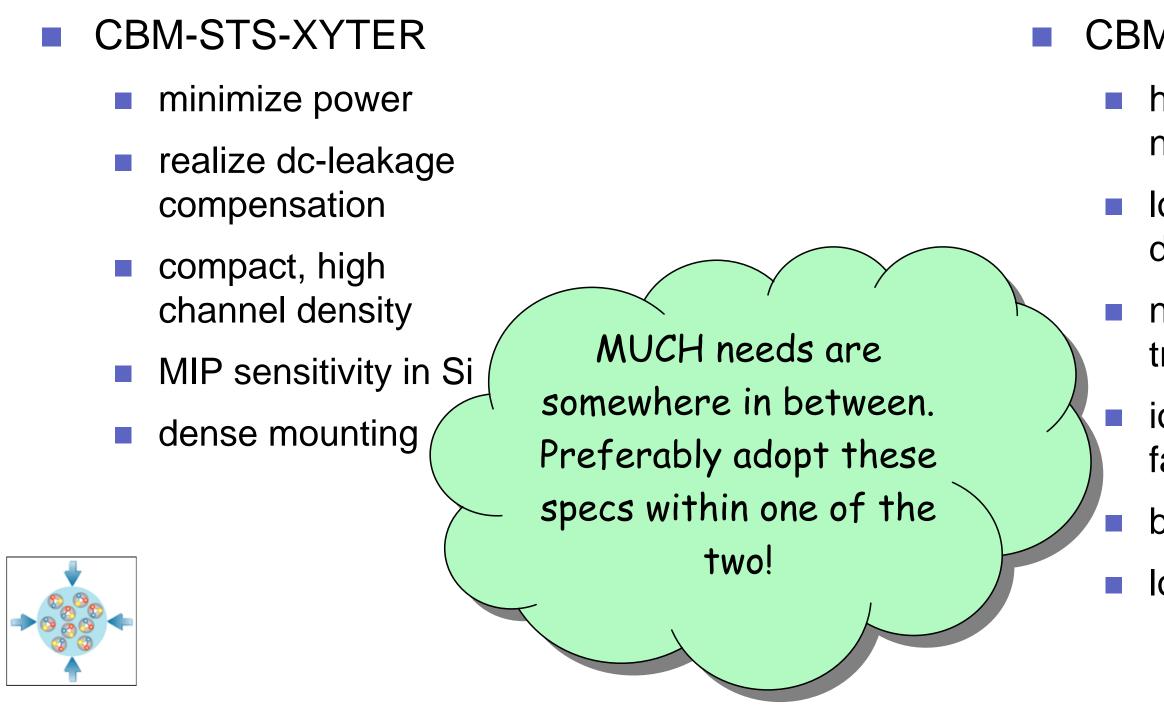
- Radiation hard design in UMC 0,180 µm (better than 10 MRad)
- Minimized power consumption
- Integration of modern, low power ADC on chip \rightarrow purely digital interface
- Highly multiplexed data interface (minimize cableing)
- Optimized system synchronization capabilities
- **SEU** tolerance
- Detector DC coupling capability
 - Dense mounting capability







CBM-XYTER Family Planning



Both XYTER chips will employ common rad. hard library and common design blocks for the readout FiFo and MUX (data sparcification and de-randomization), slow control interface, data transfer serializers, testability features and clocking and time stamp generation.

CBM-TRD-XYTER

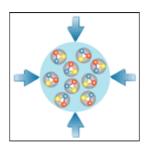
- high resolution needs (8 to 9 bit)
- lower channel density
- next neighbor forced trigger logic?
- ion tail cancellation facilities
- baseline restoration
- lower occupancy



CBM-STS-XYTER

- Robert Szczygiel and Pawel Grybos (AGH Krakow) will realize the job. (They share experience on the n-XYTER development within DETNI)
- Pre-study ongoing
- MIP sensitivity with around 120 000 e dynamic range
- 128 channels, high density
- Time over threshold (TOT) architecture
 - extremely power saving due to less architectural overhead
 - low resolution needs, 4 to 5 bit
 - low demand on silicon real estate
- Particular demands on S/N for clean discrimination







- Peter Fischer et al. (ZITI Heidelberg) embarked on the realization of this chip,
- specific architectural needs for the TRD-XYTER have not entirely crystallized yet.
- Concerted workshop on FEE needs in Dec. 2008
 - with detector physicists
 - and electronics engineers to work out the TRD-XYTER spec-frame





Assessment of specifications ongoing since Dec. 08

χ fulps in system12k n_{ch} sys/n _ ch cpi5k32k-8kpower limit/chanel12k $M/128$ chanels10mW10mWnoise limit $M/128$ chanels10mW500e500emax.nd.obs $M/128$ chanels $M/128$ chanels100kma500emax.nd.obs $M/128$ chanels $M/128$ chanels $M/128$ chanels500emax.nd.obs $M/128$ chanels $M/128$ chanels $M/128$ chanels $M/128$ chanelsmax.nd.obs $M/128$ chanels $M/1288$ chanels $M/1288$ chanels $M/1288$ chanelsmax.nd.obs $M/1288$ chanels $M/12888888888888888888888888888888888888$						_		
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with the set of the	32-128	32-128	64 - 256, def.:128	128 or 64	128?	8-16?	128?	#channels/chip
power limit/channel $($	100k	100k	700k	200k-1000k/?			1.5M	#channels in system
Anise of the set	32k-8k		5k	n_ch_sys/n_ch_chip			12k	#chips in system
max. rad. dose100 krad ?100krad ?avg. detector cap. $35pF$ $10 pF$ $10pF$ $7pF$ max. detector cap. $< 100 F$ $50pF$ $2300pF$ $7pF$ nex. detector cap. $< 100Hz$ $< 100Hz$ $250Hz$ $310Hz$ $2300pF$ event rate < 1000 $< 1000/hamber ~3 ch per hit$	10mW	10mW	1W/128channels	1W/128 chan??				power limit/channel
And the constraint of the const	500 e-	500e-		~1500 electrons (sigma)				noise limit
nax. detector can nax. detector can shear term 1000 1000 1000 $1000/chamber 3ch perh10001000/chamber 3ch perh10001000/chamber 3ch perh10001000/chamber 3ch perh1000/chamber 3c$		100krad		100 krad ?				max. rad. dose
And the set of t	7pF		10pF	10 pF			35pF	avg. detector cap.
Anti-tic for the strength Anti-tic for the strength Anti-tic for the strength $hits/here 150Hz 250Hz 260Hz 4.11/200Hz 200Hz average signal and person \Lambda \cdot 4C 200C 150-300 ke 150Hz 160Hz 4.11/200Hz 200Hz average signal and person \Lambda \cdot 4C 200C 150-300 ke 160Hz 160Hz 4.01/200Hz 4.01/200Hz $	7pF	2/300pF	50pF	50 pF				max. detector cap.
nx. hit rate/channel 150kHz 250kHz? 250kHz? 250kHz 4.11/200kHz 200kHz average signal ampi, ~4fC 20fC 150-300 ke 15fC 4fC 4fC signal distribution Landau exp. exp.? mix Landau and Exp. Landau	2.5 MHz		<=10MHz	< 10 MHz			<=10MHz	event rate
Average signal ample Av4fC 20fC 150-300 ke 15fC 4fC signal distribution Landau exp. exp.? mix Landau and Exp. Landau Landau Landau measured quality spat. res. spat. res. hit/no hit spat. res. spat. res. spat. res. dep. on det. type spat. res. spat. res. rect. 30-40 ns max. poss. signal some MIPs 20fC * 10 2-4Me 169ke 200ke 120fC ADC res./amplitude E Time resolution 10ns/hit 4ns/hit 4ns/hit				1000/chamber ~3 ch per hit			1000	hits/event
Signal distributionLandauexp.exp.?mix Landau and Exp.LandauLandauLandaumeasured qualityspat. res.spat. res.hit/no hitspat. res.spat. res.spat. res.spat. res.spat. res.spat. res.spat. res.spat. res.rect. 30-40 nsfinax. poss. signalsome MIPs20fC * 1020fC * 1020fC * 10rect. 30-40 ns109 nc100 ncADC res./amplitudeET57-8 bit100 nc100 nc100 nc100 ncTime resolutionEEE100 nc100 nc100 nc100 nc	200kHz	411/200kHz	40kHz	250kHz	250kHz?		150kHz	max. hit-rate/channel
measured qualityspat. res.spat. res.hit/no hitspat. res.spat. res.	4fC	15fC		150-300 ke		20fC	~4fC	average signal ampl.
signal shape dep. on det. type rect. 30-40 ns max. poss. signal some MIPs 20fC * 10 2-4Me 169ke 200ke 120fC ADC res./amplitude f 5-5 bit 5-8 bit 0.8 fC 0.8 fC Time resolution i <t< td=""><td>Landau</td><td>Landau</td><td></td><td>mix Landau and Exp.</td><td>exp.?</td><td>exp.</td><td>Landau</td><td>signal distribution</td></t<>	Landau	Landau		mix Landau and Exp.	exp.?	exp.	Landau	signal distribution
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ADC res./amplitude 7 - 8 bit 0.8 fC Time resolution 10ns/hit 4ns/hit	rect. 30-40 ns			dep. on det. type				signal shape
Time resolution 10ns/hit 4ns/hit	120fC	200ke	169ke	2-4Me		20fC * 10	some MIPs	max. poss. signal
	0.8 fC			7 -8 bit				ADC res./amplitude
special tasks baseline res. spark prot. spark prot.	4ns/hit	10ns/hit						Time resolution
	spark prot.			spark prot.		baseline res.		special tasks



