Detector Control System board for FAIR

J. A. Lucio Martínez
Infrastructure and Computer Systems in Data Processing (IRI)
Goethe University Frankfurt

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Challenge

- FAIR uses EPICS
- All Components and actuators need to be integrated to EPICS
- No cave access during / directly after beam
- Components need to be added manually if no default interface is included
- Radiation environment forces special assurances for some scenarios

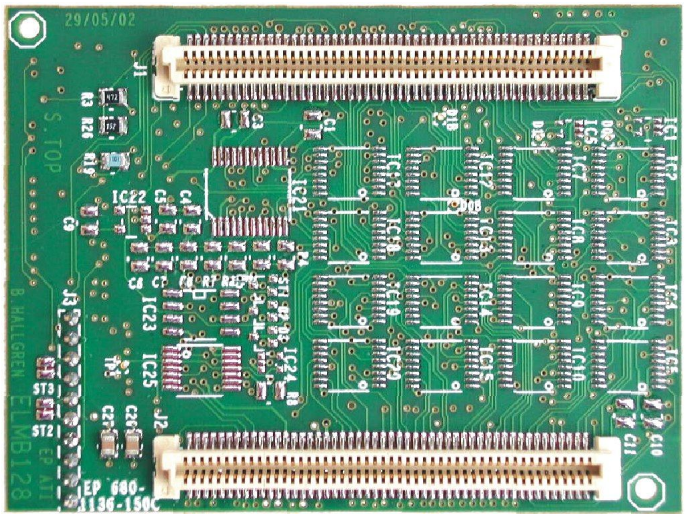
Solution: DCS Board

- Ensure optimal operation of the experiment
- Integration of connected digital / analog sensor data
- Monitor sensors and control actuators:
  - Temperature
  - Cooling status
  - Amplification adjustment
  - Bias voltages used by particle detector sensors
- Operation in radiation environment and strong magnetic field by selection of adequate components
- Maybe provide basic sensors on board

Example: DCS @ CMS and ATLAS

Information from B. Hallgren et. al.
The Embedded Local Monitor Board (ELMB) in the LHC Front-end I/O Control System

- *Embedded Local Monitor Board*
  - *Intelligence provided by 2 x AVR ATMEL ATmega3L 8 bit*
  - *AT90S2313 for in System programming*
- *Simulation of 10 years of operation @ Atlas Muon MDT detectors yield:*
  - *TID: 6,4 Gy*
  - *Single Event Effect (SEE): 4,8 x 10^{10} hadrons/cm^2*
- *It has been shown that by using COTS a certain level of radiation tolerance can be achieved*
- *Not suitable for FAIR*



Example: DCS @ CMS and ATLAS

Not suitable for FAIR

- Error detection relies on CAN CRC, Message Frame Check, Monitoring and Bit stuffing
- Not specified if error detection mechanism can be run parallel to normal tasks or if it runs just in testing routines
- Errors may happen in internal RAM and might propagate as program execute without being detected
- Bit flips must be detected as soon as they occur
- No redundancy to detect fail in instruction execution
- 8 bits, 4 MHz only :-)

Outline

- Requirements for DCSB Integration
- CortexR4/5F – TI TMS570
- RTEMS/EPICS compatibility
- Beam-Test
- DCS board Realization
- Recap

Step beyond: DCS Board Processor

Requirements for DCS board COTS processor

1

Real Time OS:
Scheduling to comply with Real Time requirements/ schedule processes by Priority, MCU Cortex-R4F optimized for Real-Time operation

2

Fault Tolerant features:
ECC Error correction for internal memories and parity check/ Cyclic Redundancy Check for peripheral memories with no performance cost

3

COTS Low cost MCU
Commercial Off The Shelf MCU Cortex-R4F for safety applications

4

Compatibility with current control system:
Use of EPICS is now widely spread. The MCU should be able to run this SCADA

Solutions comparison

	Cortex-R4F (TI-TMS570)	FPGA Solution	Cortex-A7	ATmega3L (ELMB slide 4)
Real Time optimized	●	●		
Fault-tolerant	●			
Low price	●		●	●
EPICS compatible	●	●	●	

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TMS570 safety features

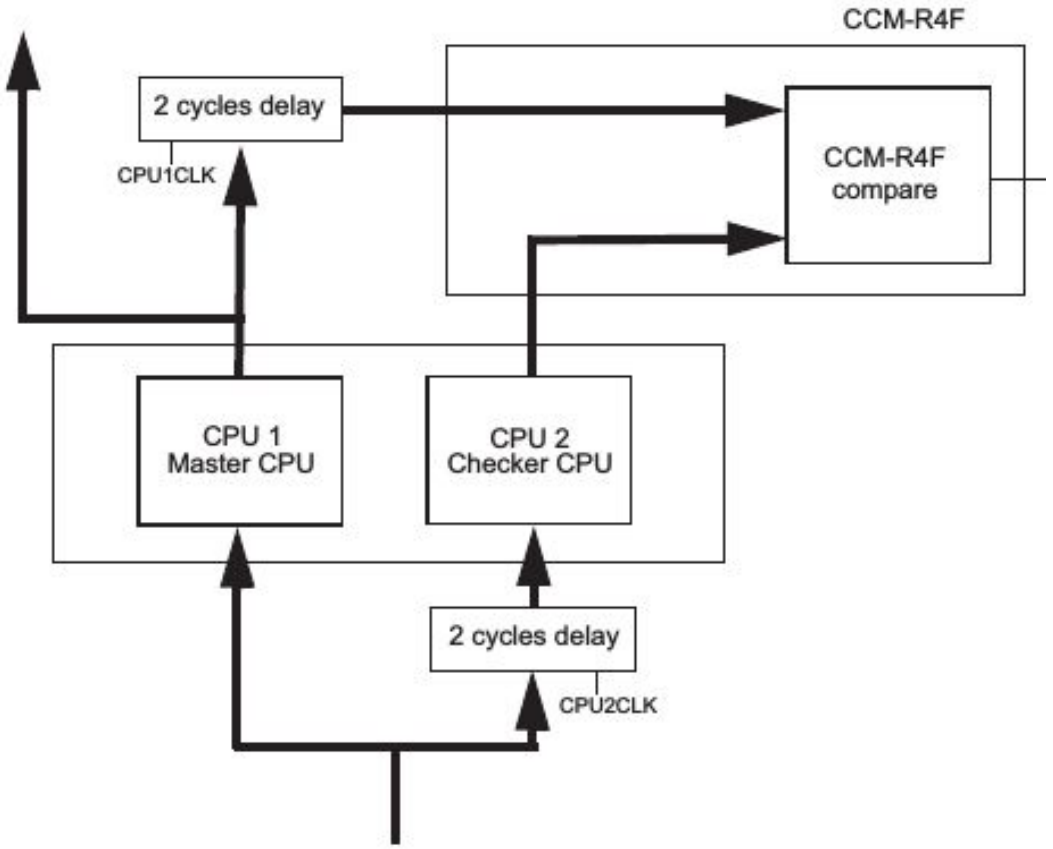

Figure from Texas Instruments:
Fig 9-1 SPNU499B August 2013

- 256/512KB ECC on tightly coupled internal SRAM
- 3/4 MB ECC on internal flash memory
- Dual lockstep running (DMR)
- CRC and parity check on peripheral memories
- ESM (Error Signaling Module)

TMS570 Specifications

	LS3137 - $33	LC4357 - $65
Processor	CortexR4F	CortexR5F
ADC Inputs	2x24 Inputs, 5 V, 12 Bits	1x32 + 1x24 Inputs, 5 V, 12 Bits
Interfaces	Eth,FlexRay,I2C,CAN,SPI,SCI	Eth,FlexRay,I2C,CAN,SPI,SCI
Interrupt GPIOs	16	16
GPIOs	101	145
Internal memory	3MB Flash+256 KB RAM	4MB Flash+512 KB RAM
External memory	16bit 128 MB	16bit 128 MB
Reset	µC CMD/nRST pin	µC CMD/nRST pin
Clock	180 MHz (Without Cache)	300 MHz (32 KB Cache)
Local Intelligence	Yes, incl. FPU	Yes, incl. FPU
Radiation Tolerance	Not 'officially' supported	Not 'officially' supported
Transfer Speed: Ctrl ↔ PC	10/100 Mbps (EMAC)	10/100 Mbps (EMAC)
Transfer Speed: Sensor ↔ Ctrl	1 Mbps (CAN), 10 Mbps (FlexRay)	1 Mbps (CAN), 10 Mbps (FlexRay)
Short -/ Long-Term Availability	yes	yes
Power (operating):ADC+prog.	341-652 mA (PoE Class 1)	683-1163 mA (PoE Class 2)

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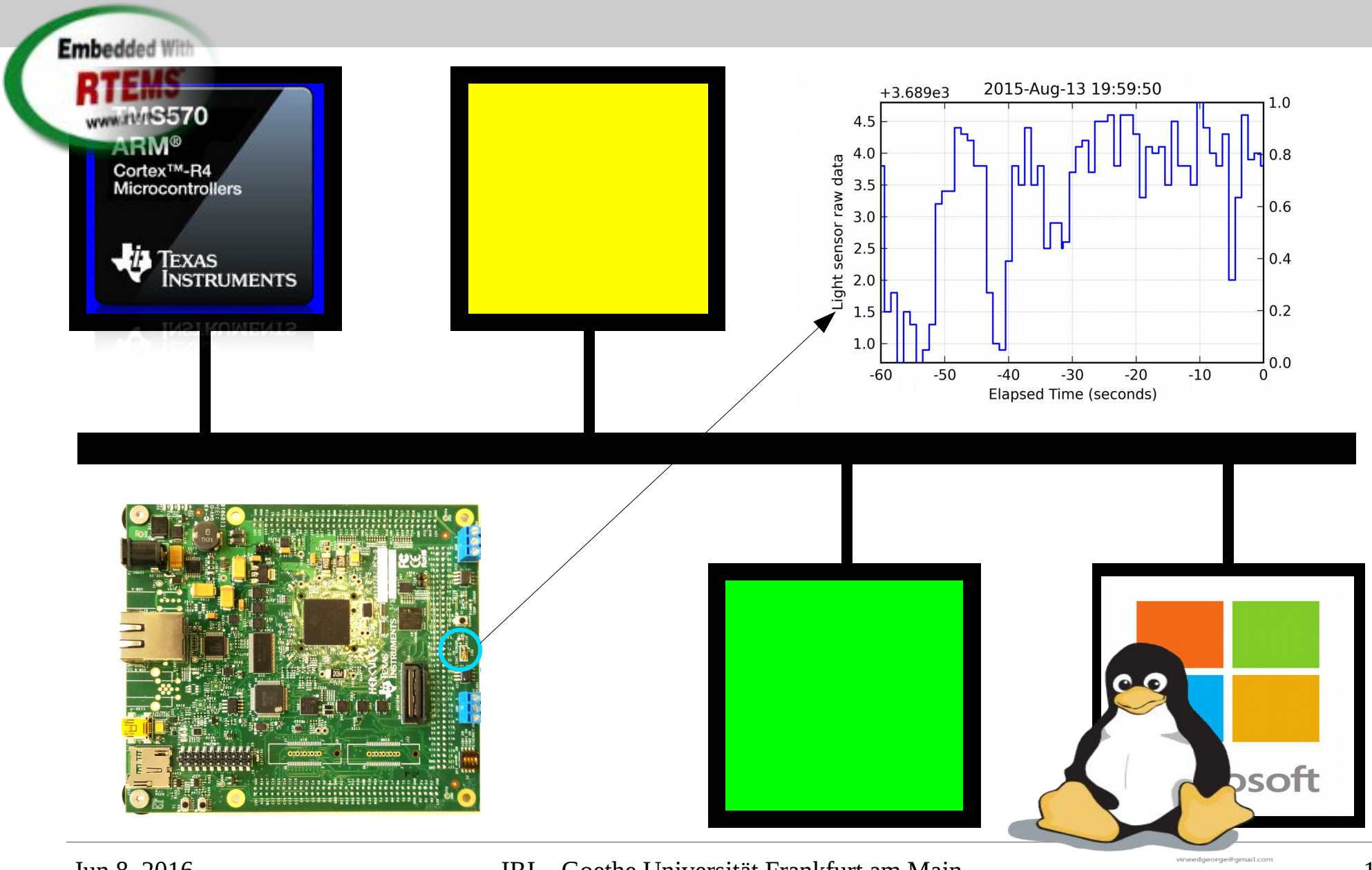
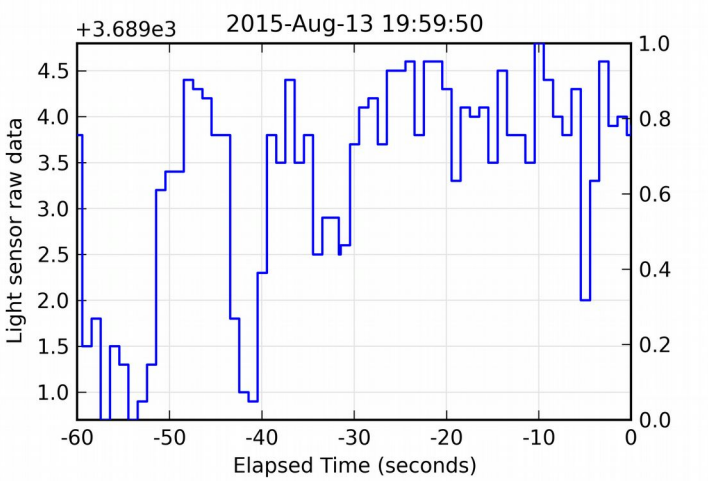
RTEMS/EPICS successfully ported to TMS570 Cortex-R4



EPICS Interfaces will be provided together with DCSB

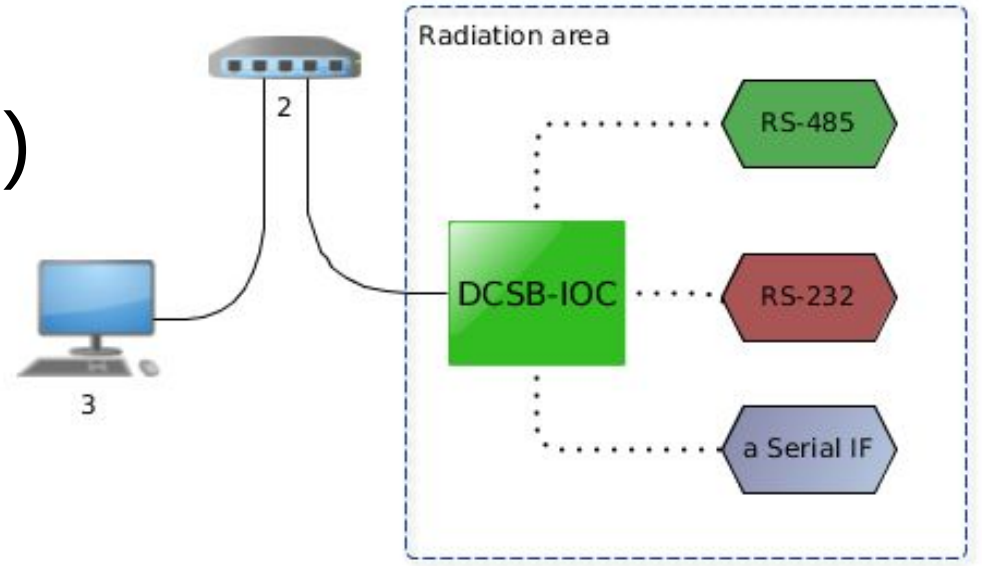
Example: EPICS ADC Integration



- devAiADC.c
  - Initializes ADC
  - ADC registers configuration
  - Extracts ADC value once
- aiADC.dbd
  - Declares a new analog input called devAiADC
- aiADC.db
  - Gives the record devAiADC a description of the value
  - Defines how often is the value scanned
  - Defines mathematical functions to process raw values

EPICS Interfaces will be provided together with DCSB

- Even more complex protocols supported via StreamDevice and ASYN applications
- Example: Serial Interface (tested on TMS570 RTEMS/EPICS version)



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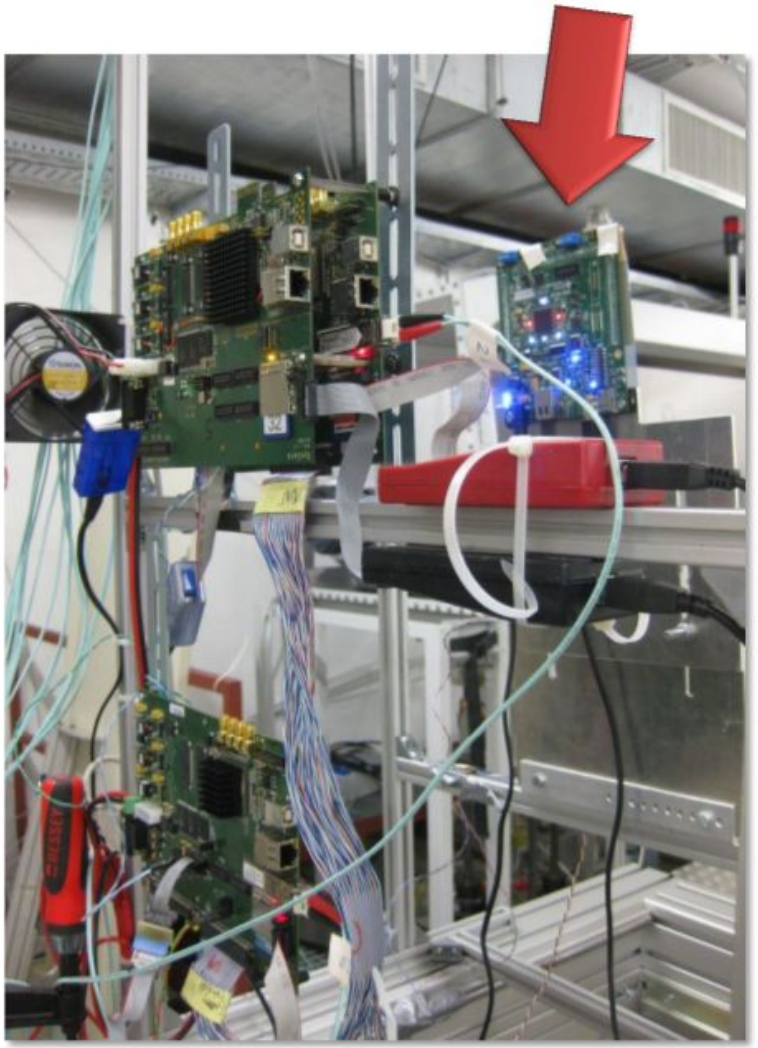
Beam-test for TMS570

Slide from Jano Gebelein
To SCA or not to SCA, February 2014

TMS570 Beamtest Results

- COSY Juelich
- July 2013
- Beam:
  - Protons
  - Momentum ~2.0 GeV/c
  - Intensity: ~$5 \cdot 10^6$ / ($s \cdot cm^2$)
- DUT: TMDX570LS31HDK with TMS570LS3137 Dual Pipeline ASIC µC
- Testdesign (Pritesh Gudge):
  - SRAM Memory Scrubber



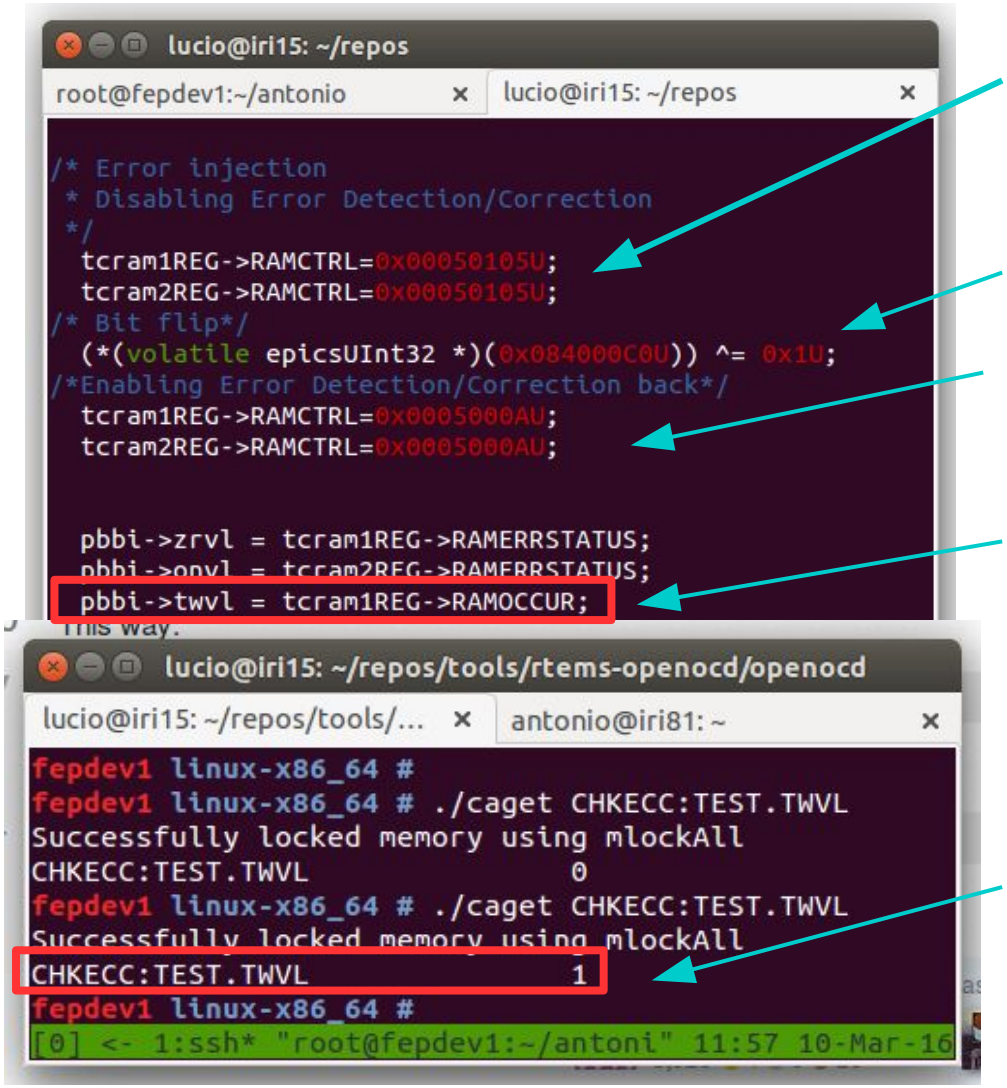
Beam-test for TMS570: results

Slide from Jano Gebelein
To SCA or not to SCA, February 2014

TMS570 Beamtest Results ctd.

- Total Operational Time in Beam: ~14 hours
- Total Resets: 11 (including both necessary/voluntary)
- Total SEUs Detected and Corrected: 13216
- Total Uncorrected Single-Bit Errors: 0
- Total Uncorrected Multi-Bit Errors: 5
- Conclusion:
  Valuable Candidate for DCS Board

TMS570 SRAM Error Injection as seen from RTEMS/EPICS



1)Disable Error Detection/Correction

2)Flip bit

3)Enable Error Detection/Correction

4)Monitor Single Bit Error Ocurrences Register (RAMOCCUR) with EPICS mbbi record twvl.

5)Injected error detected

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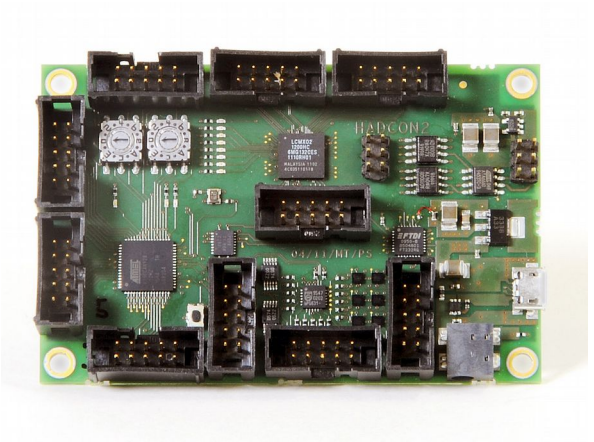
DCS Board Realization

- Take the best from available solutions



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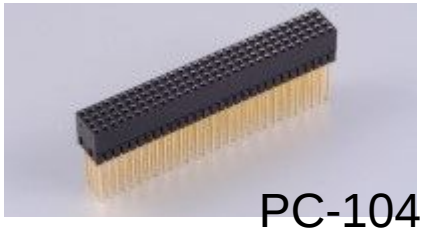
- HADCON2
  - Credit Card sized
  - EPICS support
  - I^2C, 2x4ch 8bit DAC, CAN, SPI, ADCs, RS232 (USB-FTDI)

- Add
  - Safety and radiation error mitigation mechanisms
  - Fast IF (10Mbit/s)
  - Up to 145 GPIOs
  - Fast soft Errors Detection through EPICS

DCS Board Realization

Brainstorming with: Marcel Steinen, Florian Feldbauer and Peter Zumbruch

- Requirements
  - Robust
  - Safe
  - Easy Configuration: Plug and Play: define a small module for a specific protocol to feed EPICS
  - Low Cost
- PC-104 Connector for stackable boards to use further interfaces (CAN, RS485) and Power.



PC-104

- PoE optional depending on if stackable board is providing power
- Additional Interfaces can be requested, please contact luciomar@iri.uni-frankfurt.de

Recap

- Safety Cortex-R4F/R5F is available as a low cost COTS device:
  - Supports Real Time applications
  - Second CPU improves fault tolerance
  - RTEMS/EPICS running well on it
  - Error accumulation within embedded memory mitigated (proven by beam test)
  - Supports multiple interfaces

→ DCS Board specification / schematics in progress

Thank you for your attention