Update on the Activities on PASTA

Alessandra Lai, Forschungszentrum Jülich, 7 June, 2016

Outline

JÜLICH FORSCHUNGSZENTRUM

PASTA Readout Chain

PASTA Configuration

Outlook

JDRS: Jülich Digital Readout System

The basic components

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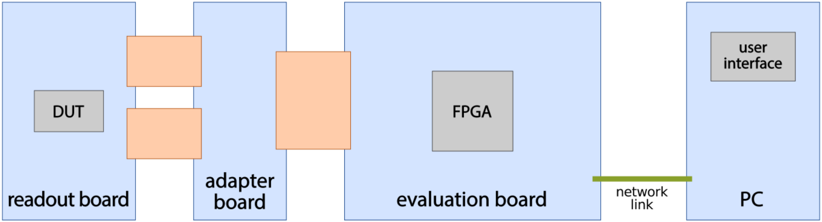
Jülich Digital Readout System (JDRS): same as for the ToPix chip.



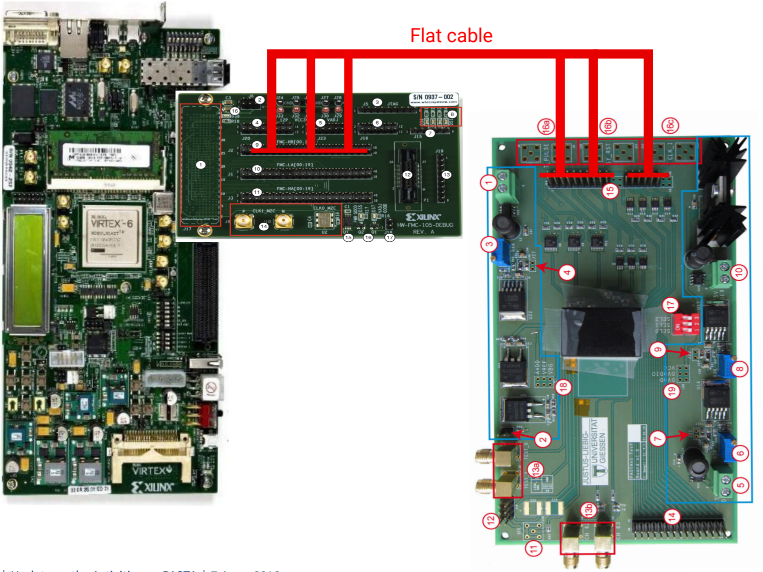
Data conversion and communication with the PC:

- DUT: ToPix, PASTA
- evaluation board: Xilinx ML605 (Virtex-6 FPGA)
- firmware: VHDL

Configuration and data handling:

- PC
- software: C++
- **MVD readout framework (MRF)**
- **Qt-based GUI**

The real set up



Preliminary operations

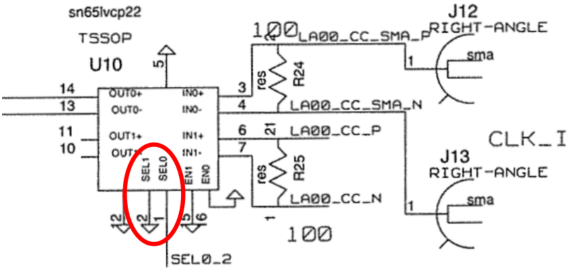
- Program in the firmware the physical connections between the readout board (PASTA) and the evaluation board (FPGA).
- Check with the oscilloscope if all the signals are routed correctly.

Pin #	Signal	FMC Signal Name	Pin #	Signal	FMC Signal Name
1	CLK_I +	LA00_CC_P	2	Sync_Reset+	LA10_P
3	CLK_I -	LA00_CC_N	4	Sync_Reset-	LA10_N
5	-	-	6	TEST_Pulse+	LA11_P
7	-	-	8	TEST_Pulse-	LA11_N
9	SDI +	LA02_P	10	-	-
11	SDI -	LA02_N	12	-	-
13	SCLK +	LA03_P	14	-	-
15	SCLK -	LA03_N	16	-	-
17	CS +	LA04_P	18	-	-
19	CS -	LA04_N	20	-	-
21	-	-	22	-	-
23	-	-	24	-	-
25	TX0 +	LA06_P	26	-	-
27	TX0 -	LA06_N	28	-	-
29	TX1 +	LA07_P	30	CLK_O+	LA17_CC_P
31	TX1 -	LA07_N	32	CLK_O-	LA17_CC_N
33	SDO +	LA08_P	34	-	-
35	SDO -	LA08_N	36	-	-
37	-	-	38	-	-
39	-	-	40	-	-

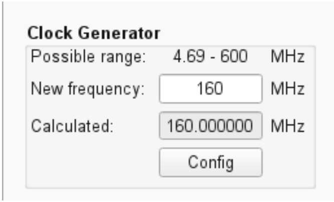
We found some small bugs mostly caused by the fact that the system was never tested together with the chip.

Connect PASTA to the readout chain

- Connect PASTA and send the 160 MHz clock $\longrightarrow$ no response.
- Problem: the clock does not reach the chip because of a wrong connection of the LVDS switches on the board.
- Solution: make the proper connection with a wire (for all the LVDS switches).

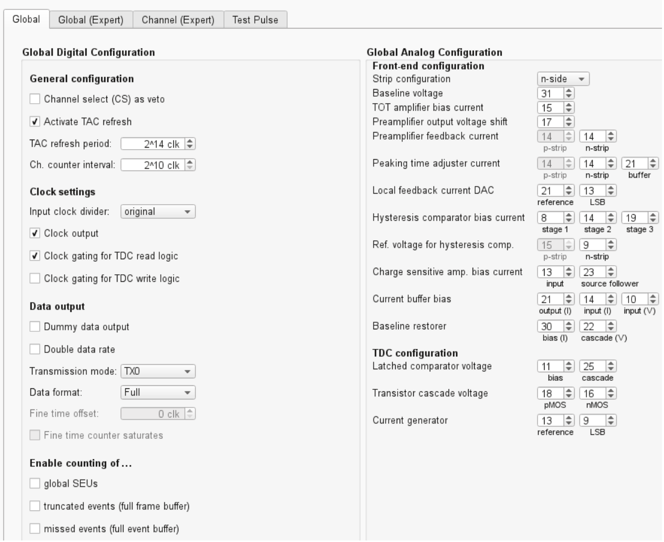


Current consumption



Clk	Digital (mA)	Analog (mA)	Service (mA)
60	23	107	300
80	27	107	300
100	30	107	300
120	33	107	300
140	36	107	300
160	39	107	300

Global Configuration I



Global Configuration II

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Global | Global (Expert) | Channel (Expert) | Test Pulse

Global Configuration

	Item	Pos	Len	Min	Max	Set Value	Read Value
1	BLR_Ib	137:141	5	0	31	30	30
2	BLR_Vcas	132:136	5	0	31	22	22
3	CB_Ib1	127:131	5	0	31	14	14
4	CB_Ib2	122:126	5	0	31	21	21
5	CB_Vbias	117:121	5	0	31	10	10
6	CSA_Ib1	112:116	5	0	31	13	13
7	CSA_IbSF	107:111	5	0	31	23	23
8	Comp_Vb	142:146	5	0	31	11	11
9	Comp_Vcas	147:151	5	0	31	25	25
10	HCGDAC+	99:102	4	0	15	15	15
11	HCGDAC-	103:106	4	0	15	9	9
12	HC_Ib1	94:98	5	0	31	8	8
13	HC_Ib2	89:93	5	0	31	14	14
14	HC_Ib3	84:88	5	0	31	19	19
15	IfDAC_Ilsb	79:83	5	0	31	13	13
16	IfDAC_Iref	74:78	5	0	31	21	21
17	Iref_cs	162:166	5	0	31	13	13
18	Iref_ratio_lsb	167:171	5	0	31	9	9
19	PREAMP_Ifn	69:73	5	0	31	14	14
20	PREAMP_Ifp	64:68	5	0	31	14	14
21	PREAMP_Ishift	59:63	5	0	31	17	17
22	PTA_Ibn	54:58	5	0	31	14	14
23	PTA_Ibp	49:53	5	0	31	14	14
24	PTA_Ibuf	44:48	5	0	31	21	21
25	TAC_refresh	4:7	4	0	15	3	3
26	ToT_Ib	39:43	5	0	31	15	15
27	Vcas_n	152:156	5	0	31	16	16
28	Vcas_p	157:161	5	0	31	18	18
29	baseline_voltage	33:38	6	0	63	31	31
30	ch_ctr_interval	21:24	4	0	15	0	0
31	clock_divider	8:9	2	0	3	0	0
32	clock_output_en	31	1	0	1	1	1
33	count_global_SEU	27	1	0	1	0	0
34	count_missed_evt	25	1	0	1	0	0
35	count_trunc_evt	26	1	0	1	0	0
36	cs_as_veto	29	1	0	1	0	0
37	ext_pulse_en	3	1	0	1	1	1
38	fine_ctr_offset	13:20	8	0	255	0	0
39	fine_ctr_saturate	12	1	0	1	0	0
40	p_strip_config	32	1	0	1	0	0

Analog and digital configuration is combined. Positions 0-31 concern the digital and 32-171 concern the analog domain.

Channel Configuration

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Channel Configuration

	Item	Pos	Len	Min	Max	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
1	HCLDAC_e	28:32	5	0	31	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	HCLDAC_t	23:27	5	0	31	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	If	18:21	4	0	15	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8
4	Iref_ratio_e	37:40	4	0	15	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10
5	Iref_ratio_t	33:36	4	0	15	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10
6	channel_en	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
7	count_discarded_evt	13	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	count_local_SEU	16	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	count_missed_evt	14	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10	count_noise_evt	12	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11	count_refresh	15	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12	count_valid_evt	11	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
13	hit_validation	5	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
14	parallel_sync_FF	6	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
15	prediction_mode	4	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
16	stop_signal_delay	9:10	2	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17	sync_chain_length	7:8	2	0	3	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
18	test_mode_en	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19	trigger_mode	2:3	2	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20	unused	22	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21	use_delay_line	17	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	Item	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43
1	HCLDAC_e	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	HCLDAC_t	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	If	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8
4	Iref_ratio_e	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10
5	Iref_ratio_t	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10
6	channel_en	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
7	count_discarded_evt	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	count_local_SEU	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	count_missed_evt	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10	count_noise_evt	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11	count_refresh	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12	count_valid_evt	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
13	hit_validation	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
14	parallel_sync_FF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
15	prediction_mode	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
16	stop_signal_delay	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17	sync_chain_length	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
18	test_mode_en	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19	trigger_mode	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20	unused	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21	use_delay_line	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Ctrl+A: Adopt selected value for all channels

Selected item: ch set read

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Send and Readback the Configuration

So far we edited the configuration values but we did not actually send any information to the chip.
To write the configuration to PASTA simply press the related button.

Problem with Channel Configuration

The configuration is successfull for channel addresses from 0 to 31, but seems to fail for the other half of the channels.

Channel Configuration

	Item	Pos	Len	Min	Max	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41
1	HCLDAC_e	28:32	5	0	31	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	HCLDAC_t	23:27	5	0	31	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	If	18:21	4	0	15	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8
4	Iref_ratio_e	37:40	4	0	15	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10
5	Iref_ratio_t	33:36	4	0	15	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10
6	channel_en	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
7	count_discarded_evt	13	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	count_local_SEU	16	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	count_missed_evt	14	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10	count_noise_evt	12	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11	count_refresh	15	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12	count_valid_evt	11	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
13	hit_validation	5	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
14	parallel_sync_FF	6	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
15	prediction_mode	4	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
16	stop_signal_delay	9:10	2	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17	sync_chain_length	7:8	2	0	3	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
18	test_mode_en	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19	trigger_mode	2:3	2	0	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20	unused	22	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21	use_delay_line	17	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	Item	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
1	HCLDAC_e	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	HCLDAC_t	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	If	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8
4	Iref_ratio_e	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10
5	Iref_ratio_t	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10
6	channel_en	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
7	count_discarded_evt	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	count_local_SEU	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	count_missed_evt	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10	count_noise_evt	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11	count_refresh	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12	count_valid_evt	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
13	hit_validation	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
14	parallel_sync_FF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
15	prediction_mode	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
16	stop_signal_delay	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17	sync_chain_length	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
18	test_mode_en	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19	trigger_mode	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20	unused	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21	use_delay_line	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Possible explanation

The channel address is 7 bits long, although you would only need 6 for 64 channels, as PASTA has.
At the moment the LSB is always 0 (in theory PASTA should ignore it).
What happens if PASTA does not ignore it, but ignores instead the MSB?

sent		interpreted	
ch.1	000001 0	ch.2	0 000010
ch.2	000010 0	ch.4	0 000100
ch.3	000011 0	ch.6	0 000110
ch.31	011111 0	ch.62	0 111110
ch.32	100000 0	ch.0	1 000000

It would mean that we are able to configure only the channels with address even and < 31.

Configuration of the Internal Test Pulse

PASTA can generate a test pulse internally.
Two possibilities:

- Test pulse used directly instead of the discriminator output (digital signal).
- Test pulse fed throught the analog calibration circuit (analog signal).

Configure Digital Test Pulse

	Item	Pos	Len	Min	Max	Set Value
1	NPulses	0:9	10	0	1023	0
2	Pulse Lenght	10:17	8	0	255	0
3	Pulse Spacing	18:25	8	0	255	0

Configure Analog Test Pulse

	Item	Pos	Len	Min	Max	Set Value
1	Channel address	8:13	6	0	63	0
2	Enable cal circuit	0	1	0	1	0
3	Probing signals from ch to pad	7	1	0	1	0
4	Pulse amplitude	1:6	6	0	63	0

Config TP Digital

Config TP Analog

External Test Pulse

PASTA can receive an external test pulse via the SMA connectors.

- Waveform generator
- Logic analyzer

$\longrightarrow$ the chip responds to stimuli

To understand how it responds, we need to read out the data.

Summary of Chip Configuration I

Global Configuration

Command	Address	Data Length		CRC-8	Description
		N_{wr}	N_{rd}		
1000	-	172	1	Required	Write global configuration
1001	-	-	172	Required	Read global configuration
1010	-	26	26	Required	Configure internal test pulse
1011	-	-	10	Required	Read global counter
1100	-	14	1	Required	Write global test congfiguration
1101	-	-	1	Required	Read global test congfiguration

Table 5: Commands for the global configuration

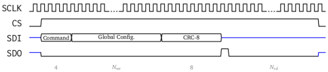

Figure 4: Example of a write command without the Address data

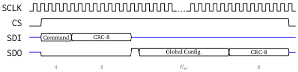

Figure 5: Example of a read command without the Address data

Configuration and readback are succesful.

Summary of Chip Configuration II

Channel Configuration

Command	Address	Data Length		CRC-8	Description
		N_{wr}	N_{rd}		
0000	Required	41	41	Required	Write channel configuration
0001	Required	-	41	Required	Read channel configuration
0010	Required	1	1	Required	Write channel test configuration
0011	Required	1	1	Required	Read channel test configuration
0100	Required	-	10	Required	Read channel counter

Table 4: Commands for the channel configuration

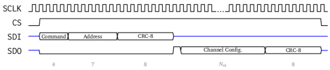

Figure 2: Example of a reading command with all fields

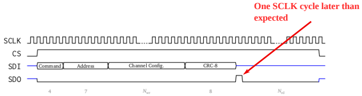

Figure 3: Example of a writing command with all fields

Configuration and readback fail for channel address > 31.

Other remarks

- Problem: SDO has inverted polarity.
- Workaround: invert it logically in the firmware.

Outlook

JÜLICH
FORSCHUNGSZENTRUM

- Implement the generation of a test pulse in the firmware.
- Read the data out from the chip and analyze it.
- Fix the problem related to the channel configuration.