PANDA-EMC ADC – IDENTIFYING REQUIREMENTS

Amplitude resolution:

1MeV..8GeV → 14-bit ADC or double 10-bit dual range

Time resolution:

20 ns signal rise-time → 160 MHz with 3 samples on leading edge
200 ns integrated signal rise-time → 25 MHz with 5 samples on leading edge

Processing power

Flexibility/Re-programmability
Raw data buffer 5-10us for each channel
Feature extraction
Control/ remote configuration capability

Inside the PANDA detector

Power dissipation issue

→ Maximum dissipation not fully established
→ Effort required to minimize power consumption
→ Lower sampling frequency
→ Minimizing processing power redundance

Radiation damage issue

→ careful simulation needed
→ radiation resistancy tests of prototypes can be done in The Svedberg Lab, Uppsala

PANDA-EMC INTERNAL ADC – IDENTIFYING KEY COMPONENTS

Board Size:

Max 65 X 110 mm → small components, limited quantity

ADC:

LTC-2261, 14-bit, 125 MSPS, 127 mW
→ 2 W per board,
→ currently best performance/power consumption factor

Processing power

	XC5V70FX70T	XC3S4000
Advantages	High performance Internal Hi-speed serializer PowerPC based embedded system	Sufficient performance Moderate power consumption MicroBlaze based embedded system
Disadvantages	High power consumption	Needs external data serializer → Additional component

Optical Interface

SFP type → can be decided later
SFF type → smaller size

ANALOG-TO-DIGITAL CONVERTER

LINEAR TECHNOLOGY

LTC2261-14
LTC2260-14/LTC2259-14

14-Bit, 125/105/80Msps
Ultralow Power 1.8V ADCs

FEATURES

- 73.4dB SNR
- 85dB SFDR
- Low Power: 127mW/106mW/89mW
- Single 1.8V Supply
- CMOS, DDR CMOS or DDR LVDS Outputs
- Selectable Input Ranges: $1V_{P-P}$ to $2V_{P-P}$
- 800MHz Full-Power Bandwidth S/H
- Optional Data Output Randomizer
- Optional Clock Duty Cycle Stabilizer
- Shutdown and Nap Modes
- Serial SPI Port for Configuration
- Pin Compatible 14-Bit and 12-Bit Versions
- 40-Pin (6mm × 6mm) QFN Package

APPLICATIONS

DESCRIPTION

The LTC®2261-14/LTC2260-14/LTC2259-14 are sampling 14-bit A/D converters designed for digitizing high frequency, wide dynamic range signals. They are perfect for demanding communications applications with AC performance that includes 73.4dB SNR and 85dB spurious free dynamic range (SFDR). Ultralow jitter of $0.17ps_{RMS}$ allows undersampling of IF frequencies with excellent noise performance.

DC specs include ±1LSB INL (typical), ±0.3LSB DNL (typical) and no missing codes over temperature. The transition noise is a low $1.2LSB_{RMS}$.

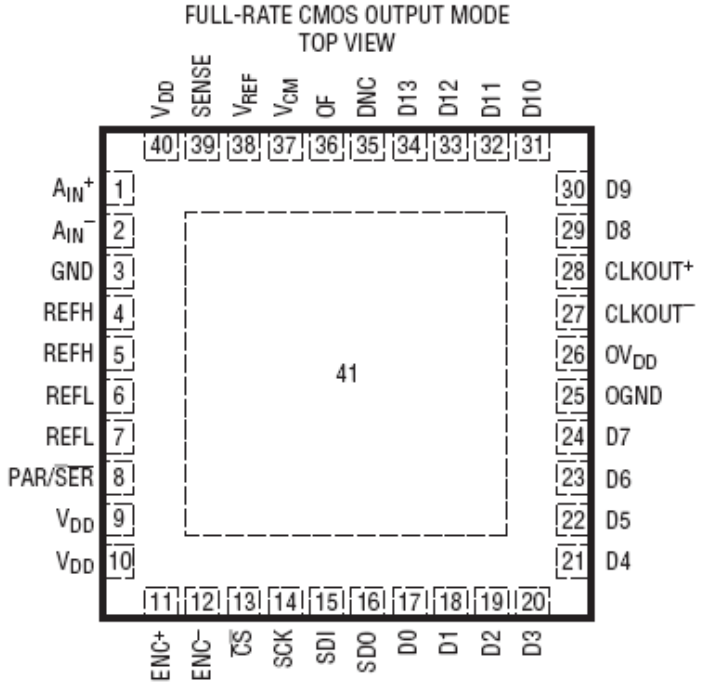
The digital outputs can be either full rate CMOS, double data rate CMOS, or double data rate LVDS. A separate output power supply allows the CMOS output swing to range from 1.2V to 1.8V.

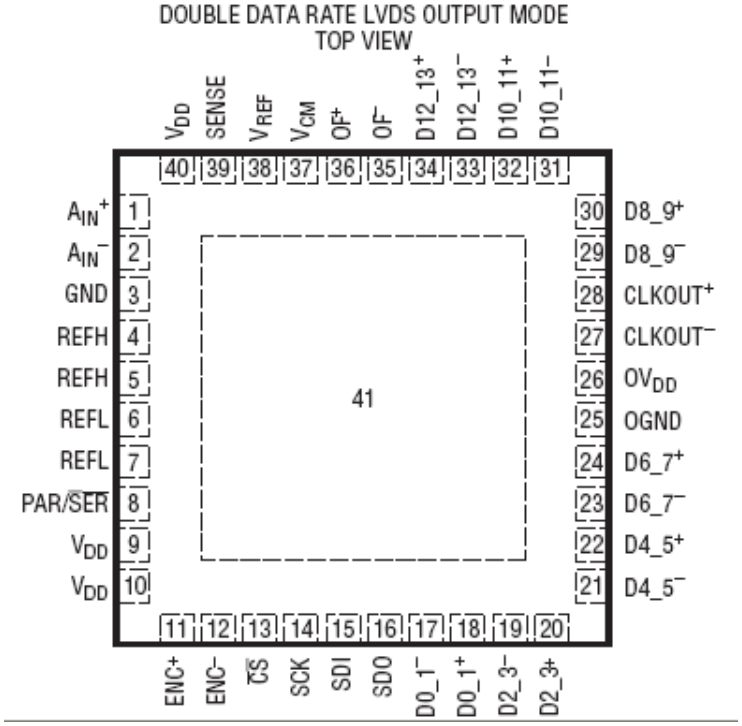
ANALOG-TO-DIGITAL CONVERTER

LINEAR TECHNOLOGY

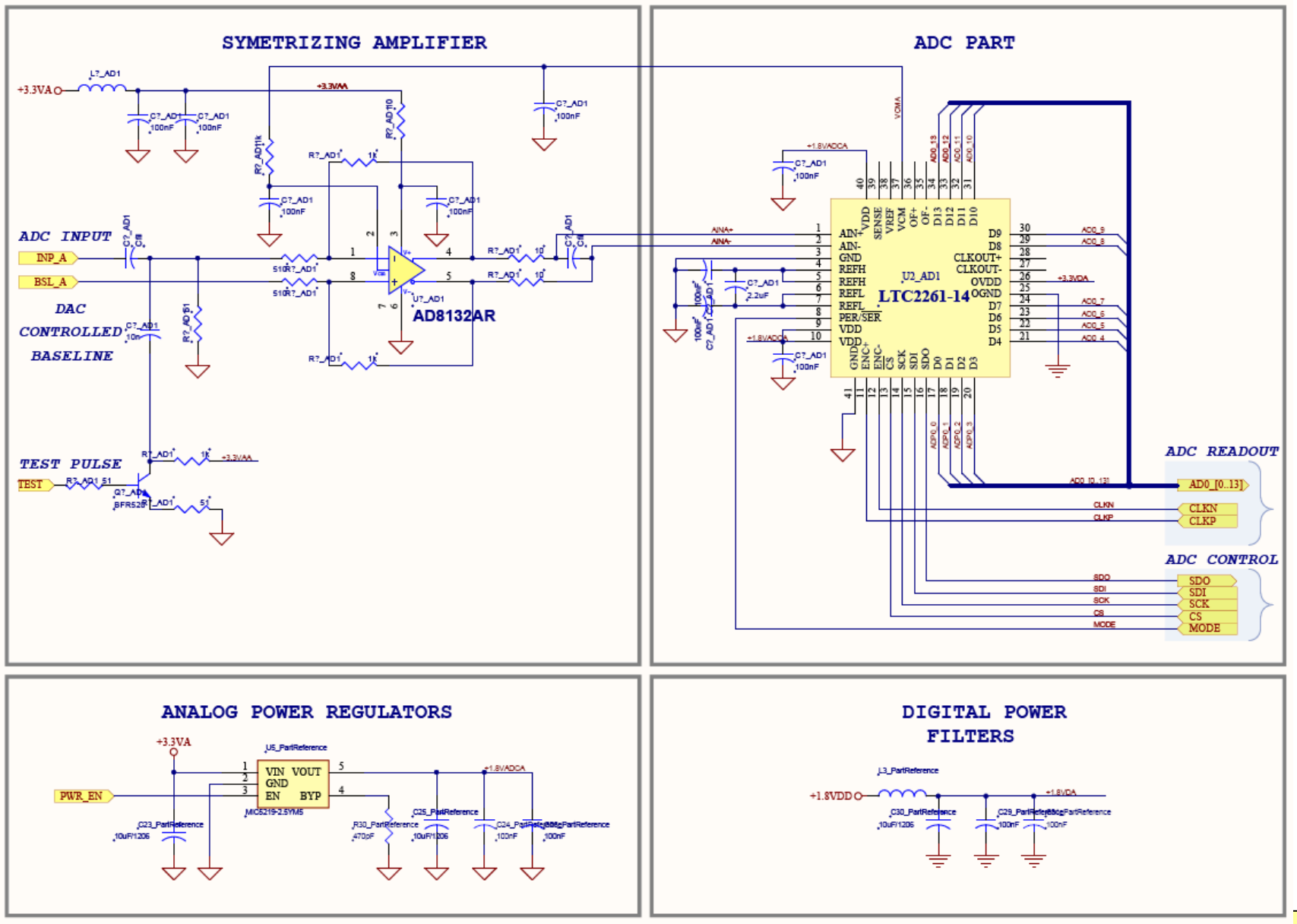
LTC2261-14
LTC2260-14/LTC2259-14
14-Bit, 125/105/80Msps

Different output possibilities

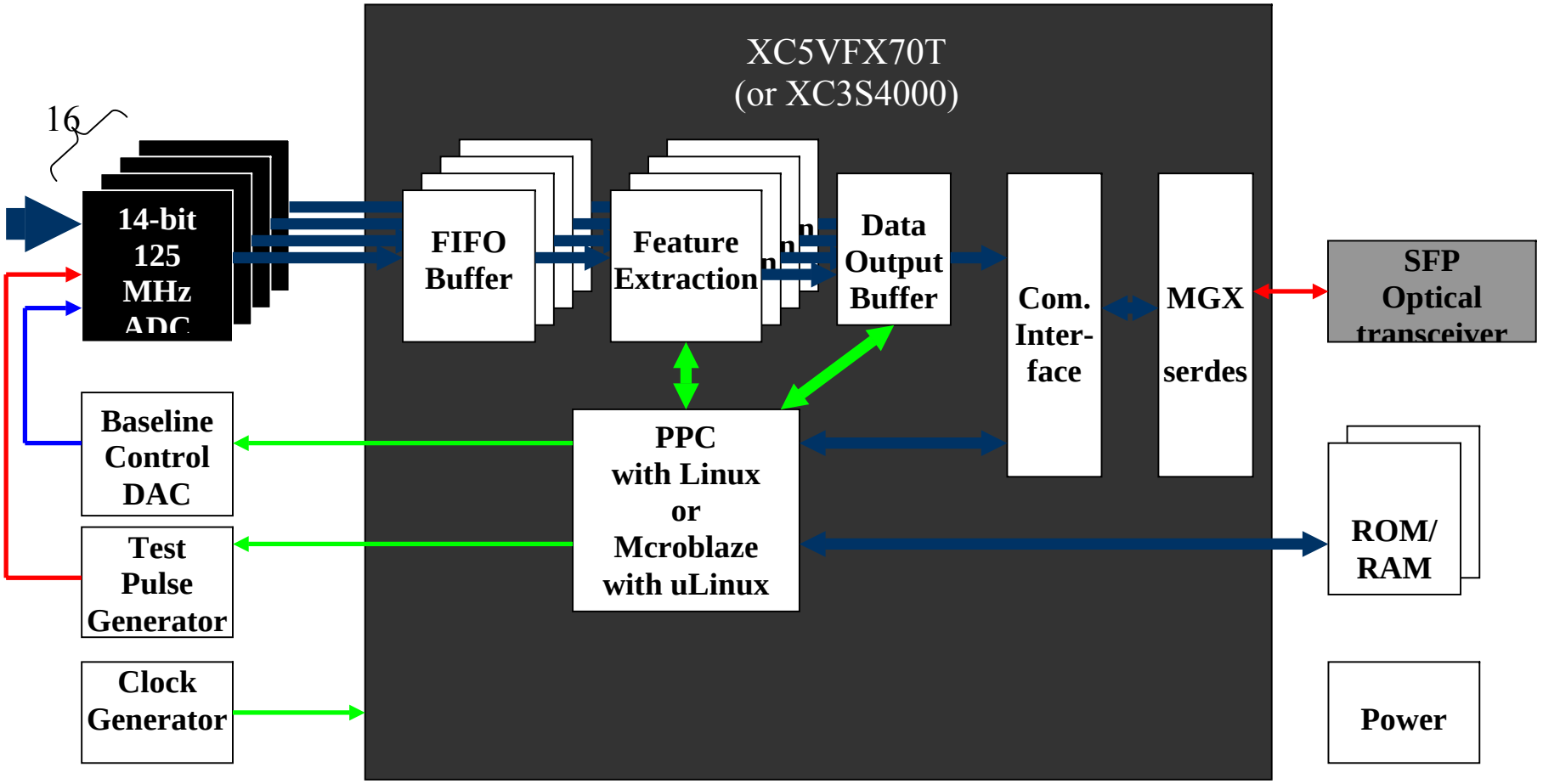




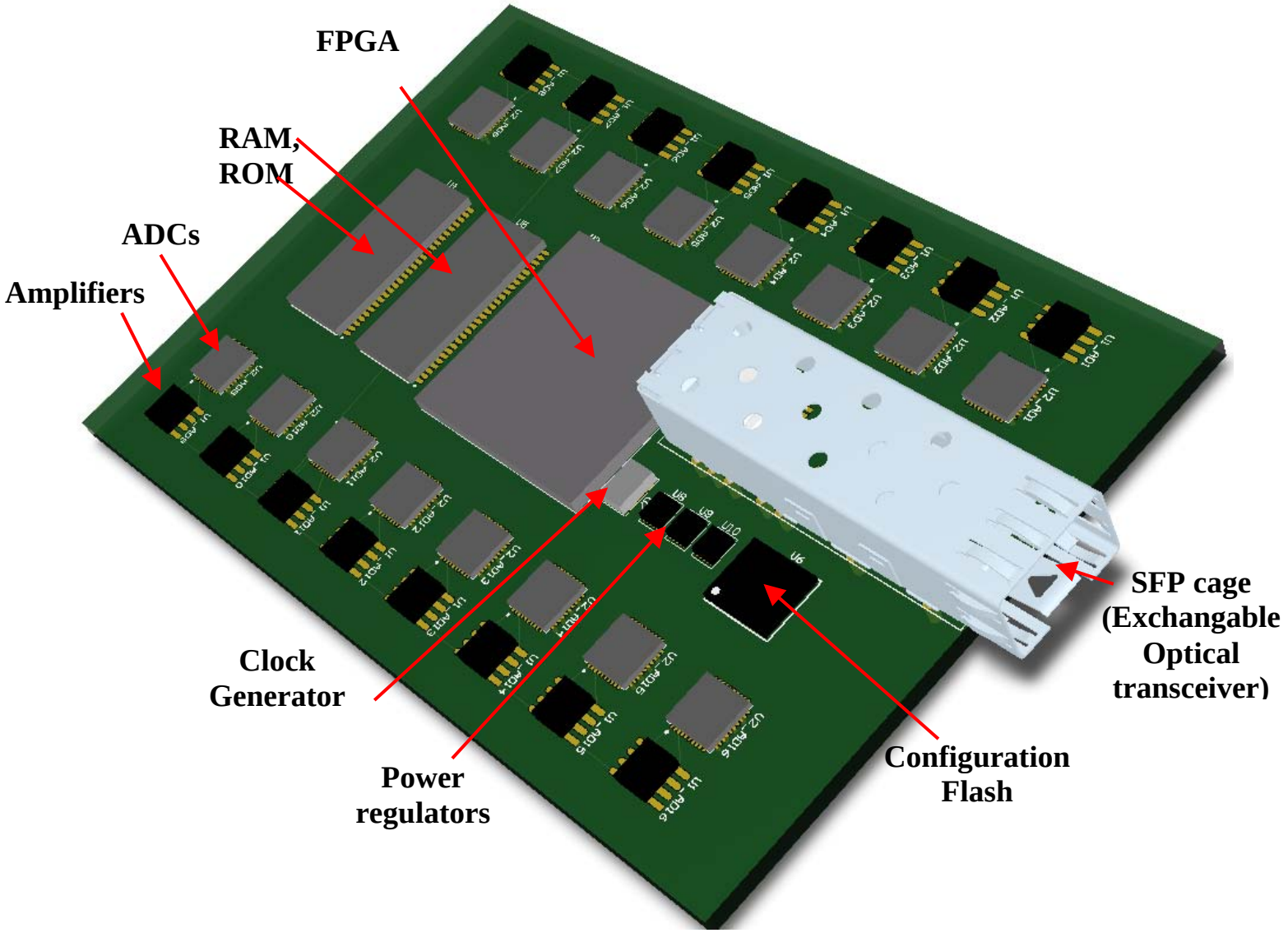
SCHEMATIC OF ONE CHANNEL



A 16-CHANNEL BOARD- HARDWARE STRUCTURE



A 16-Channel ADC Board – Preliminary Layout



A POSSIBLE ADC READOUT SYSTEM

VME-64x/VXS Carrier
(Stripped AWM-16 ADC design)

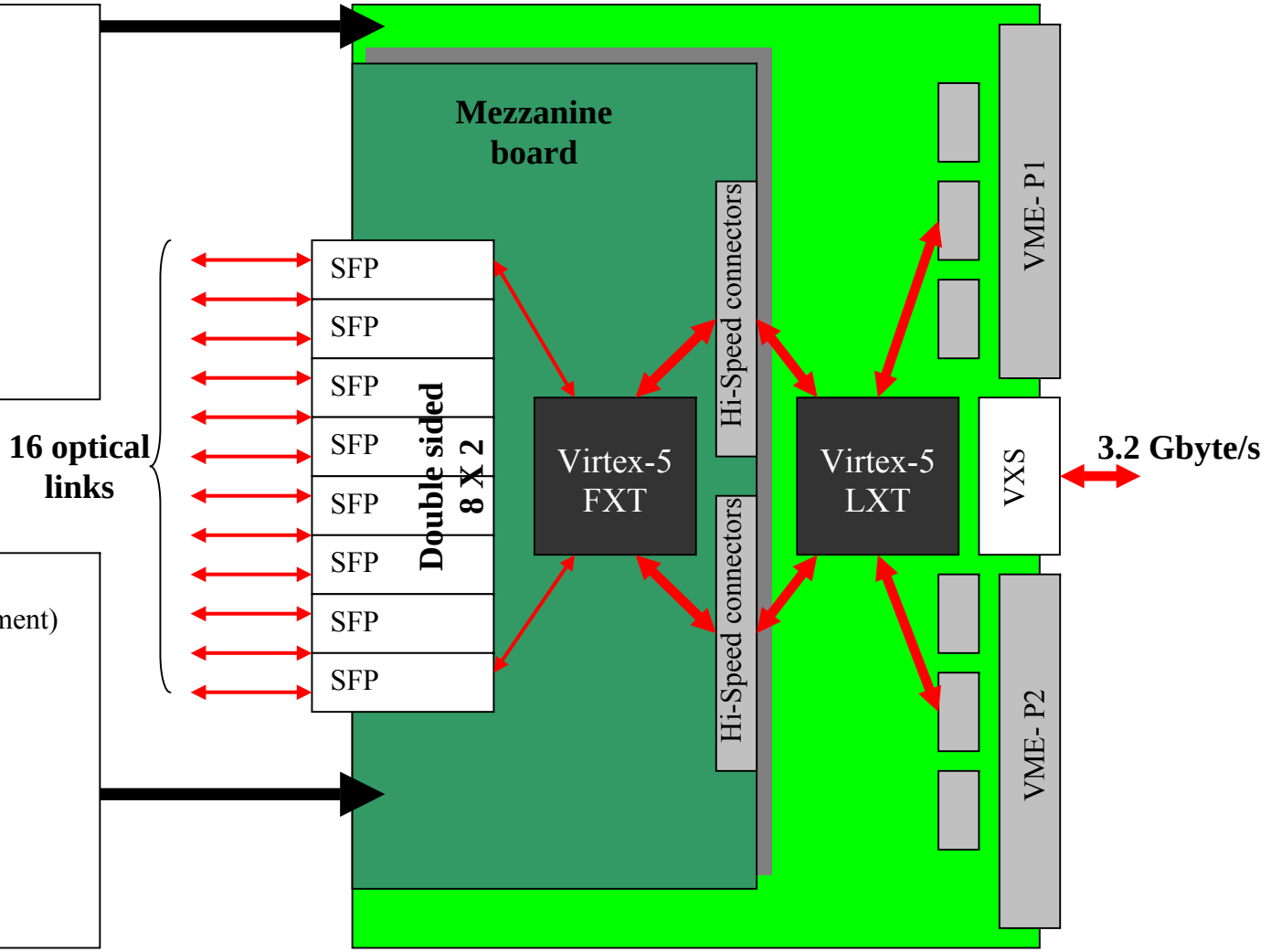
- 72 High-Speed interconnections
- Configuration Utility
- Power regulators
- 8 VXS full duplex 3.2 Gb links
- MBLT-64 VME readout mode

Ready April 2009

Optical Interface Mezzanine
(Data Collector/Trigger Unit for WASA experiment)

- 16 optical interfaces 3.2 Gb
- Data processing in Virtex-5 FXT

Ready June 2009



WORK SCHEDULE