EMC Electronics Developments at KVI

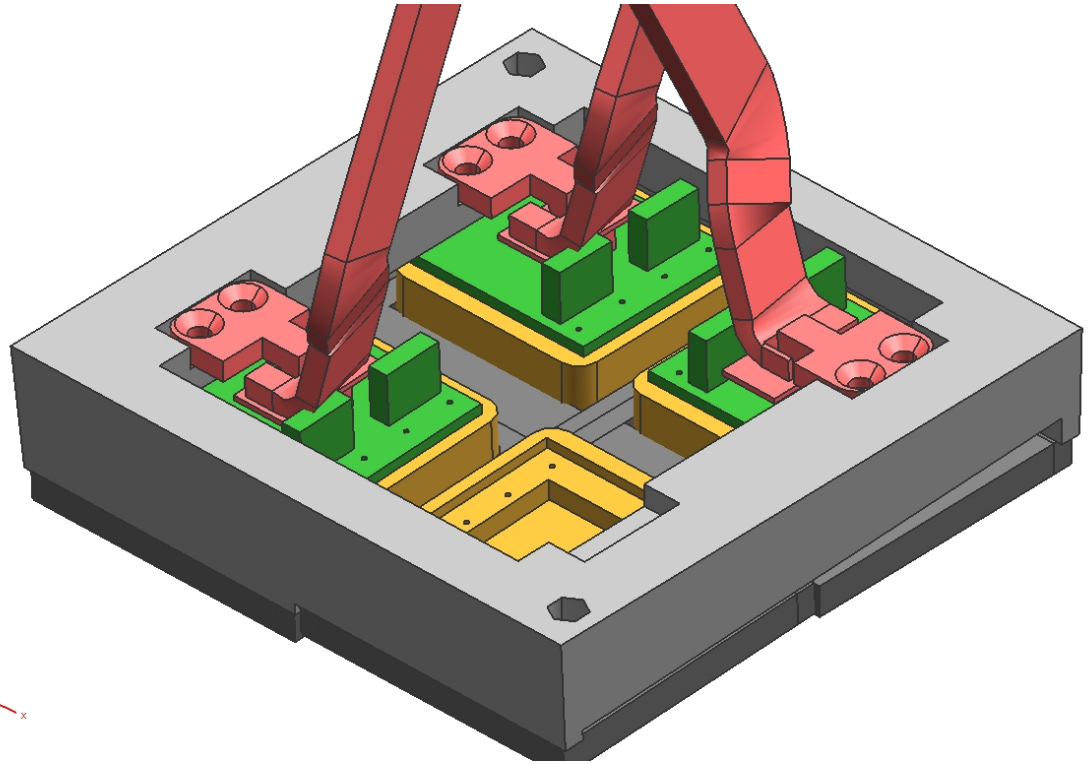
M. Kavatsyuk, E. Guliyev, P.J.J. Lemmens,
H. Löhner, T.P. Poelman, G. Tambave

Outline

- ASIC board design
- Flexible flat cable for the EMC endcap
- SADC requirements

ASIC BOARD

Insert mounted with ASIC boards (old design)



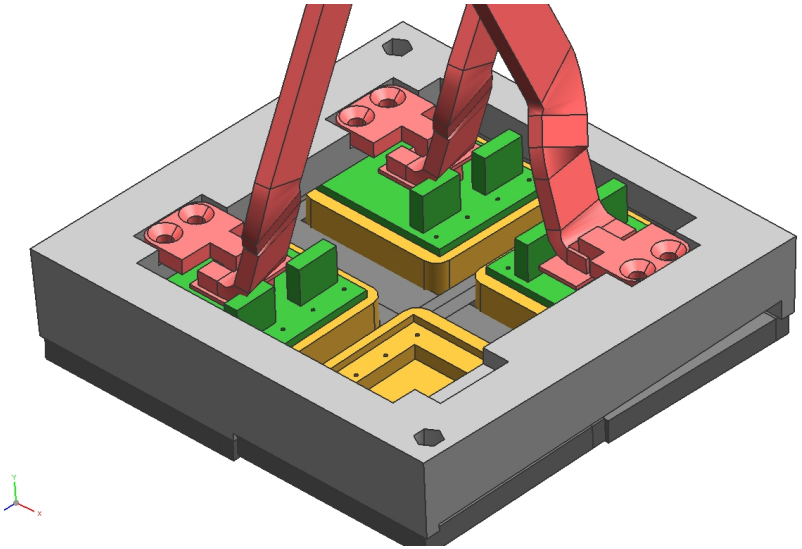
Questions to be answered:

(as for December 2008):

- possibility to fit ASIC with required components on the 18x19 mm^2 PCB
- dimensions and type of decoupling capacitors
- connection between ASIC board and collector board

ASIC BOARD
decoupling capacitors

- measurements with C={300n, 200n, 100n, 56n, 22n, 7n, 1.3n}
- data taken with 100MHz 16bit SADC
- traces analysed to deduce:
  - noise level → constant for all values of C
  - the peak integral → constant (deviation < 0.5%) for C ∈ {300n, 200n, 100n, 56n, 22n};
    for C=7n signal drop **2%**
    for C=1.3n signal drop **10%**



Conclusions: use C=56n

- type: SMD, X7R dielectric, V_{max}=630V
- dimensions: 4.5x3.2 mm², height 2.54mm

This choice allows to:

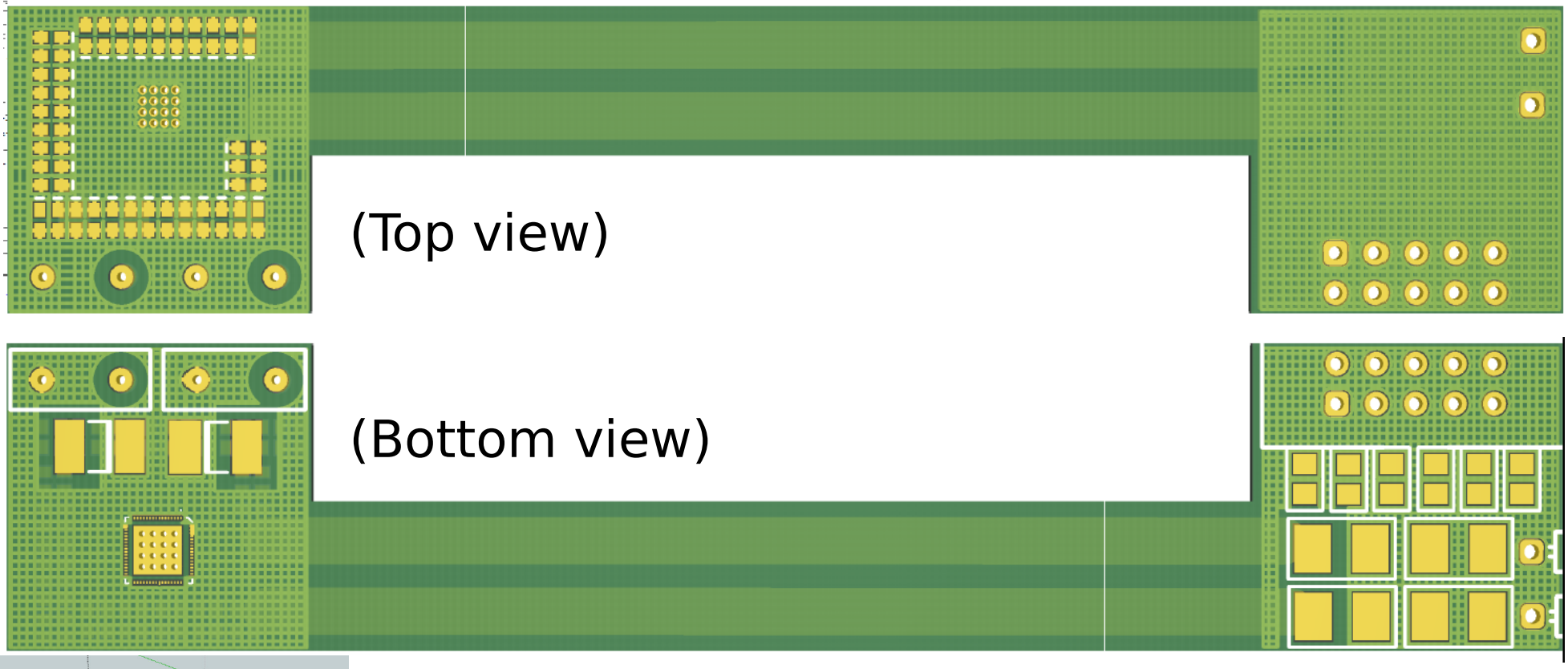
- place capacitors on the same PCB side as ASIC (bottom side)
- rotate LAAPD capsule
- make output on the opposite side to the LAAPD pins

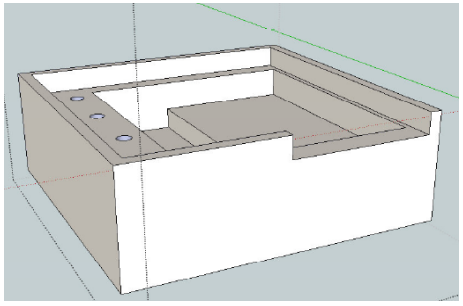
ASIC BOARD

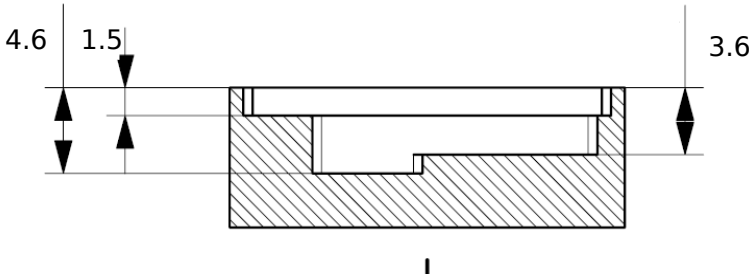
ASIC
rigid PCB
(8 layers)

Flexible flat cable
(~10cm long; 6 layers)

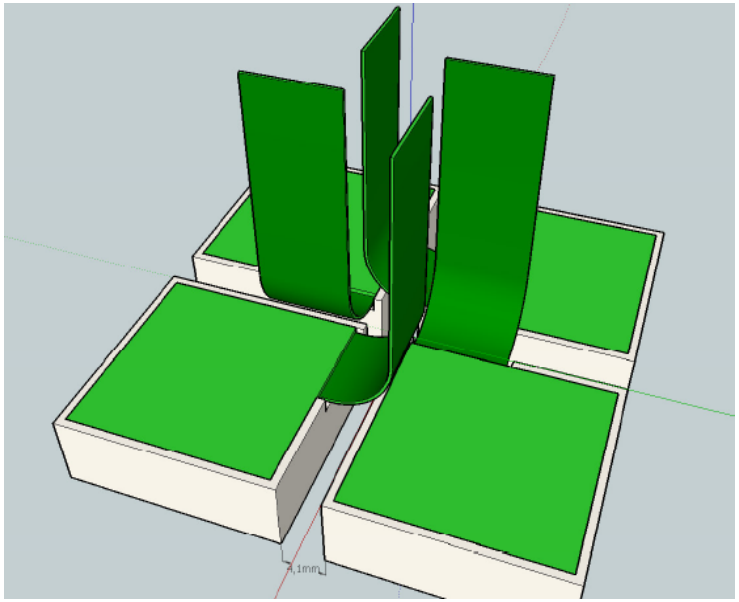
Connector board
rigid PCB (8 layers)
(HV filter)



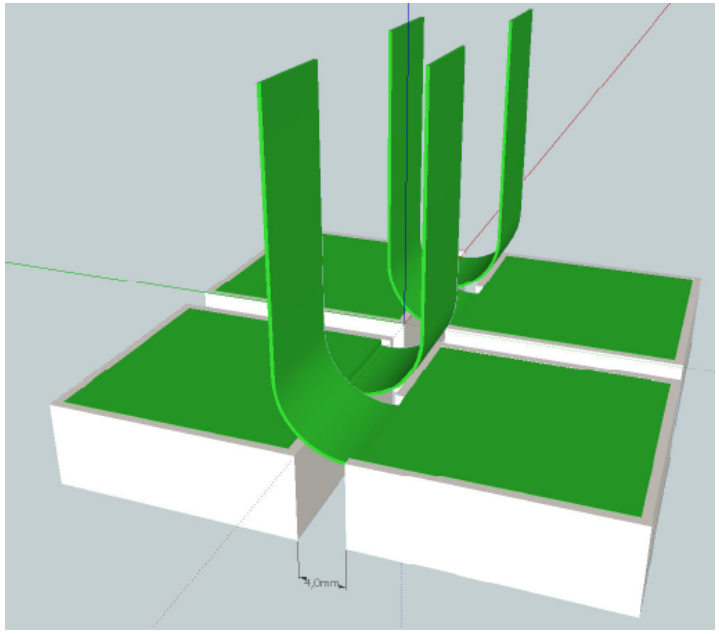




ASIC BOARD
possible arrangements



Option A
- Requires smaller feed-through for the cables in the supporting plate



Option B
- Requires larger feed-through for the cables in the supporting plate
- Larger bending radius of flexible cables

ASIC board
Conclusions

- The decoupling capacitors are selected (56n, 630V)
- Decoupling capacitors are placed on the same side as ASIC
- The design of ASIC board is almost finished
- The performance can be tested only with prototypes (~end of summer)
- The arrangement of the output cables (options A, B) should be selected according to the mechanical design preferences

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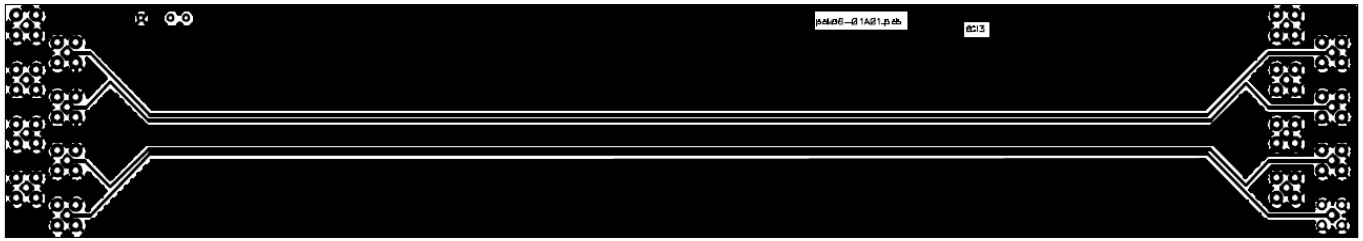
- SADC requirements

Endcap flat cable

- Investigations are done with prototype rigid PCB
- Achievable cross-talk ~ 1:62000 (30 cm long cable)
- Next weeks the complete measurements with prototype will be done



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Realistic estimation for the copper budget
(16 channels signals and HV)

Outline

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SADC requirements
achievable time resolution

Measurements with LNP preamplifier (100MHz 16bit SADC):

- LED light pulser (E_{dep}~180MeV): 0.5ns
- Ion beam (^{6}Li 2AGeV, E_{dep}~180MeV): 1.2ns
- High-energy γ-rays (E_{dep}~100MeV): 1.4ns

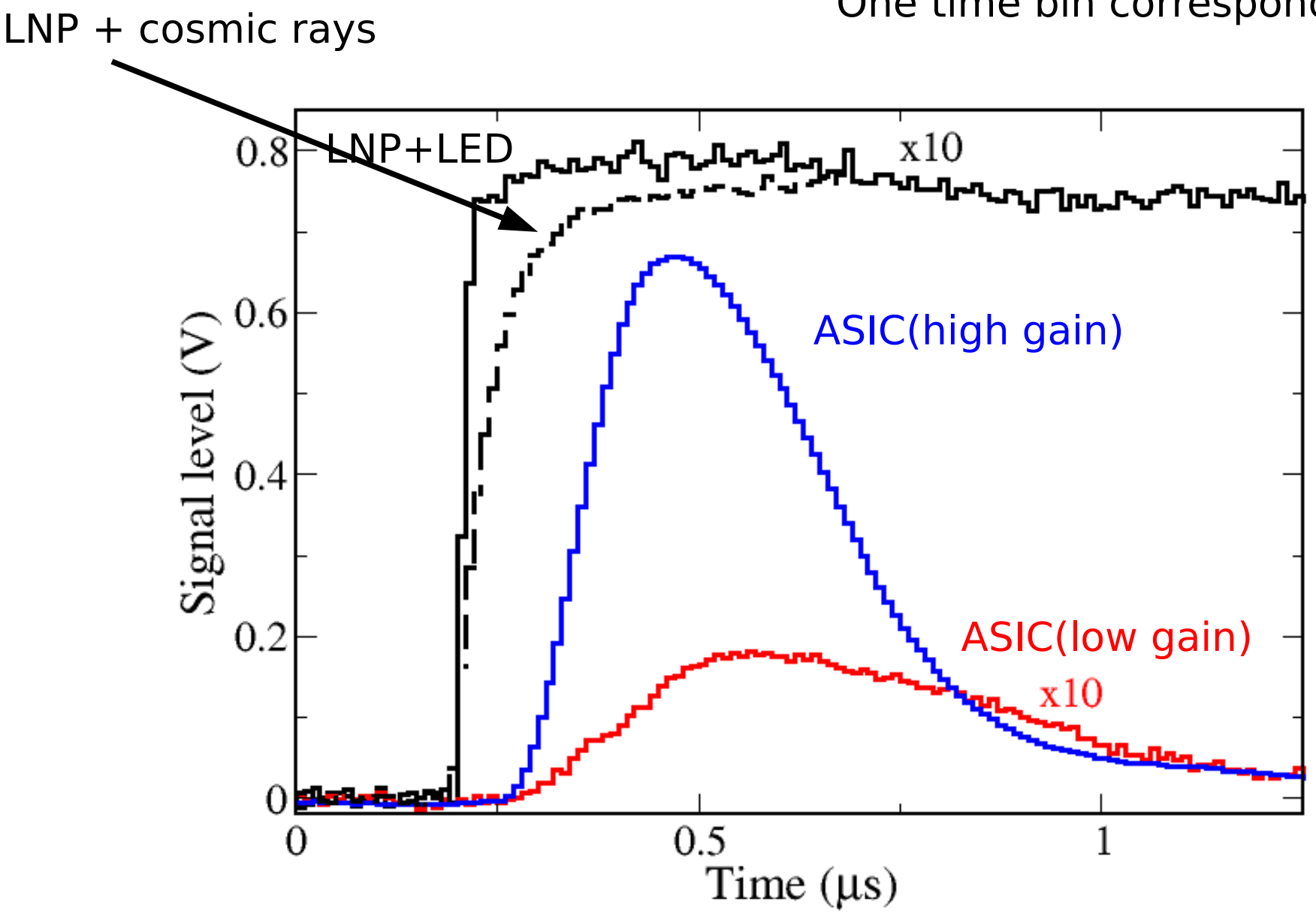
Same results are achieved with sampling rates of 50MHz and 25 MHz

but

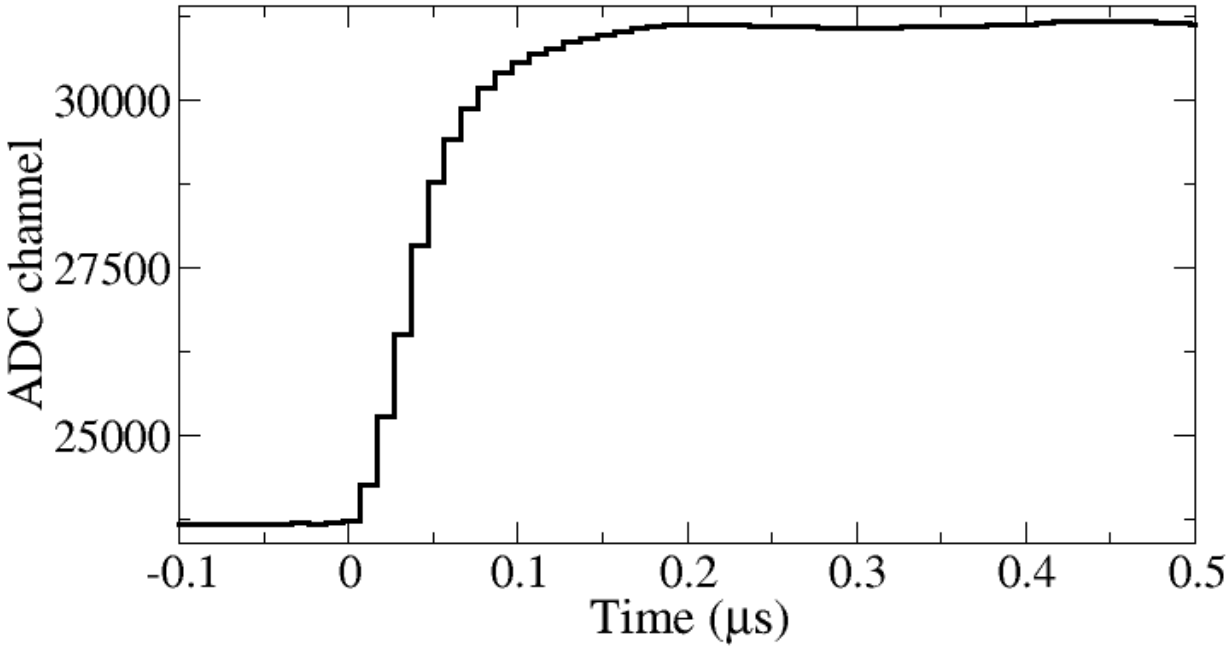
results at 25MHz are too sensitive to chosen parameters

SADC requirements
pulse shapes

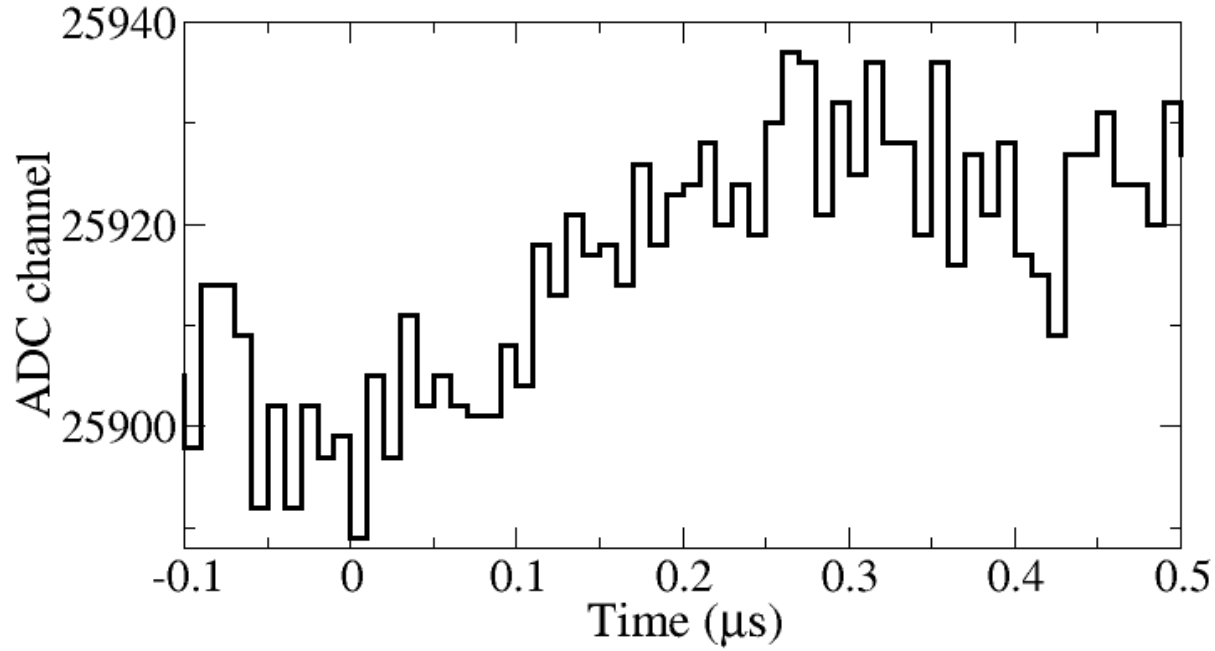
One time bin corresponds to 10ns



SADC requirements
pulse shapes



E_{dep}~1 GeV (gamma)



E_{dep}~4 MeV (cosmic ray)

One time bin corresponds to 10ns

SADC requirements
conclusions

- Time resolution is limited by the rise time of the signal (1.2ns for E_{dep}~180MeV)
- Sampling rate of **50 MHz** is sufficient to obtain optimal time and energy resolution
- Two 12bit or one 14bit SADC per LAAPD should be used. At present 12bit SADC are preferable.
  Typical effective ASDC resolution:
  - 12 bit → 11.5 effective bits
  - 14 bit → 12.5 effective bits

EMC Digitizer

To test “real” performance of SADC readout one has to build realistic prototype.

VHDL implementation of the developed feature-extraction algorithms should be tested with measurements