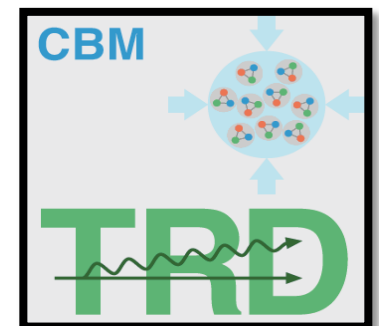


Design and Test of the Real Size Prototypes for the CBM-TRD in Frankfurt

Milad Tanha

DPG, Darmstadt

16.03.2016

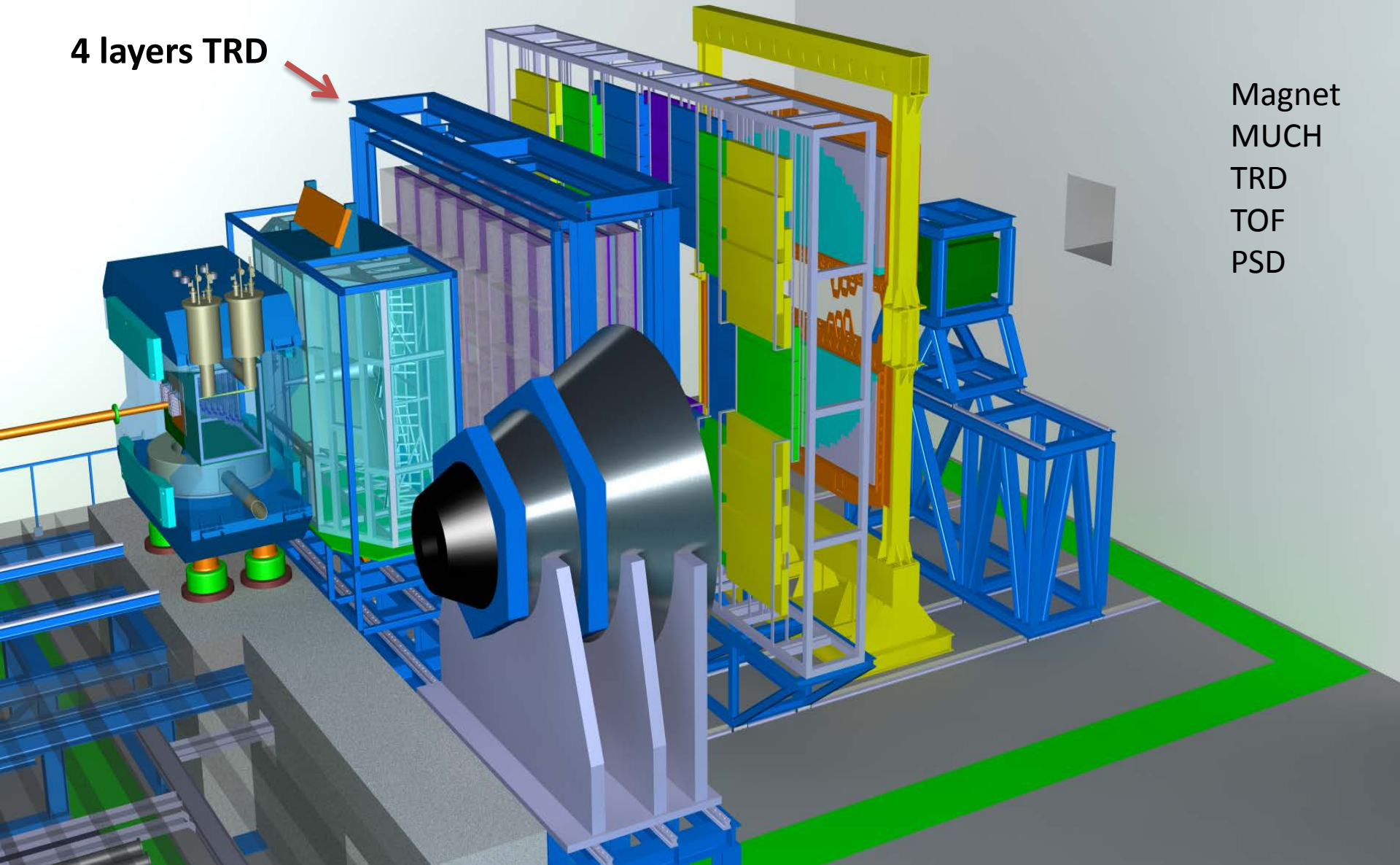


Overview:

- CBM-TRD setup for SIS 100
- Prototype design
- Readout chain
- Preliminary Results from CERN PS , SPS and laboratory test
- Outlook and summary

CBM Experiment Setup for SIS 100

4 layers TRD



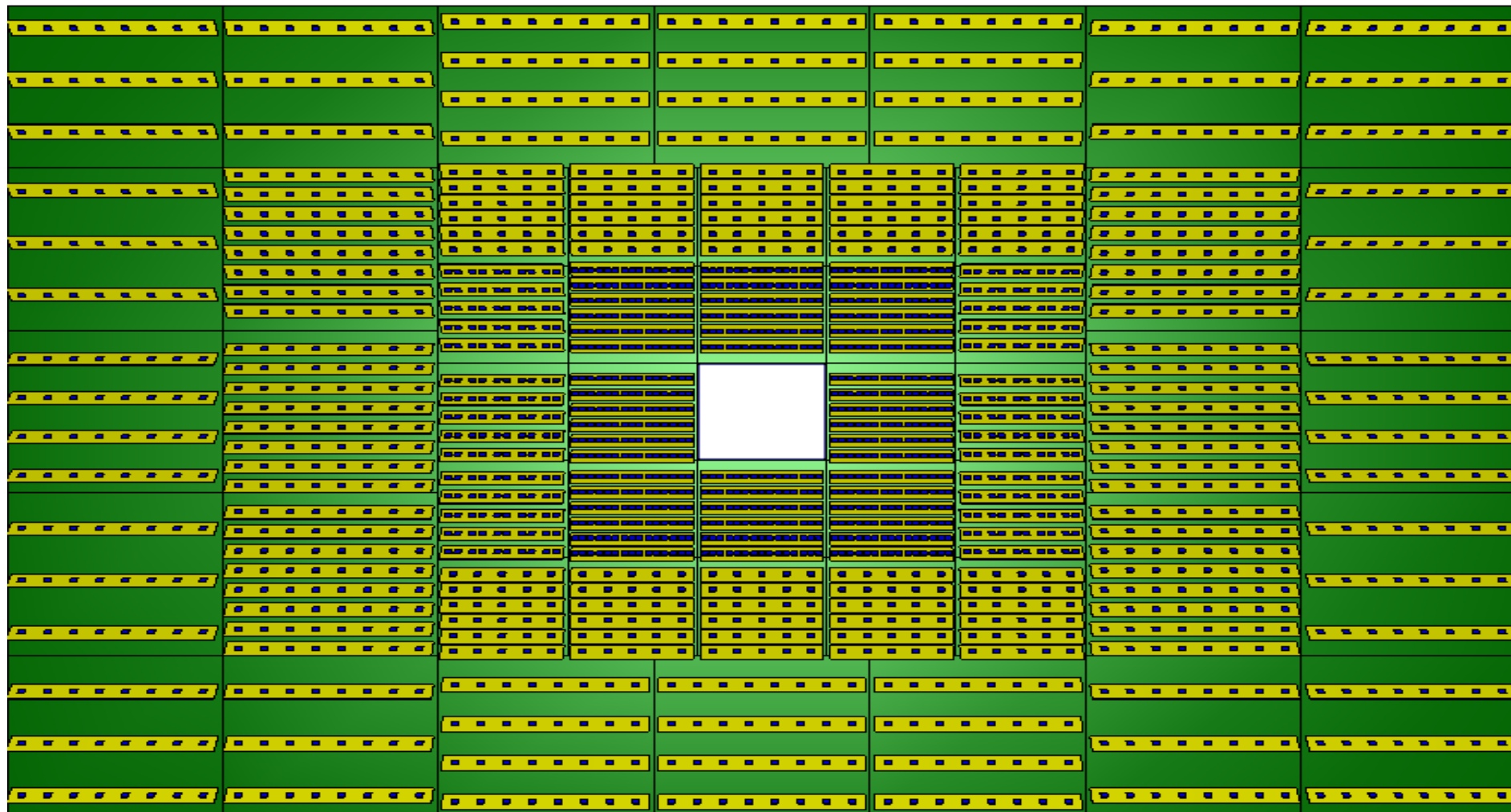
Magnet
MUCH
TRD
TOF
PSD

Back View of The First layer of TRD in SIS-100

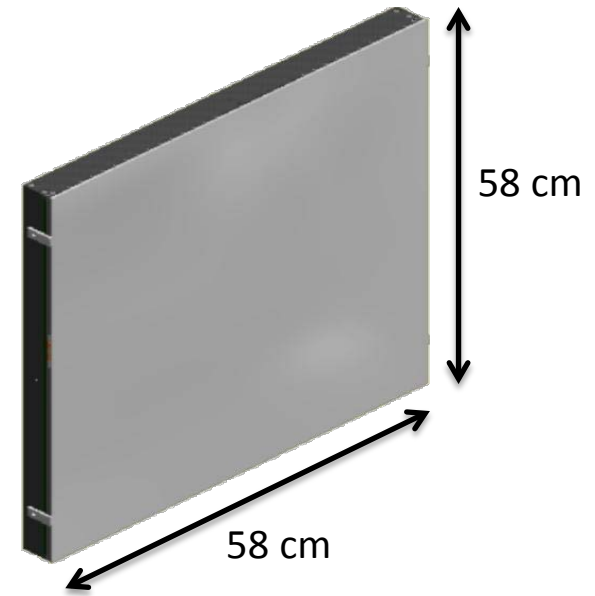
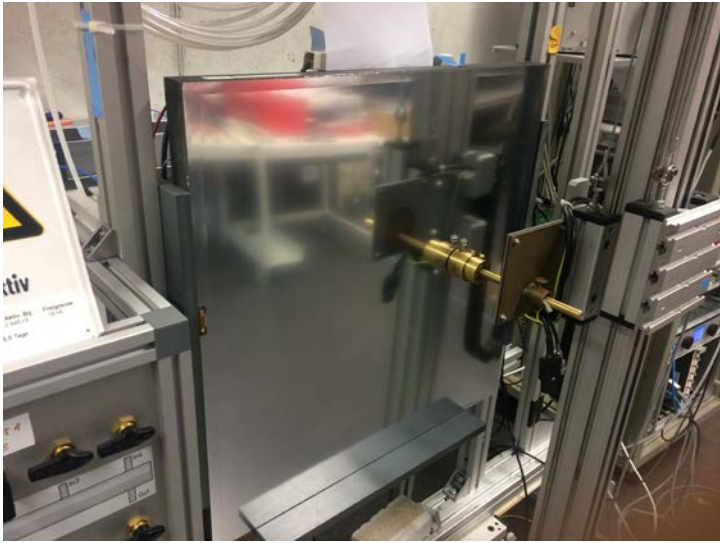
57x57 cm² for inner parts

95x95 cm² for outer parts

- Different FEBs are shown in yellow
- Regular, super, ultimate FEBs, 5x32, 10x32 and 15x32 channel ASICs respectively



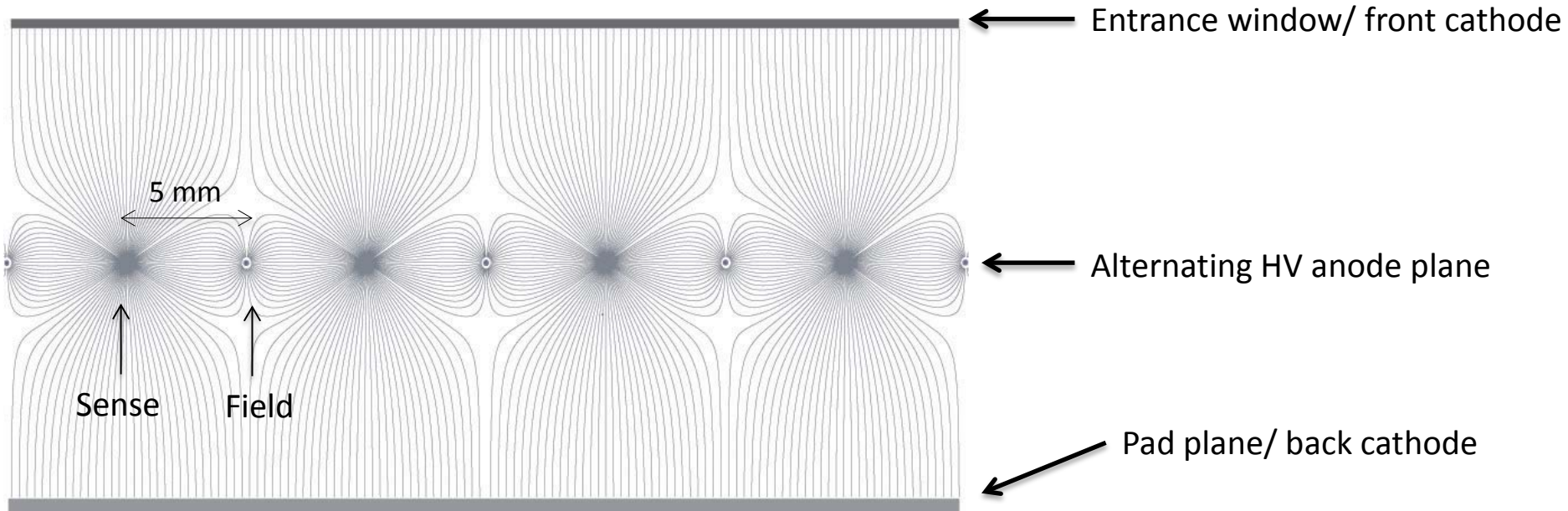
Frankfurt Prototype with Carbon Frame and Without Drift Region



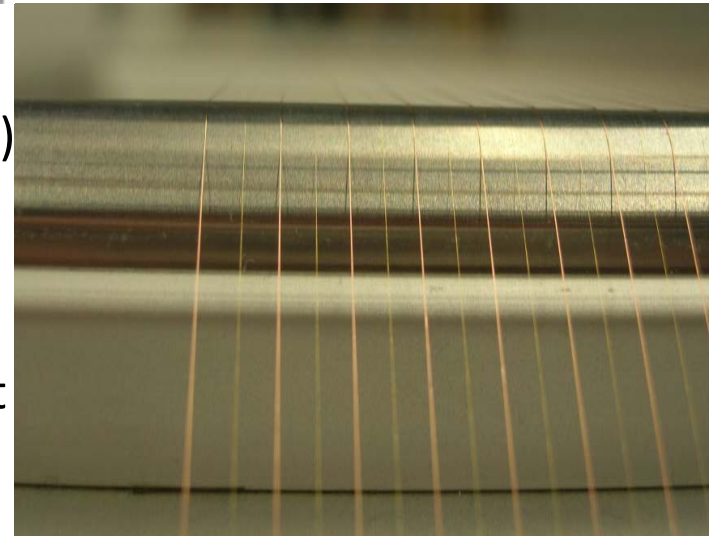
- Thin and fast MWPC, (thickness of amplification region = 3.5+3.5 mm)
- High mechanical rigidity (carbon for frame and back panel)
- Alternating HV anode without drift region
- Used at CERN-PS test in 2014 and at laboratory in Frankfurt in 2016

Electric Field of Alternating HV Without Drift Region

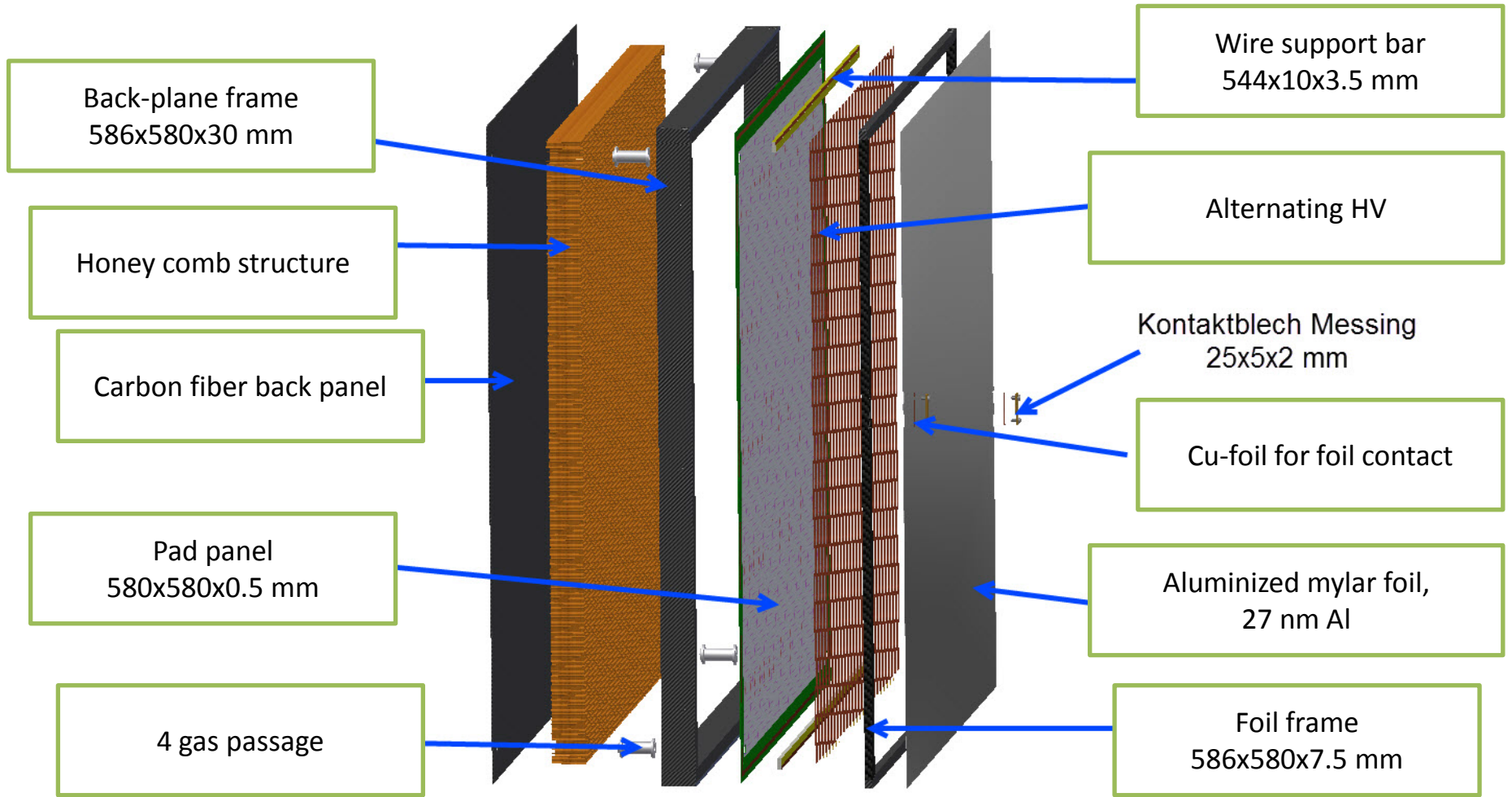
(NIMA698, 11 (2013))



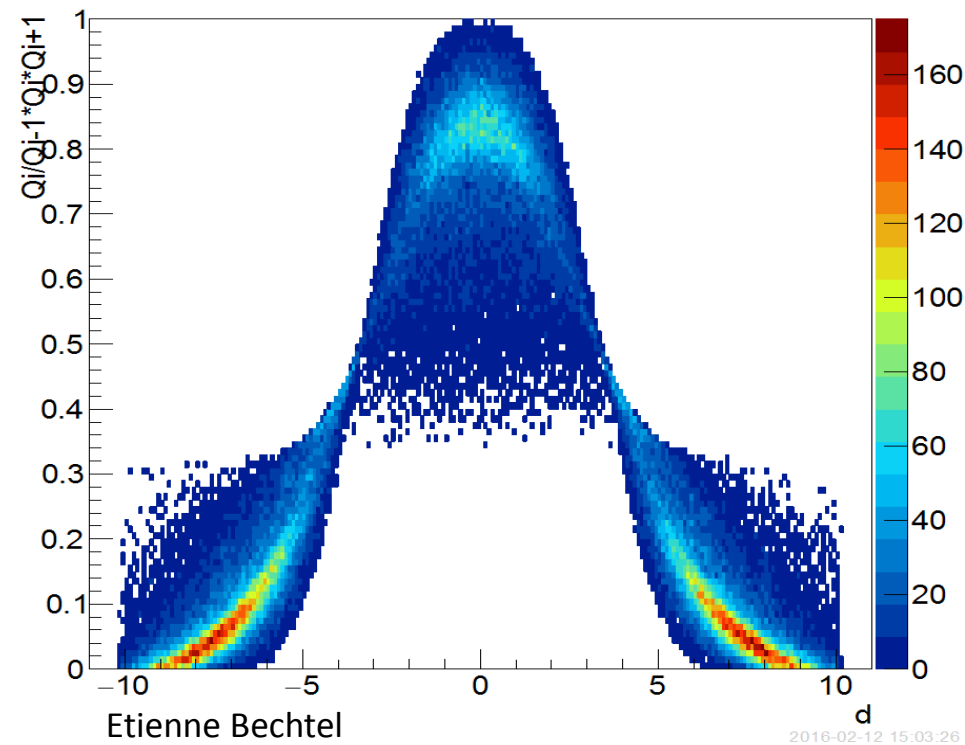
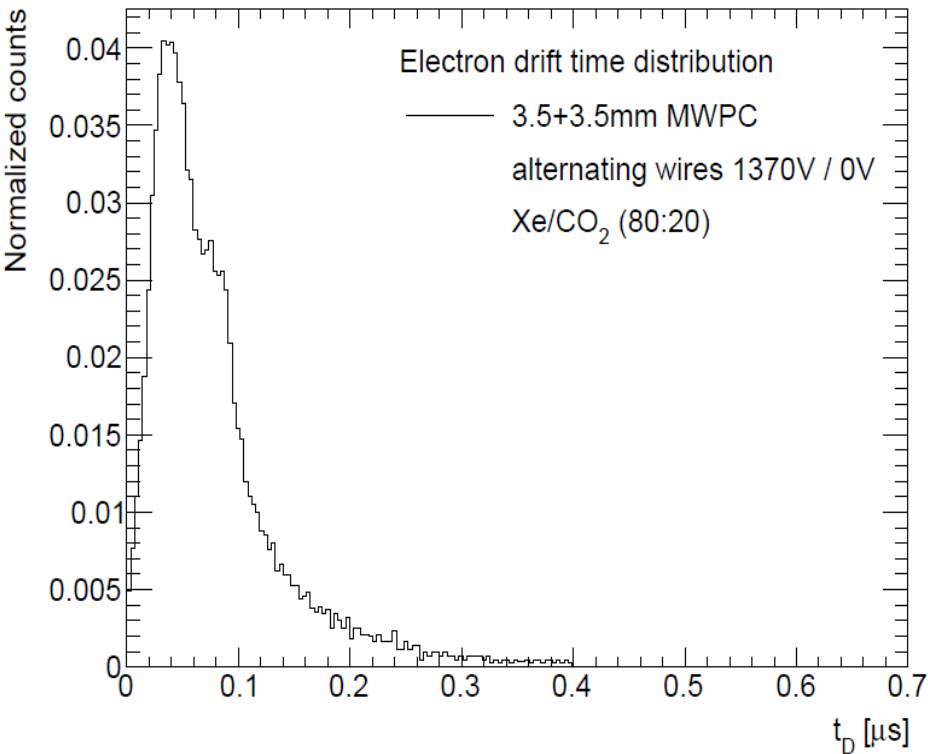
- Alternating HV anode (CuBe = 80um, AuW = 20 um)
- Reduces sensitivity to pressure variation
- Gain stability is an important issue for MWPCs w/o drift region
- less charge accumulation-->high rate environment



Structure of a TRD



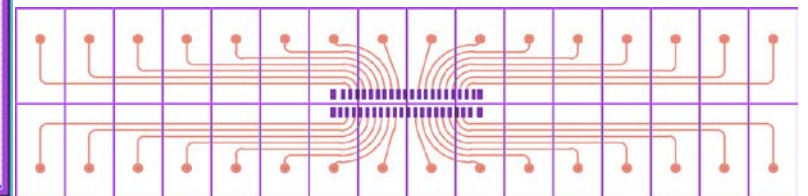
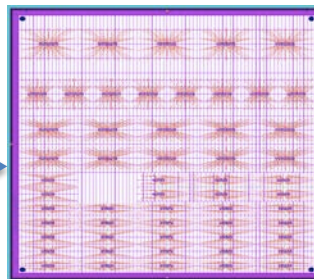
Results from CERN-PS Beam Test 2014



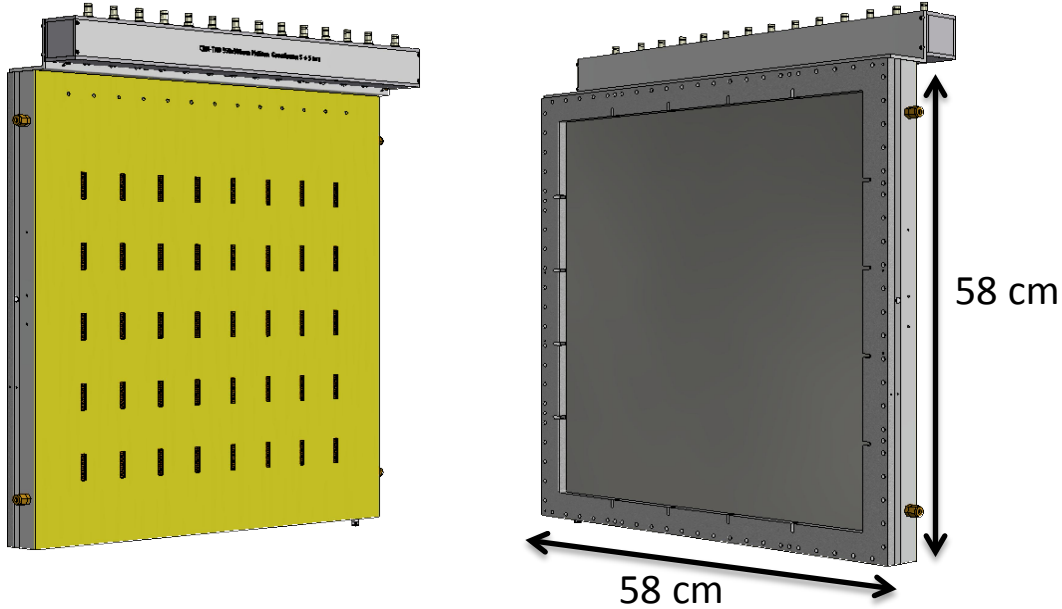
Electron Drift Time of MWPC with Garfield Simulation

Pad Response Function: distribution of a generated cluster and its spread over the read out pads

Pad-plane design

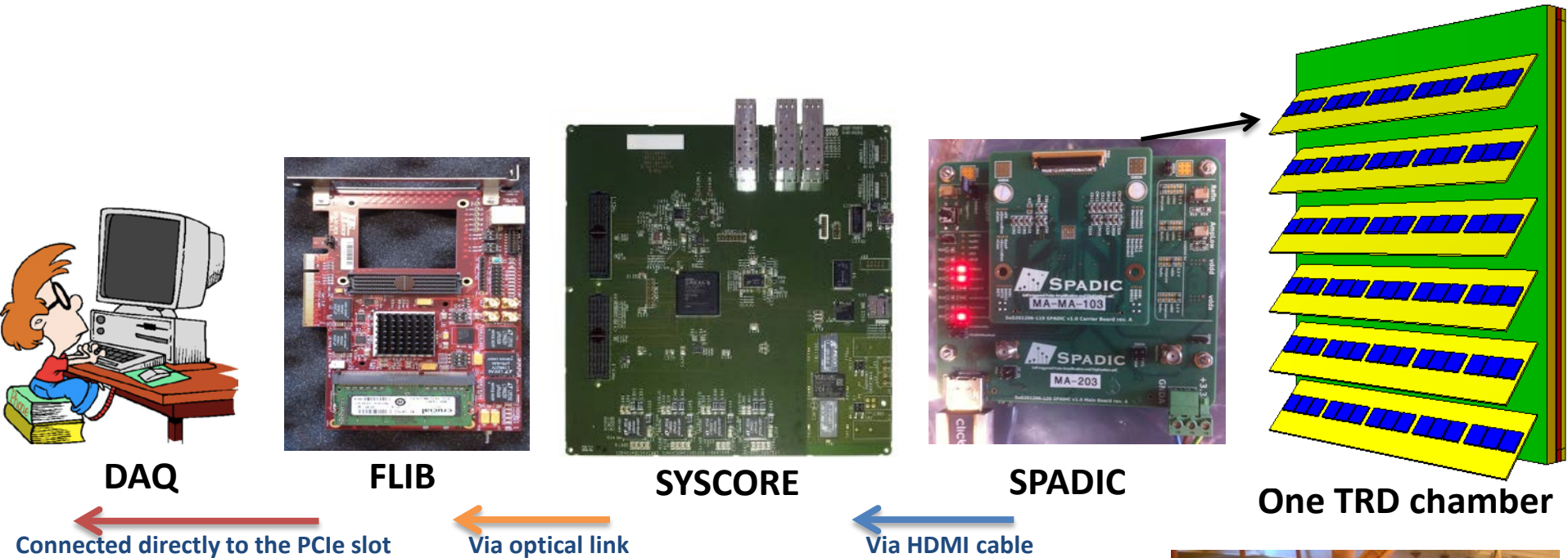


Prototype For High Rate Test at CERN-SPS



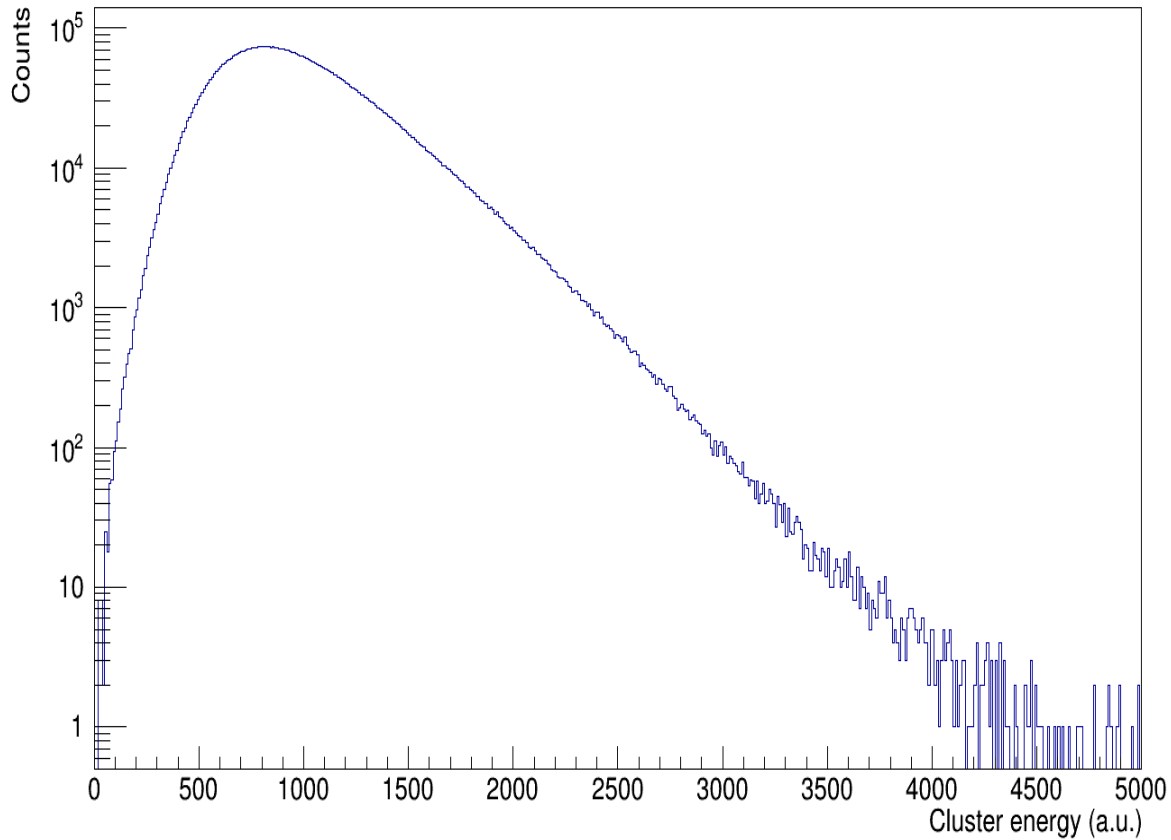
- SPS produces heavy ion beam
- The same wire geometry (alternating HV) as it's used in prototype with carbon frame
- Segmented HV supply (13 HV cable) for anode wires to sustain high load at CERN-SPS
- Thickness of amplification region (4+4 mm)
- Filter for every channel

Read-Out Chain Structure



- SPADIC: a Self-triggered Pulse Amplification and Digitization ASIC to process electrical detector signal
- The SysCore v3: is a Read-Out Controller (ROC) that is used as an interface between Front-End Boards (FEBs) and the DAQ system (FLIB)
- This read-out chain is used in CERN-PS, SPS and laboratory

Preliminary Results from CERN-SPS 2015

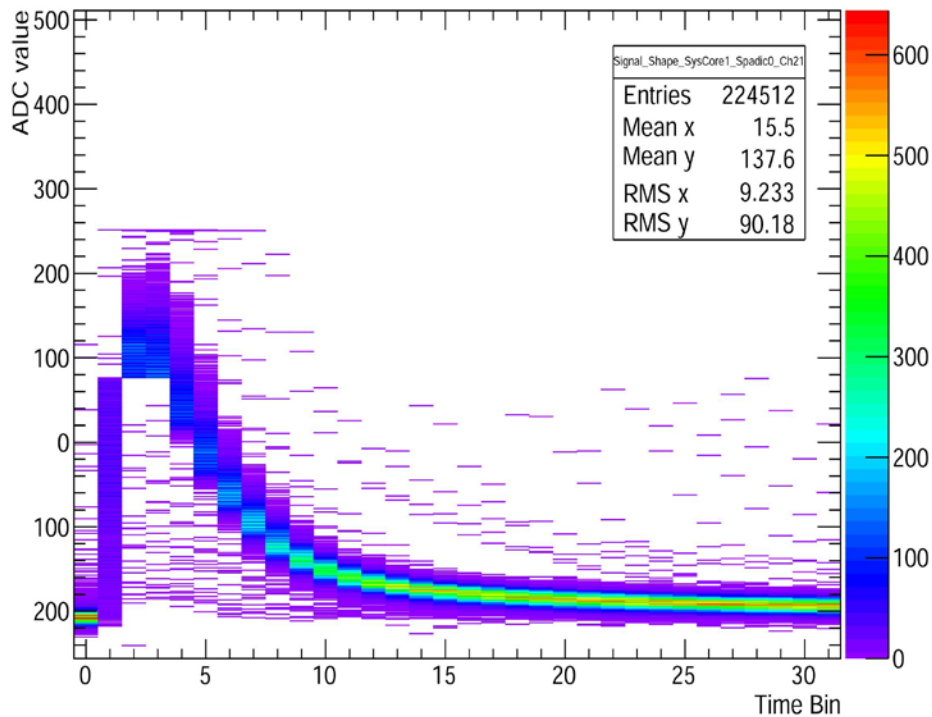


Spectrum of cluster charged
Wide length is due to the energies of heavy ions
F. Roether



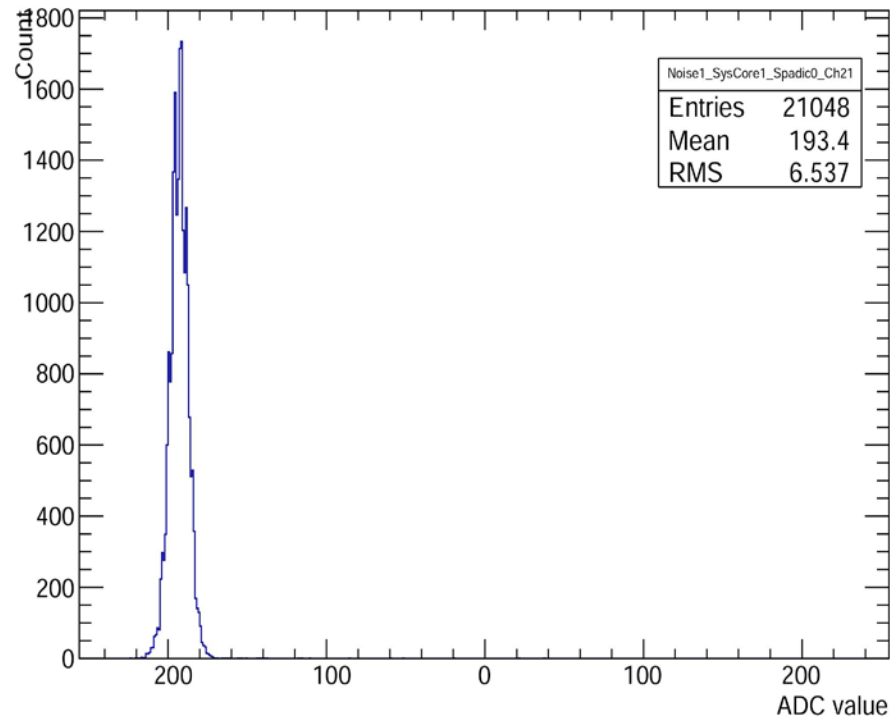
Laboratory Measurement with Fe-55

Signal_Shape_SysCore1_Spadic0_Ch21



Fe-55 raw signal , test with HV=1420 V

Noise1_SysCore1_Spadic0_Ch21



Noise of the same channel with the same configuration

Outlook

- Construction of new large prototype (95x95 cm²)
- Proceeding data analyzing from CERN-SPS 2015
- Laboratory measurement Fe-55 spectra
- Test of new electronics (SPADIC) in laboratory and
- DESY electron beam test
- CERN-SPS beam test

Summary

- Electronics/readout tested and bugs were reported to designers
- Both prototypes showed promising results
- Prototype for high-rate test were stable in high load environment during CERN-SPS beam test

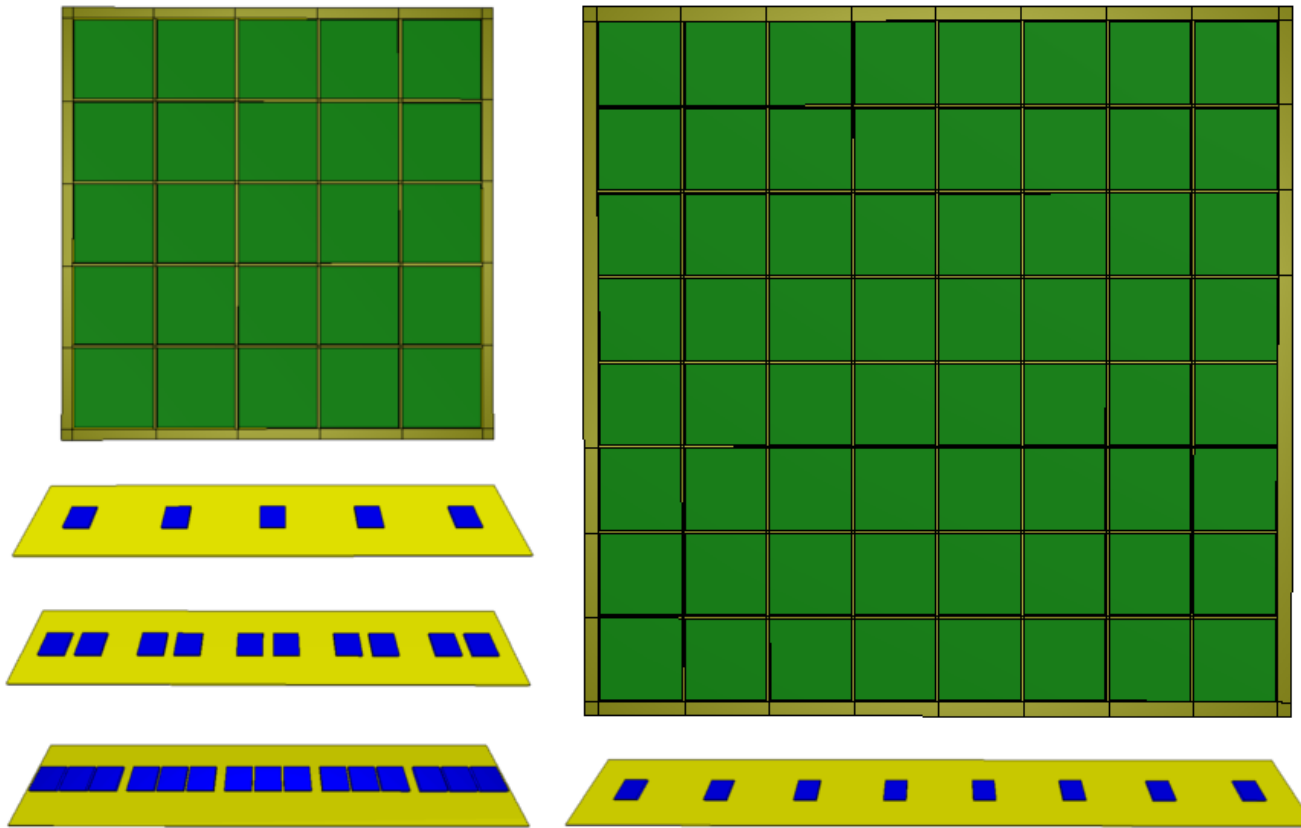
Flying TRDs



Foto by F. Roether, CERN-SPS, Nov.2015

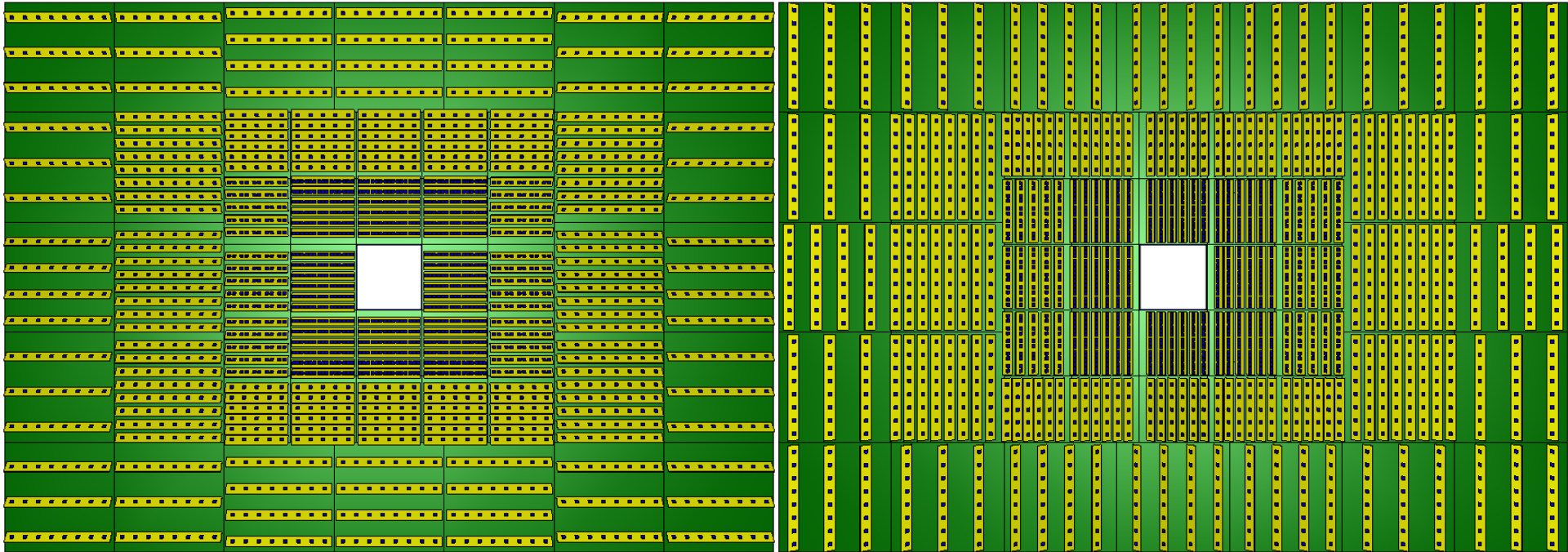
**Thank You
for Your Attention**

Back up



TRD modules and related FEB types: regular, super, and ultimate density. With 5x32, 10x32 and 15x32-channel ASICs (notation: FEB_15u, FEB_10s, FEB_05n) for the small modules and 8 x 32-channel ASICs (notation: FEB_08n) for the large module types.

Rear-side view of two different TRD layers, illustrating the orientation of FEBs on the modules.



Pad-plane Sample 2014

