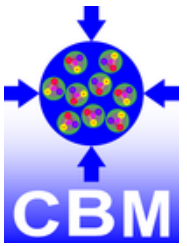
DPG Spring meeting
Darmstadt, 14-18 March 2016

The Silicon Tracking System (STS) Frontend electronics

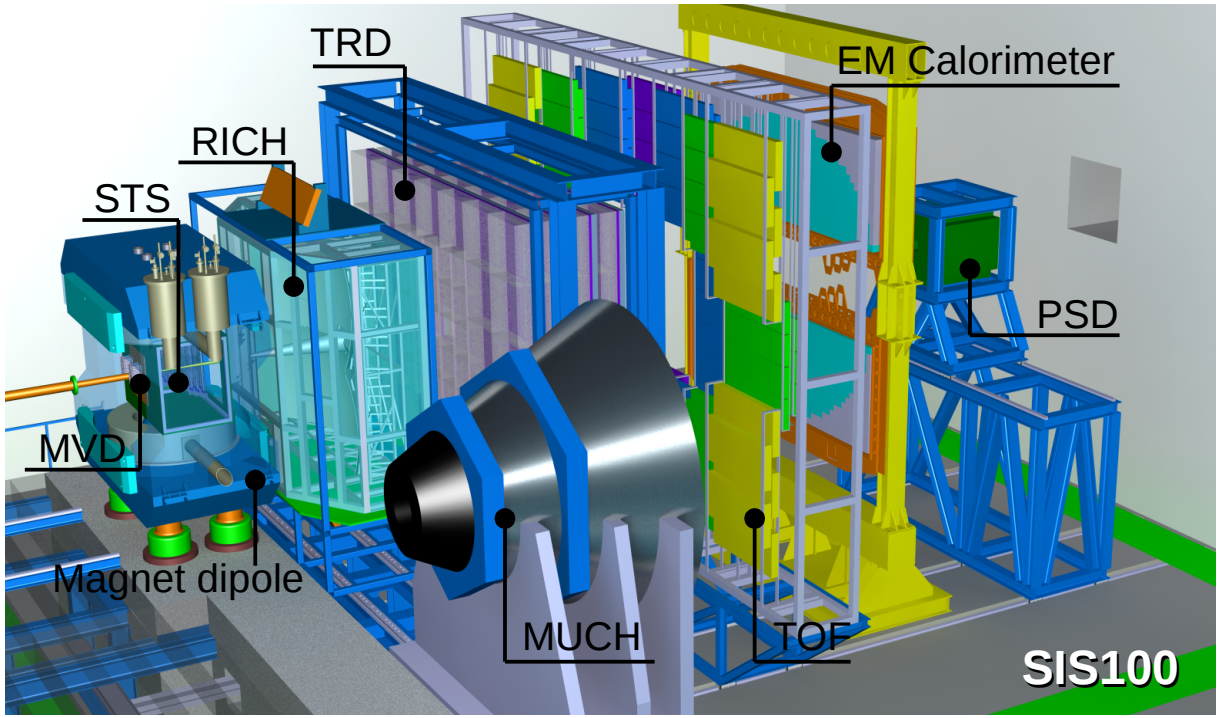
Adrian Rodriguez Rodriguez for the CBM Collaboration



Outline

- Introduction.
  - The Compressed Baryonic Matter (CBM) experiment
  - The Silicon Tracking System (STS) of the CBM experiment
- The STS Readout chain.
- The STS-XYTER ASIC.
- Noise level test results with the STS-XYTER v1.
- Brief introduction to the STS-XYTER v2.

The Compressed Baryonic Matter (CBM) experiment at FAIR



Goals:

- To explore the QCD phase diagram in the region of very high baryon densities.
- Search for the phase transition between hadronic and quark-gluon matter, the QCD critical endpoint.
- High precision measurement of rare probes.

Challenges:

- Very high collision rate (up to 10 MHz).
- No hierarchical trigger.
- Self-triggered read-out electronics.
- High-speed data processing and acquisition system.
- High granularity and radiation hard detectors & frontend electronics.

Friday, March 18, 2016, 14:00–16:00, S1/01 A04.
The Compressed Baryonic Matter experiment at FAIR
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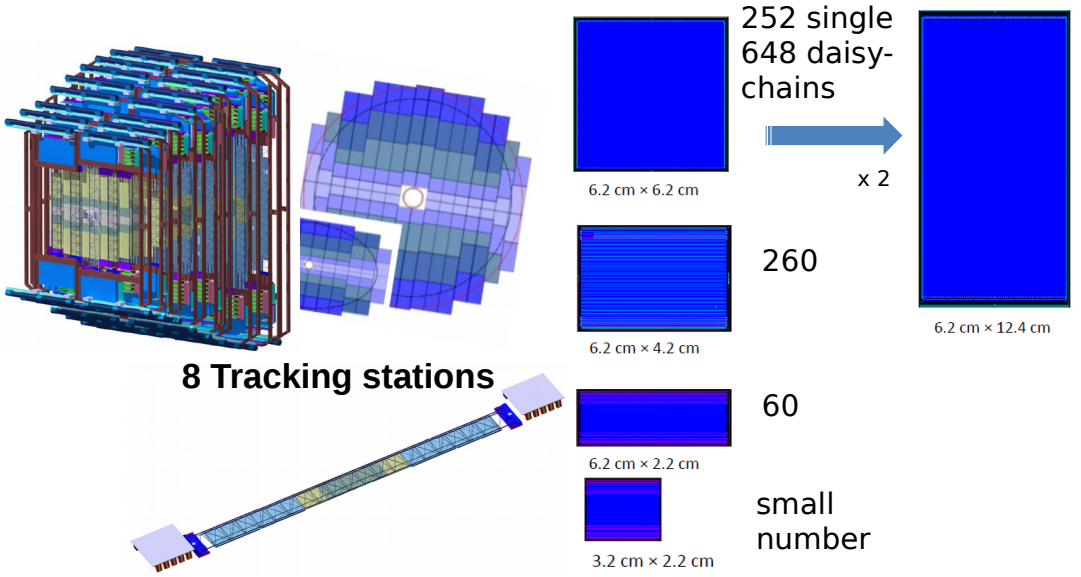
David Emschermann for the CBM collaboration

The Silicon Tracking System

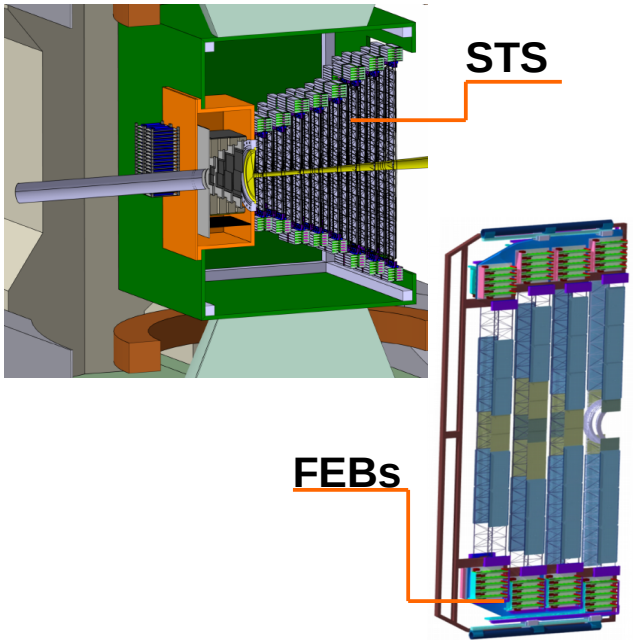
Essential component for tracking up to 1000 tracks/event at event rates up to 10 MHz in A+A collisions.

- 8 tracking stations.
- ~1300 double sided Si strip sensors (2 x 1024 strips).
- 1.8 million channels.



Challenges:

- STS is contained in a volume of approximately 1.4x2.3x1.3 m3 inside the superconducting CBM magnetic dipole (B=1 T).
- Readout electronics mounted on top and bottom of the individual detectors ladders.
- Radiation flux at the electronics place up to 200 krad/yr.
- Signal rate (typical value 150 kHz/channel) will produce 200-300 GB/s.
- Cooling and heat dissipation.



The STS Readout chain

Thursday, March 17, 2016, 17:45 HK 60.6.
The read-out chain of the CBM STS detector
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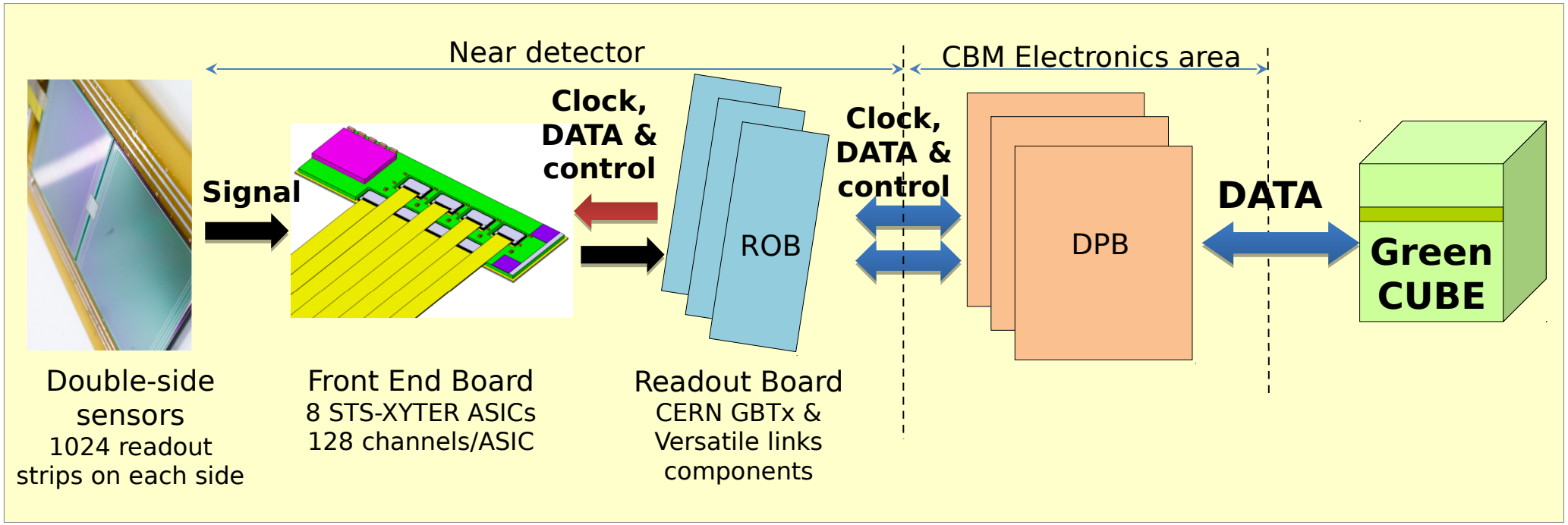
Jörg Lehnert for the CBM collaboration



1. Frontend board (FEB) carrying 8 ASICs (STS-XYTER). →
2. Readout board (ROB) for data aggregation from several FEBs, clock distribution and synchronization.
3. Data processing board (DPB) for data preprocessing, interface to slow and fast control and timing distribution.

Wednesday, March 16, 2016, 18:30. S1/05.
The workflow of CBM-STS silicon strip sensor module-assembly.
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Carmen Simons for the CBM collaboration

The STS-XYTER

ASIC dedicated for signal detection from the double-sided Si sensors.

Self-triggering chip

Provides timing and energy information for each signal.

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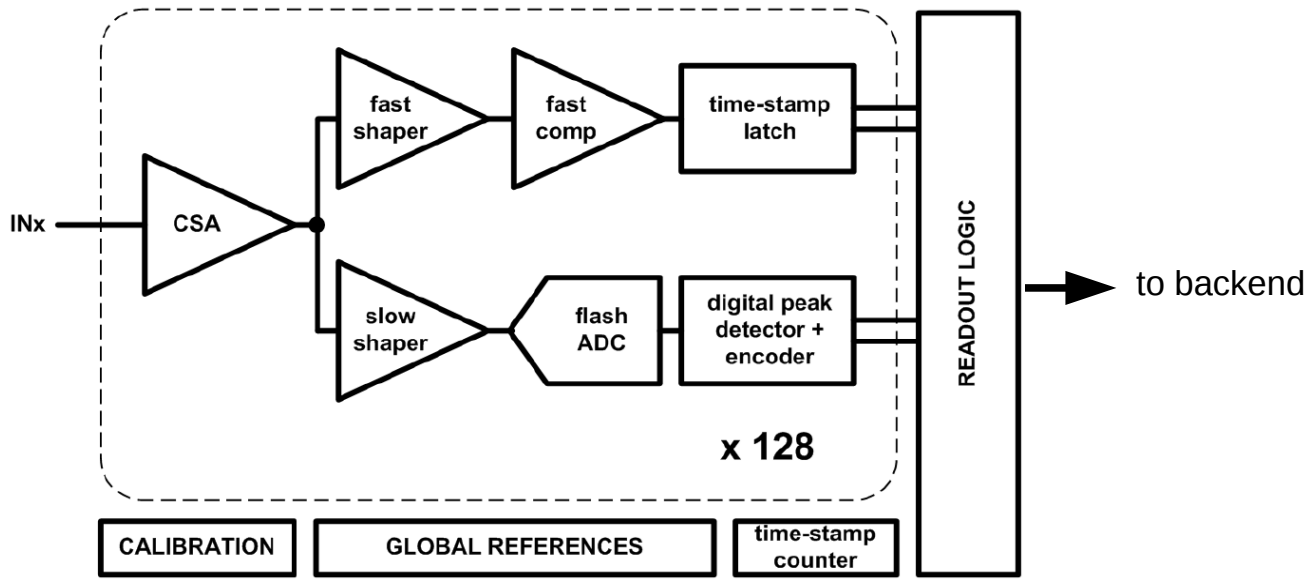


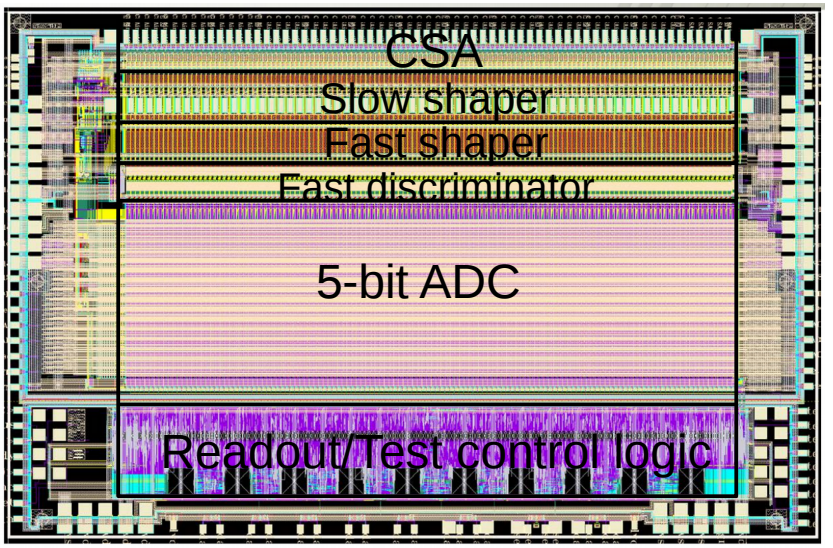
Block scheme for the STS-XYTER chip

The STS-XYTER

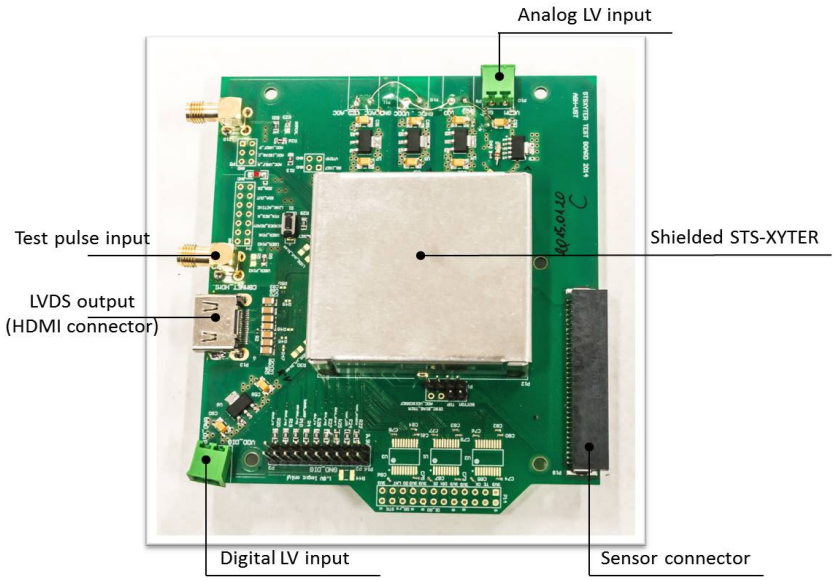
Specifications STS-XYTER v1:

- Number of channels: 128 + 2 test channels
- Input pad pitch: 58 µm
- Accepted input leakage current: 10 nA
- Sensor capacitance: 30 pF
- 150 kHit/s/ch (Typical value)
- Linearity range: up to 12 fC
- Energy resolution: 5 bits
- Input clock freuqency: 250 MHz
- Power consumption: 5 mW/channel
- Time stamp resolution: < 10 ns (after correction)
- Operating temperature range: 0°C < T < 40°C

Main goal – noise optimization!
Noise level below 1000 e- rms in charge measurement in final system



Chip overview



STS-XYTER in prototype test FEB

STS-XYTER v1 noise level measurements at GSI

Test setup:
Inside shielded box

- **2 daisy chained sensors (6.2 x 6.2 cm²)**
- **30 cm microcable readout.**
- 1 prototype FEB with 1 ASIC.

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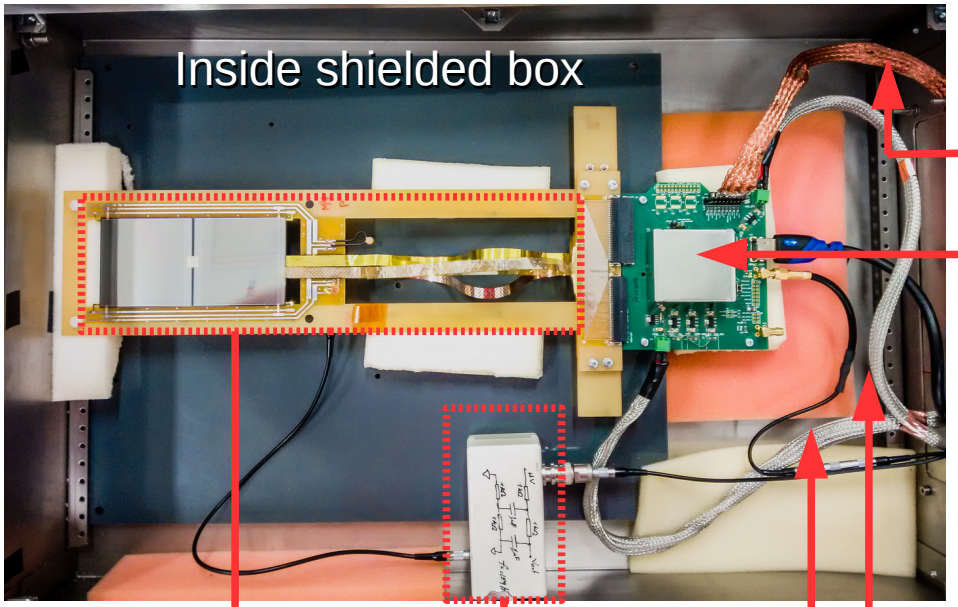
- 1 Syscore 3 ROC
- Configured with CBM-NET backend.



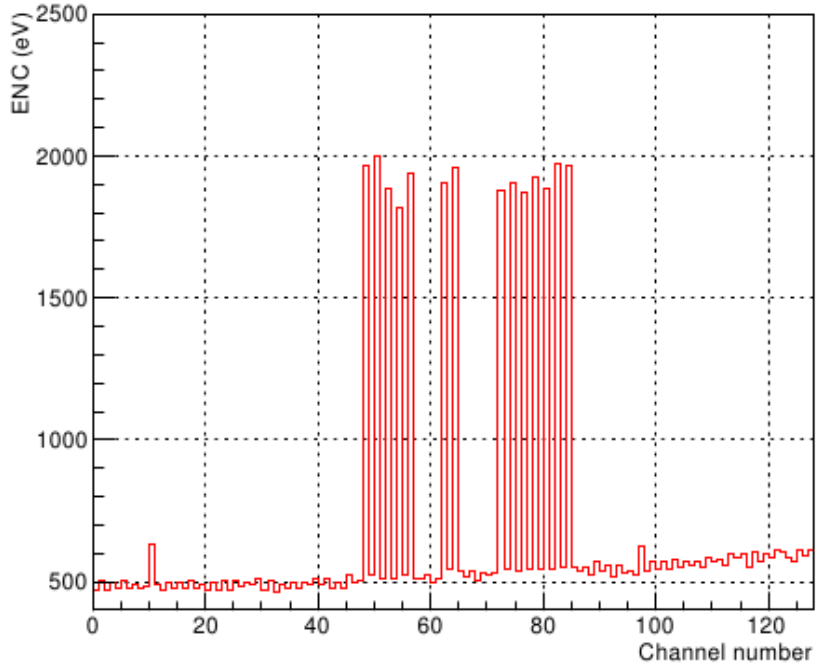
Evaluating noise levels
Noise sources:

- Sensor bias.
- Sensor capacitance, resistance and microcable.
- FEB low voltage cables.
- Common mode noise.

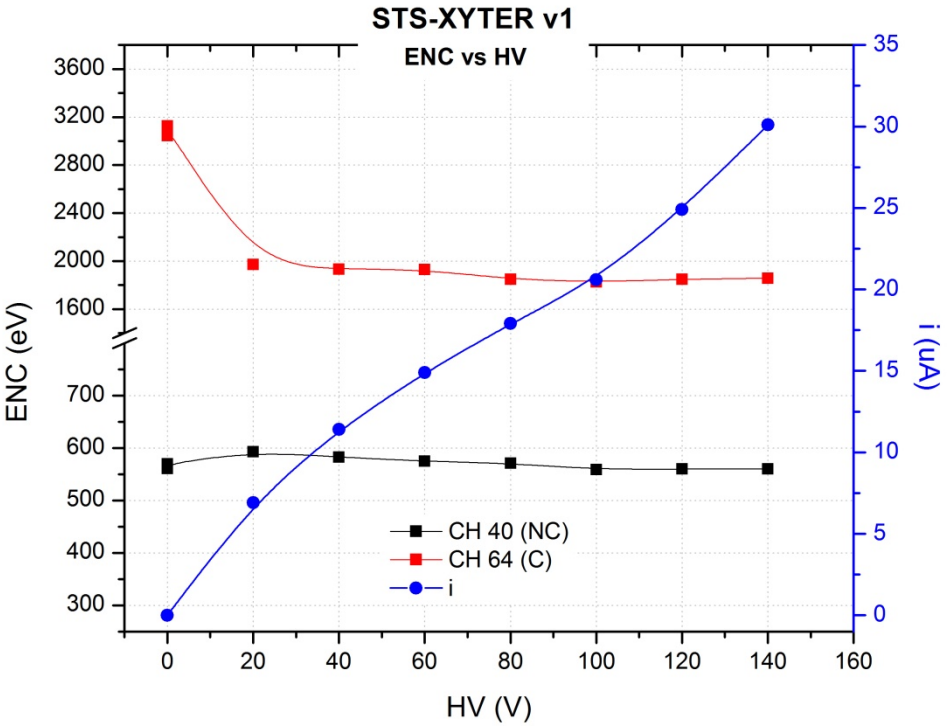
Optimization:

- Two stage RC and LC filters with common mode noise suppression in the sensor bias.
- LV cables shielding.
- Ground scheme (FEB, shielding box, cables and LV supply connected to a common ground point).

STS-XYTER v1 noise level measurements at GSI



Equivalent noise charge in the 128 channels of the STS-XYTER v1. Average value over the 31 comparators.



Equivalent noise charge in connected and non-connected channels of the STS-XYTER v1 as a function of the sensor bias voltage. Lines are just to guide the eyes.

Realistic post-layout simulations estimated the noise level for connected channels around 1600 e-.
Measured average ENC values around 1900 e-.

The STS-XYTER v2**

Currently under development. It is expected to be available in Q2 of 2016

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- New Analog Frontend:
  - New CSA based on a NMOS input transistor.
    (Study towards best ENC, testability, ensure fail-safe operation)
  - Modified shapers.
    CR-RC (fast), CR-RC3 (slow).
    (Slow shaper enable selection of shaping times 90 ns-280 ns)
- New digital backend:
  - New readout protocol and interface.
    (Optimized for operation with the GBTx)
- Other features:
  - 128 channels
  - Sensor capacitance: 30 pF → (20-50 pF)
  - 150 kHit/s/ch → (250 kHit/s/ch)
  - Time stamp resolution: < 10 ns (after correction)
  - 5 bit flash ADC
  - Power consumption: 5 mW/ch → (10 mW/ch)

Goal:
Noise reduction!

**STS-XYTER2, a prototype detector readout chip for the STS and MUCH. K. Kasinski. CBM Progress Report 2015.

Summary

- The STS-XYTER chip is dedicated for signal detection from the double-sided Si microstrip sensors in the CBM experiment.

- The STS-XYTER v1 noise level has been measured; values are in good agreement with realistic chip simulations. Main goal is the optimization of the ASIC performance in terms of noise level.

- The STS-XYTER v2 is currently being under development. Several modification and changes were considered in its design to reach the noise requirements and improve chip performance.

Thank you for your attention!