

kvi - center for advanced radiation technology

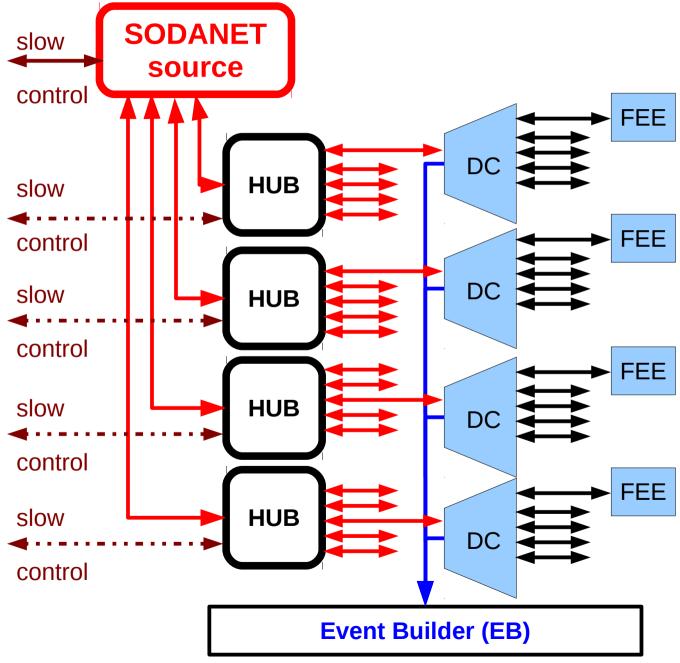
Status of the SODANET

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SODANET Topology



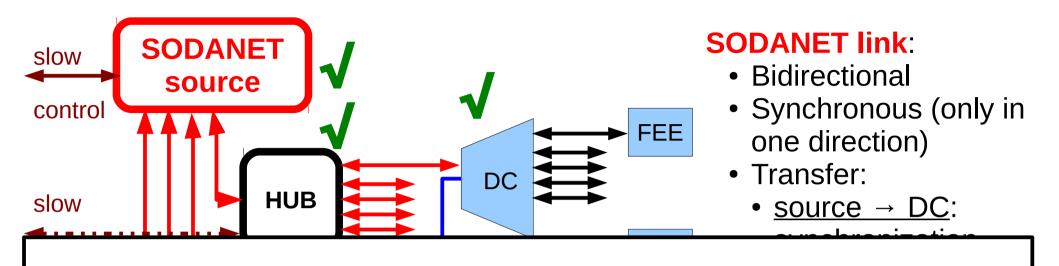
SODANET link:

- Bidirectional
- Synchronous (only in one direction)
- Transfer:
 - source → DC: synchronization information and FEE configuration
 - <u>DC</u> → <u>source</u>: slow control, used for time calibration

Data link (DC → EB):

- Unidirectional Ethernet
- Link DC ↔ FEE:
 - Bidirectional, synchronous
 - Protocol up to subsystem

SODANET Topology



This summer core components of the SODANET were Re-implemented, which resulted in a working system:

SODANET is completely implemented and tested on:

Lattice FPGA (ECP3, TRBv3), used by STT, DIRC, LUMI Xilinx FPGA (Kintex-7), used by SODANET network, EMC, MVD

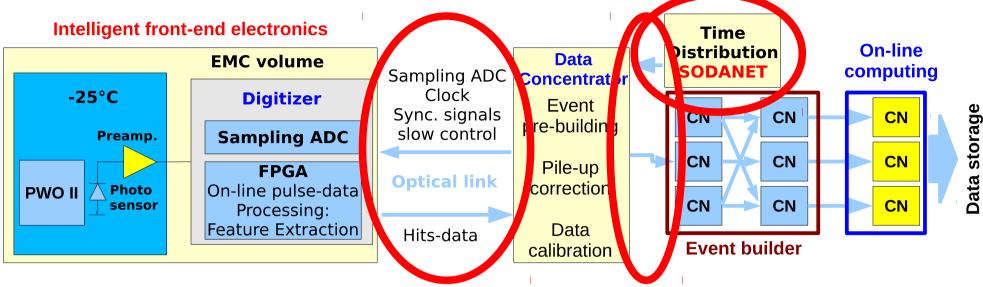
So far SODANET is integrated only into the EMC and STT readout

Event Builder (EB)

synchronous

 Protocol up to subsystem

EMC-Readout Scheme

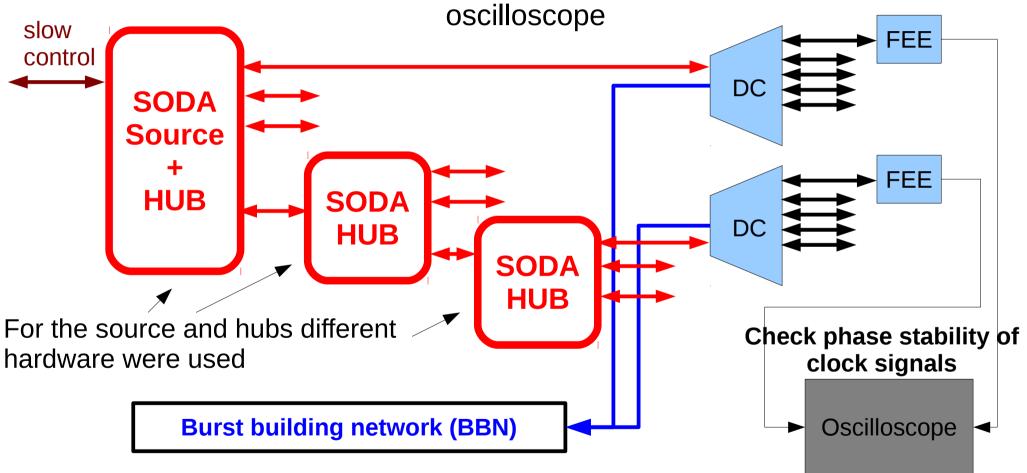


Components of the EMC readout:

- Intelligent front-end: digitizer
- Time-distribution system
- Data concentrators
- Burst-building network
- On-line computing

SODANET Test System Clocking

During test relevant SODANET links were randomly disconnected and after recovery of the system stability of the clock-signal phase was checked with

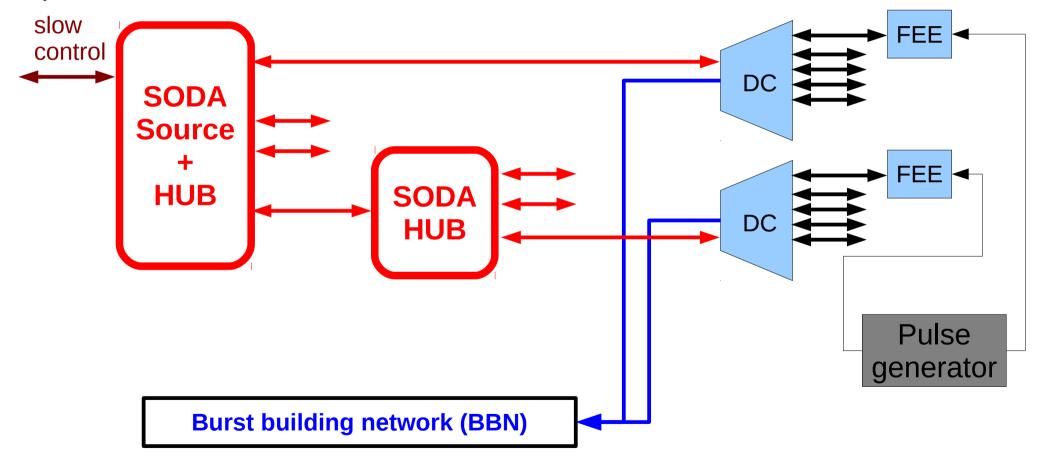


Systems with up to three levels of SODANET hubs did not show any instability

SODANET Test System Synchronisation

Signal from one pulse generator was measured by two different front-ends.

During measurement FEE modules were reset to test synchronisation procedure



Time-stamps of measured pulses were compared:

time difference should be constant

SODANET Test System Synchronisation

Signal from one pulse generator was measured by two different front-ends.

During measurement FEE modules were reset to test synchronisation procedure

adc nr adc nr pulsedata ×1 4D Minimum energy results voltages adc nr Status error Status Status 0 <u>/</u>) 0 0001 00 0 0.7 Superburst Timestami Timestamp 0.6 index 0 197860628 2378 2369 CF_delay () x **1** 0.5 Timestame Timefraction Timefraction 10 index 1 0.4 2378 283 314 () × 4D Timefraction 0.3 Energy Energy Sample freq 283 13580 13704 0.2) 80M Energy Superburst diff Superburst 0.1 1.12311E-7 13580 1978606 1978606 Measured timestdev 1.13329E-10 0.2 mean 1.12137E-7 0.3 Initialize Array difference between Plot 0 /// Waveform Graph () 0 0.4 adc nr Status 4000 -0001 × 00 0.5 detected pulses 3500-Superburst 0.6 197860628 0.7 Timestamp VISA resource name index 2500 2378 • 0 ^I/₆ USB0::0x0699::0x0343::C024592::INSTR Counts Timefraction 2000 Stop wait[s] 10 283 Start state off 1500 -Energy 13580 1000 -VISA resource name in 500-TRBnet path Save actual_path 8 VISA resource name out 1.1175E-7 1.115E-7 1.12E-7 1.1225E-7 1.125E-7 1.1275E-7 K TRBnet 2 Time + , , ,)

Measured time difference is constant \rightarrow

synchronisation is working properly

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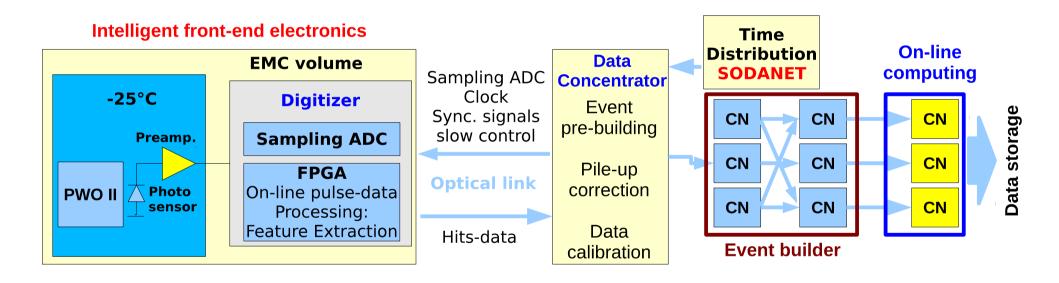
Summary

- Supported platforms:
 - Lattice (ECP3, TRBv3)
 - Xilinx (Kintex7) platforms
- SODANET is ready for implementation for ALL PANDA subsystems:
 - EMC done
 - DIRC, STT (TDC readout)
 - MVD ?

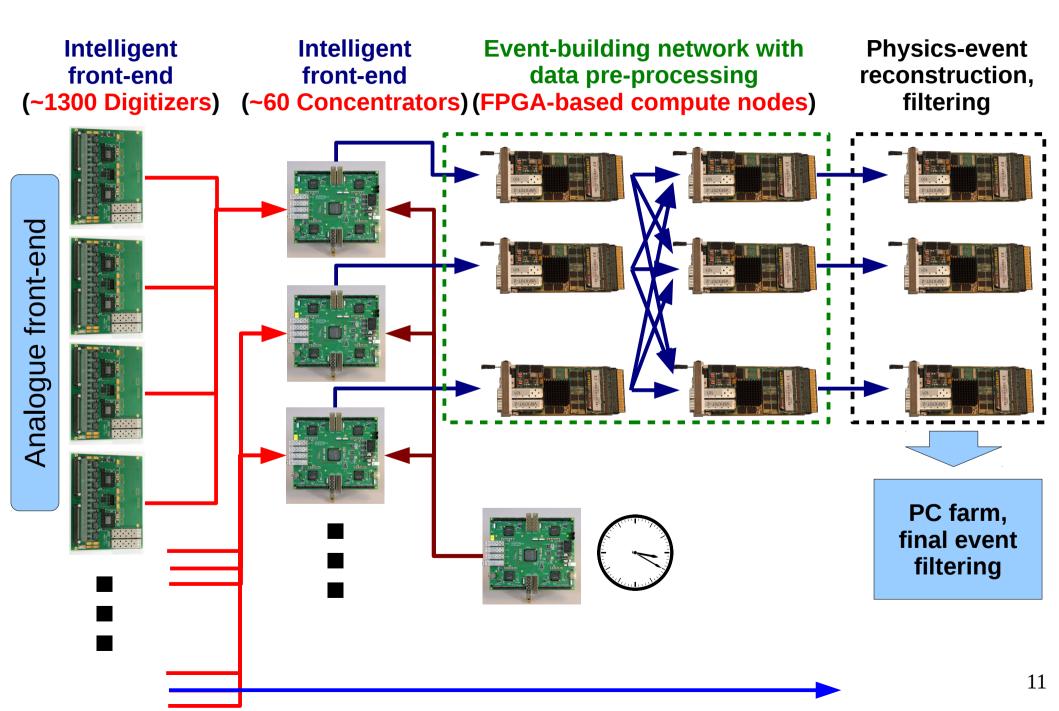
To be done

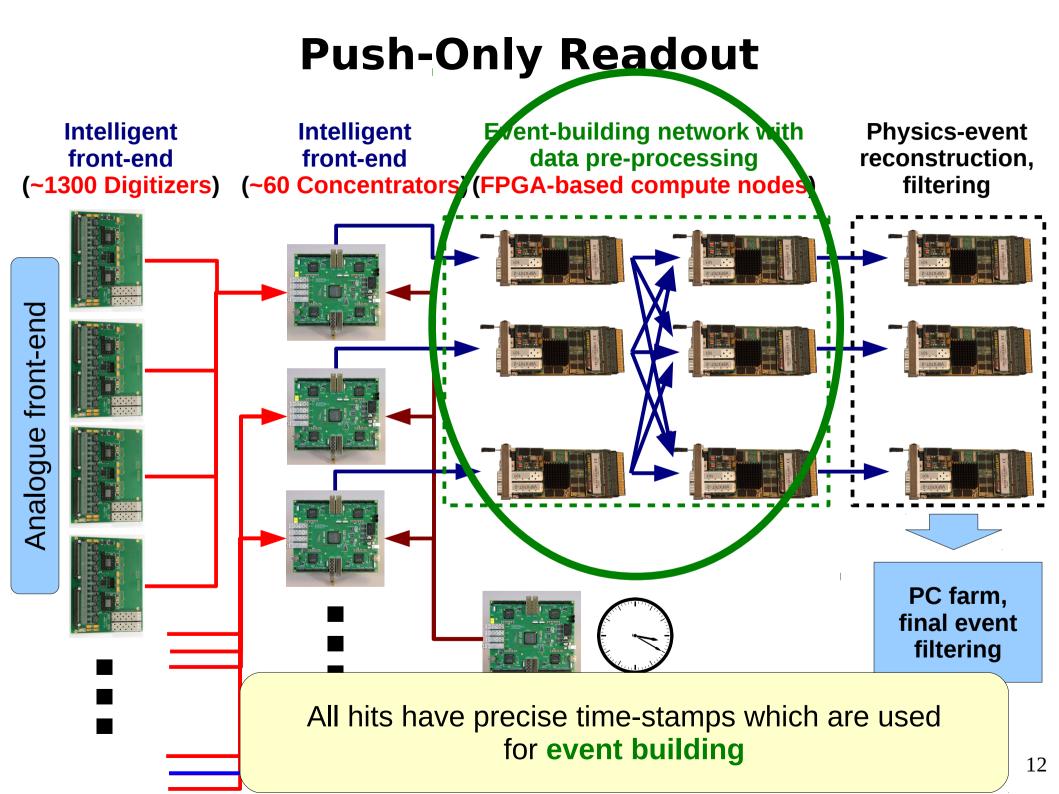
- Stability tests of the system (possible with TDC firmware for TRB board)
- Implement into readout of other subsytems
- Port to Xilinx Ultrascale FPGA families
- **Update TRBNET** component of the SODAET (current SODANET firmware uses outdated TRBNET version)
- Switch to higher network speed. TRBv3 platform is being used for R&D only: SODANET network should be based on Xilinx platform (gain of network speed from max 2.4 Gb/s to 10 Gb/s))

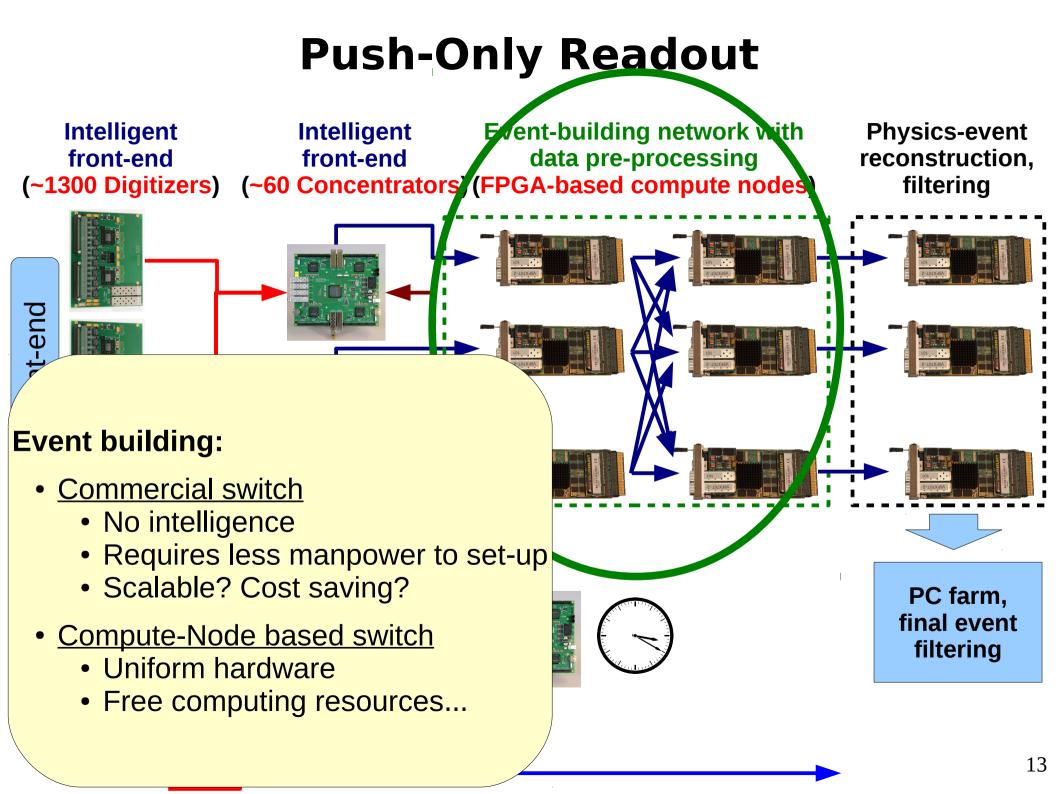
Readout of the Electromagnetic Calorimeter

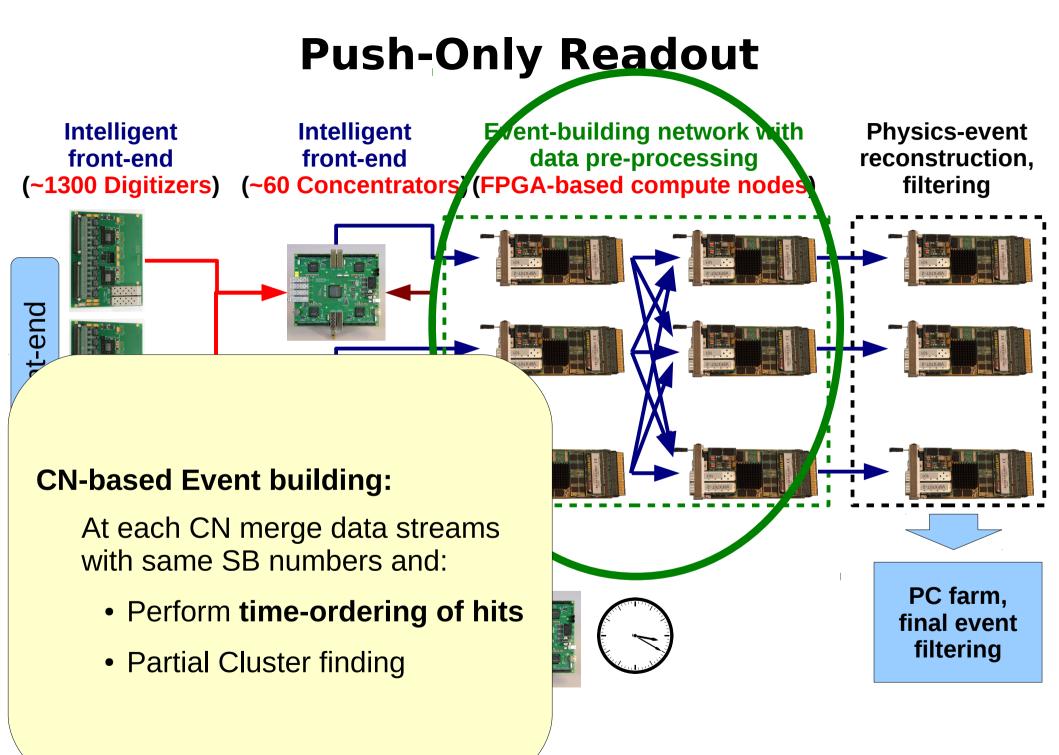


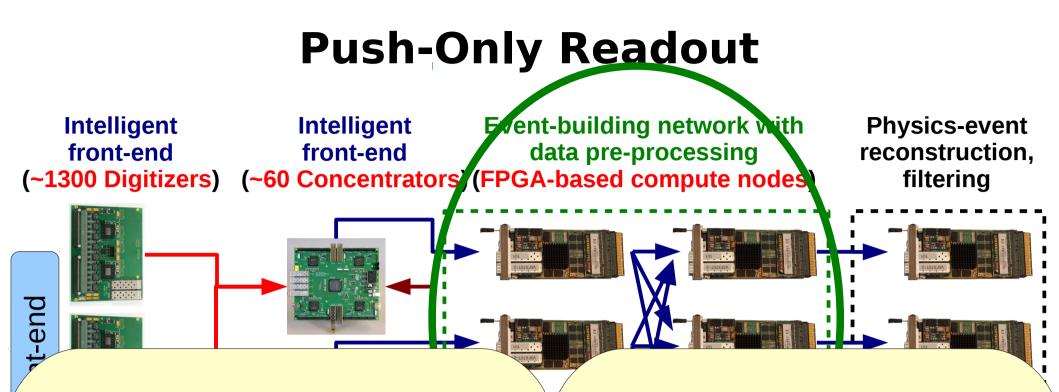
Push-Only Readout











CN-based Event building:

At each CN merge data streams with same SB numbers and:

- Perform time-ordering of hits
- Partial Cluster finding

Implemented (CN):

 Merging up to four data streams with time-ordering

Output: GB-Ethernet (considered as temporary solution)

Size of merged packets not restricted (potential problems with Ethernet output)

Push-Only Readout

