# PANDA DAQ/FEE Meeting

Sezione di Torino

# Status and perspectives for the MVD pixel detector readout ASIC

*G. Mazza*
*on behalf of the Torino MVD pixel group*

# Pixel Detector

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| | |
|---|---|
| Pixel size | *100 × 100 μm²* |
| *Chip active area* | *11.4 × 11.6 mm²*<br>*(116 rows, 110 columns)* |
| *dE/dx measurement* | *ToT, 12 bits dynamic range* |
| *Max input charge* | *50 fC* |
| *Noise floor* | *<32 aC (200 e⁻)* |
| *Input clock frequency* | *160 MHz* |
| *Time resolution* | *6.25 ns ( 1.80 ns r.m.s. )*<br>*12.5 ns ( 3.61 ns r.m.s. )* |
| *Power consumption* | *< 800 mW/cm²* |
| *Max event rate* | *6.1 · 10⁶* |
| *Total ionizing dose* | *< 100 kGy* |

# Module readout

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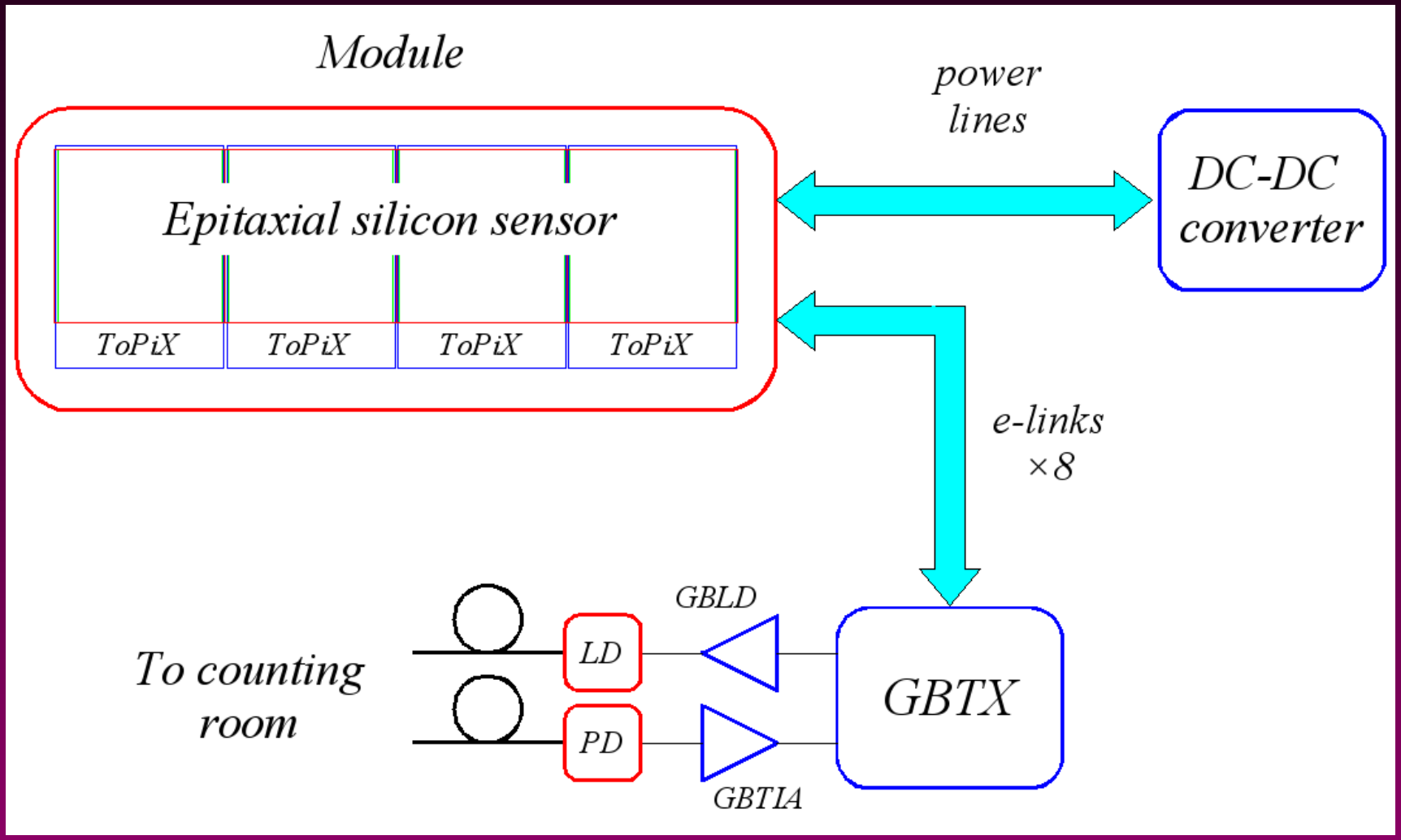
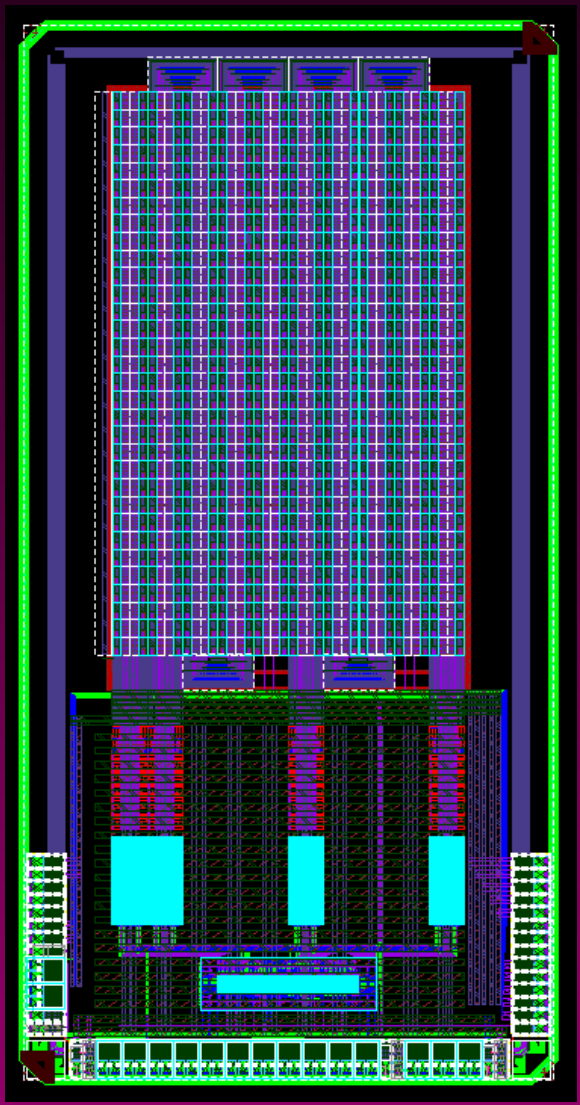


# ToPiX v4

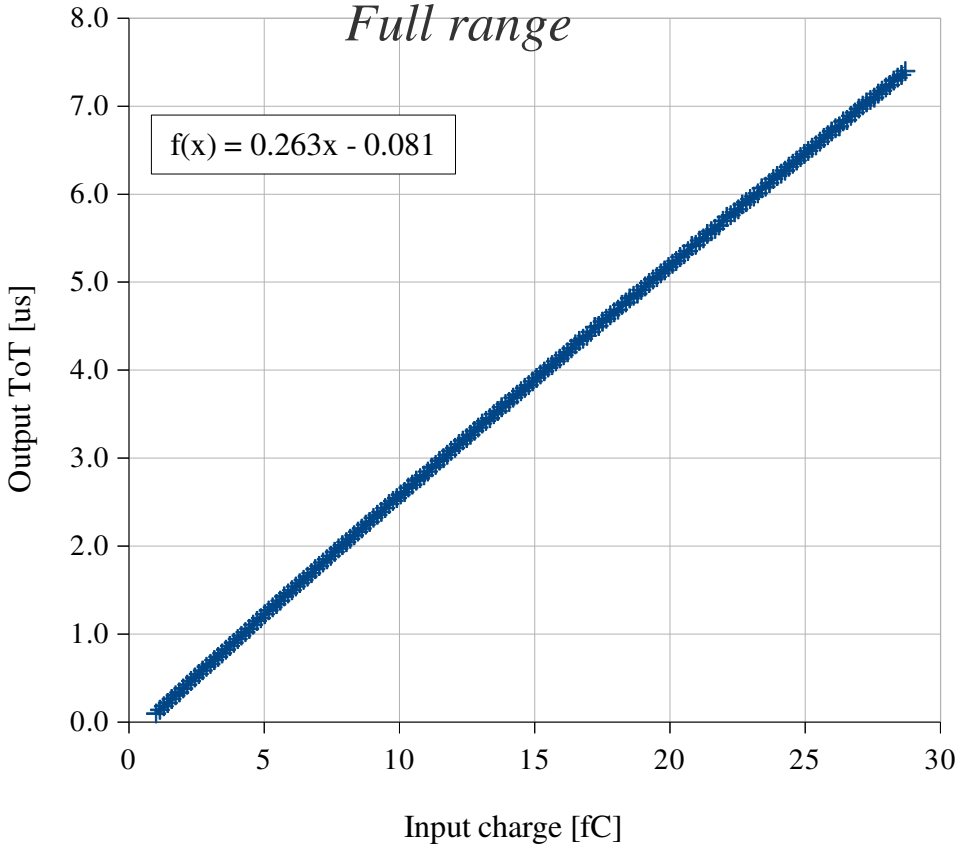
Sezione di Torino

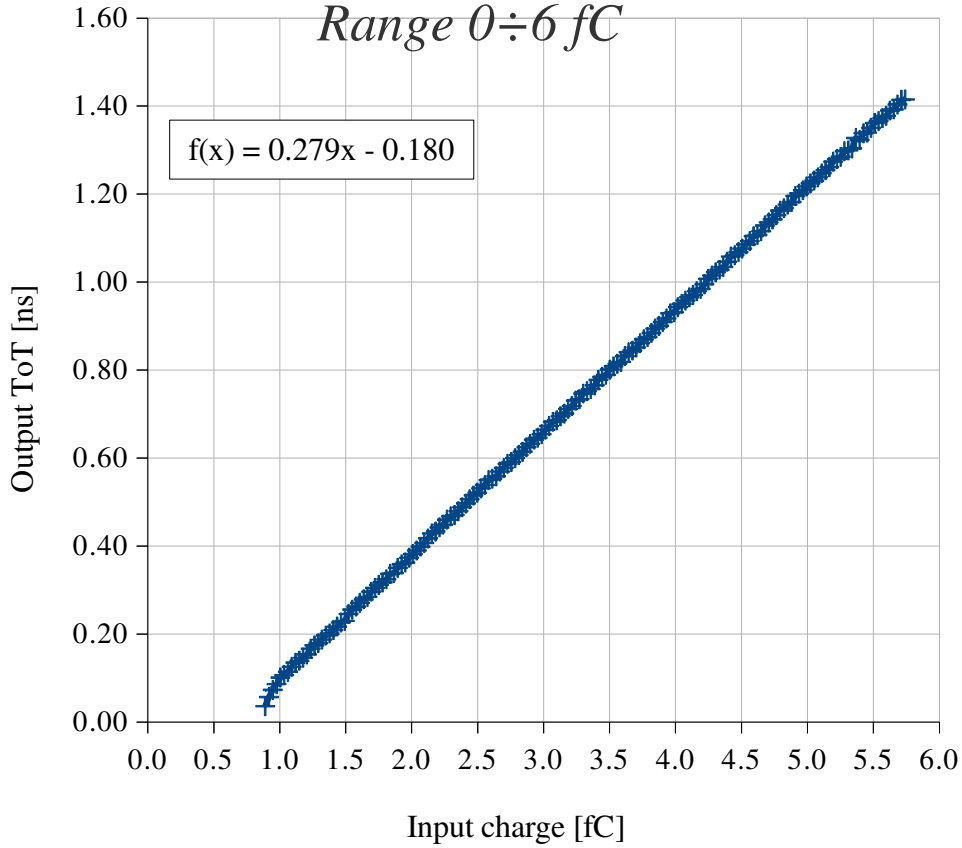


- Size : 3 mm × 6 mm
- CMOS 130 nm
- 640 pixel cells, 2×2×128 and 2×2×32 columns
- Hamming encoding and TMR pixel logic protection schemes
- Compatible with v3 sensors
- Clock frequency 160 MHz
- SEU protected EoC
- Serial data output (SDR and DDR)
- GBT-compatible SLVS I/O
- *Received on Feb 18th 2014*

# ToT measurements

Sezione di Torino



# Noise measurements

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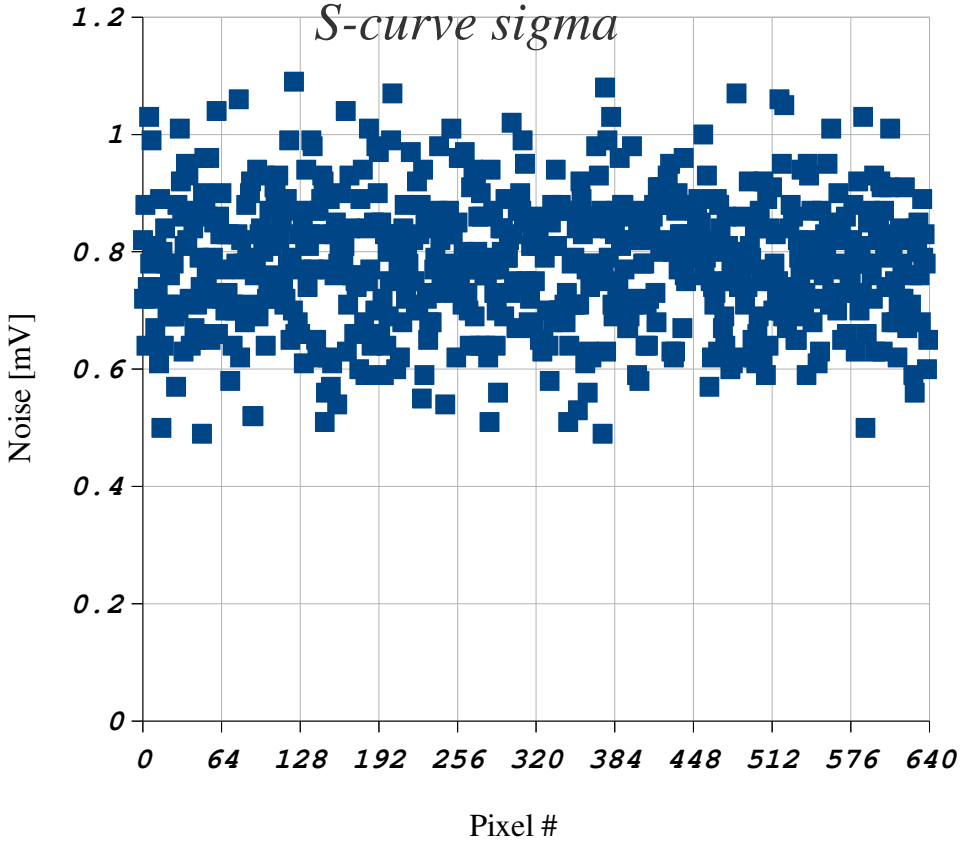
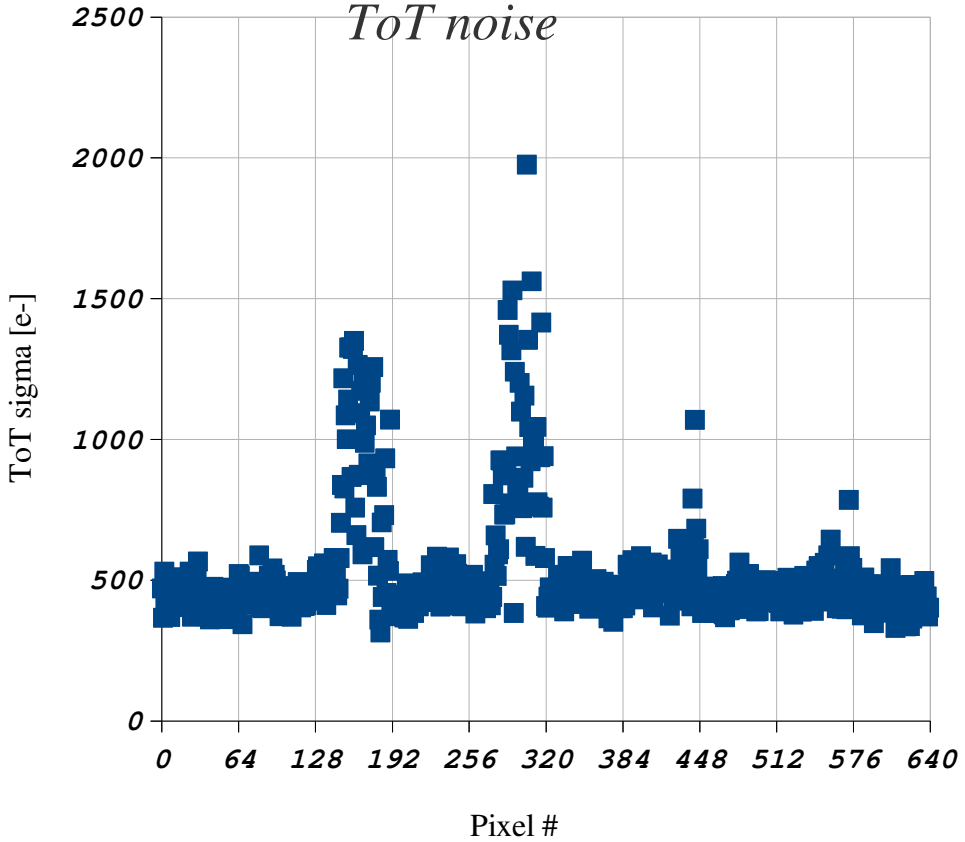
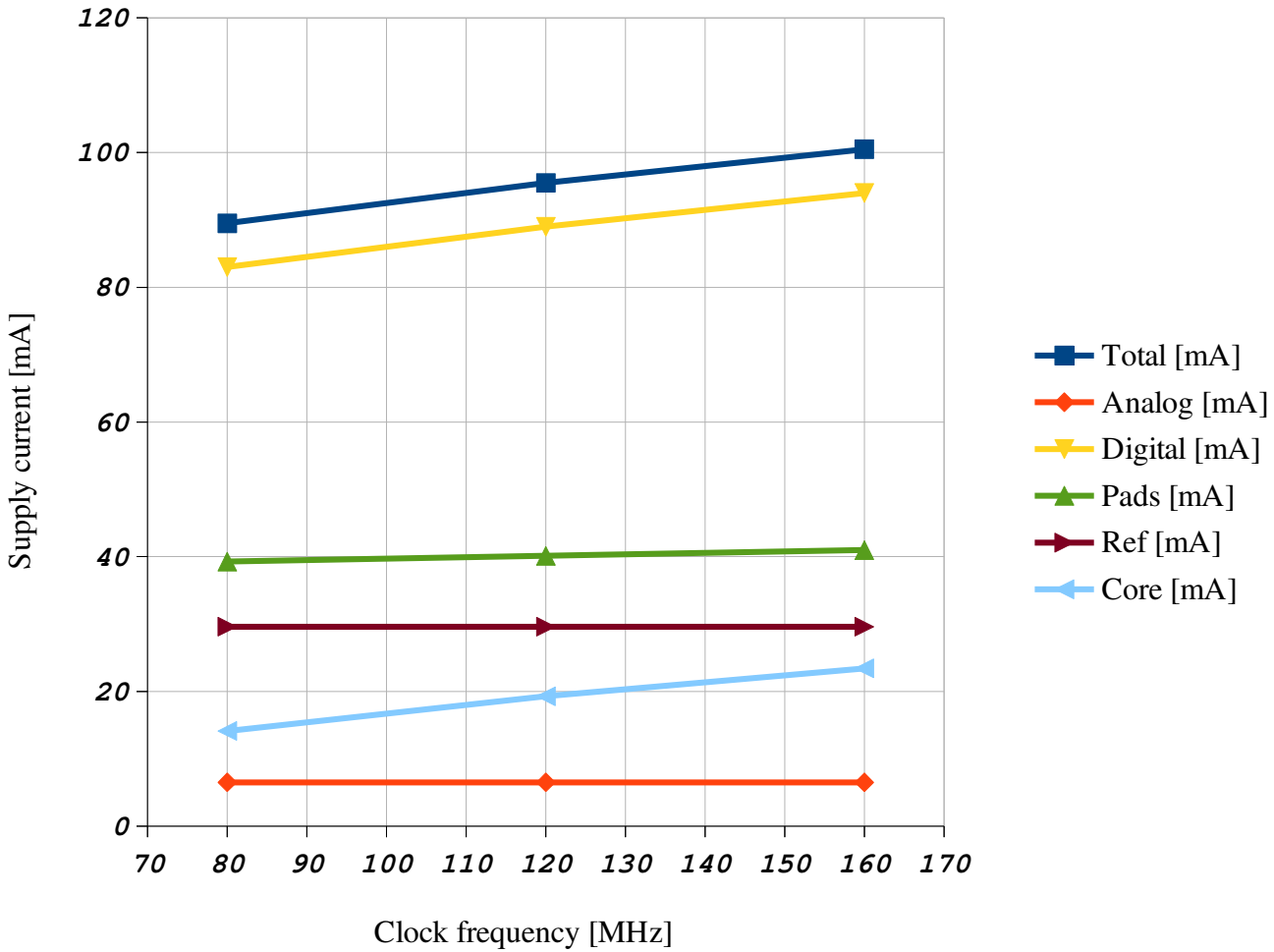


# Supply current

Sezione di Torino

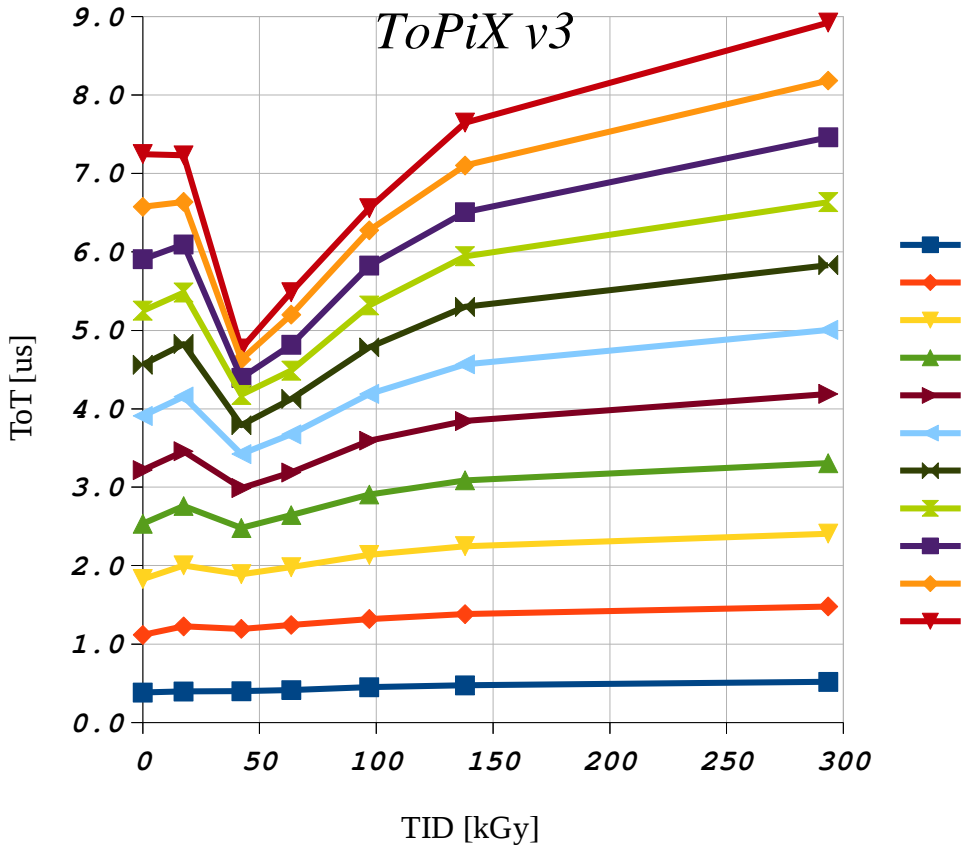


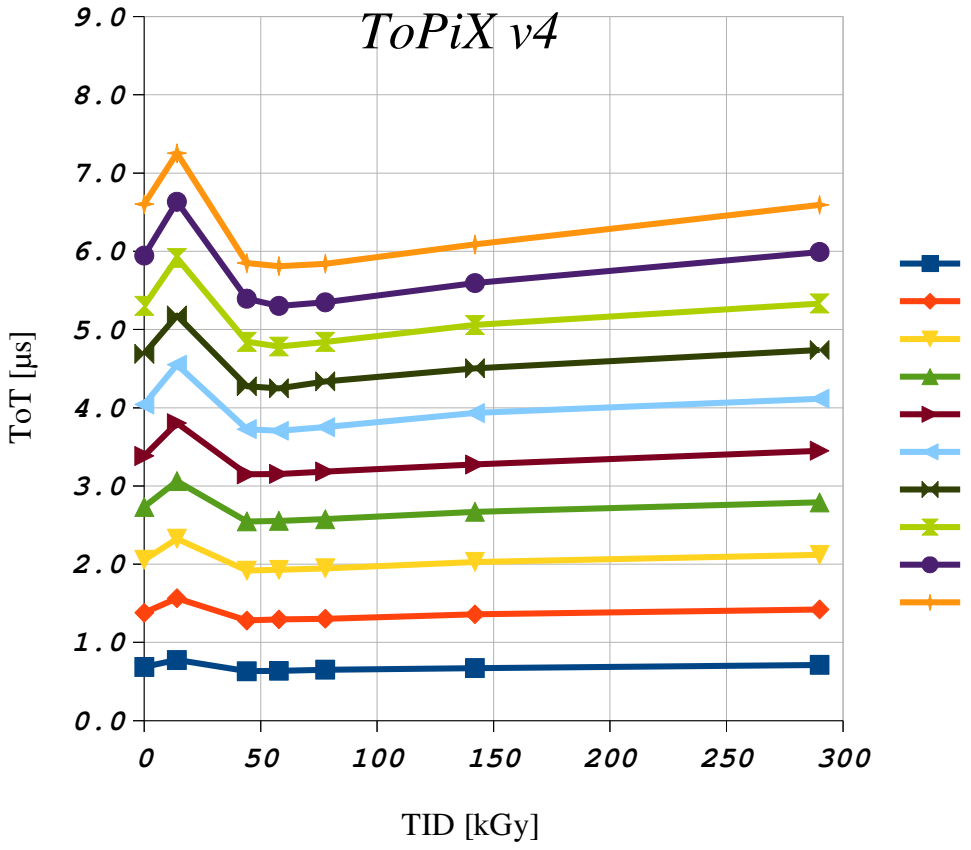

*Estimated power density for the full size version :*

*523 mW/cm$^2$ @ 80 MHz*
*666 mW/cm$^2$ @ 120 MHz*
*725 mW/cm$^2$ @ 160 MHz*

# TID mesurements ToT

Sezione di Torino



# TMR vs Hamming

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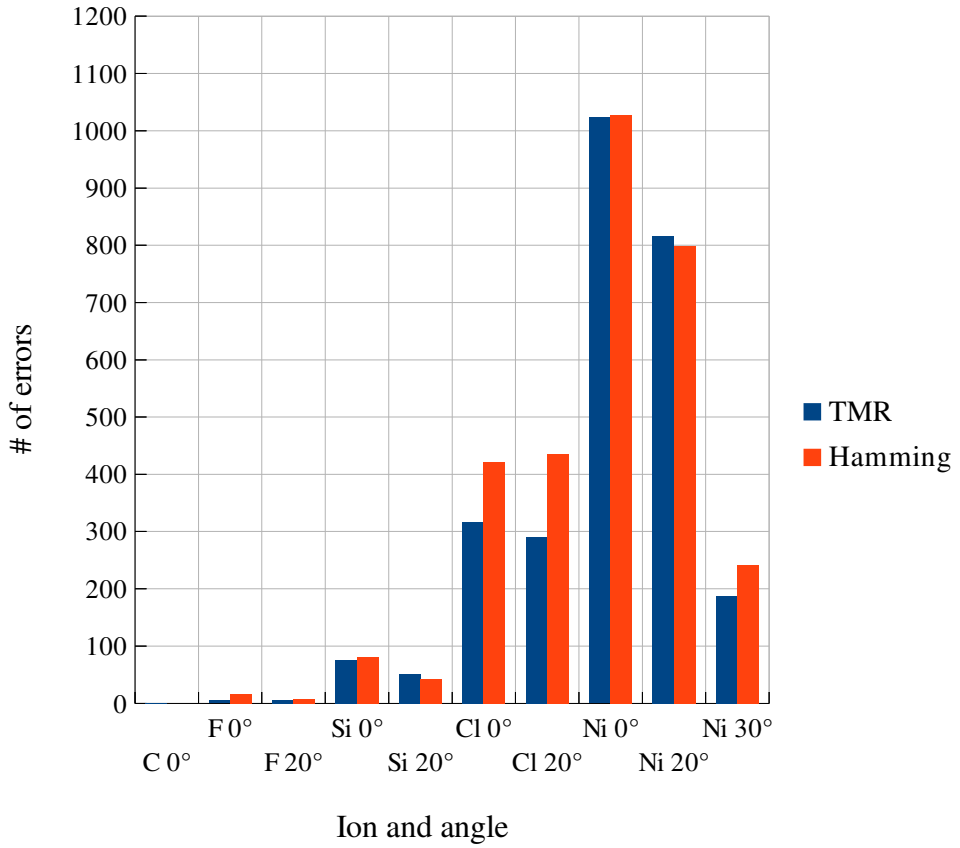


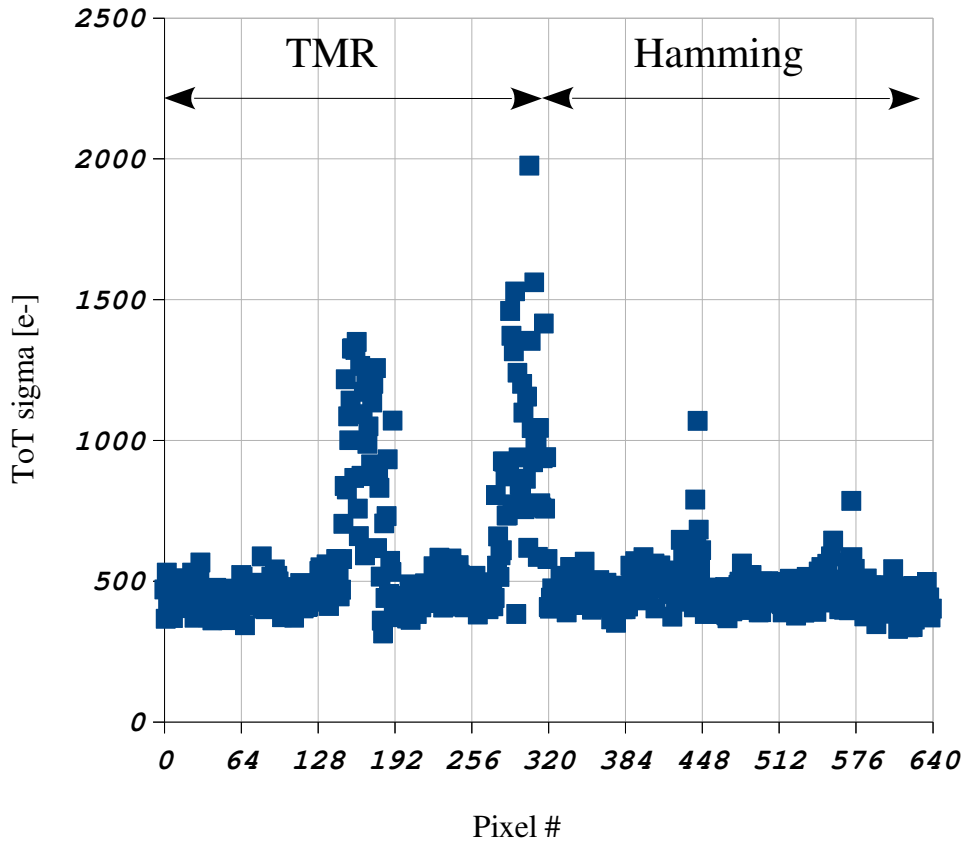

# ToPiX v5

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- Full size chip design started
- Size (*preliminary*) : 11.2 mm × 14.8 mm
- Pixel matrix (*preliminary*) : 110 × 116
- Input clock : 160 MHz
- Max output bandwidth : 4 × 320 Mb/s
- Supply voltage : 1.2 V
- Columns divided in 8 regions with 7 double columns each
- Triple tier buffering (FIFO at the end of column, region control and chip control units)

# Outlook

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- Activity on ToPiX v5 stopped on April 2015 due to issues on FAIR schedule
  - ➔ It can restart in 2016 upon approval by INFN
- Going ahead with current IBM/GF 0.13 μm technology would be a big hazard (possible technology phase-out in 2017) – looking for alternatives
- CERN has moved from IBM/GF to TSMC as their reference technology (both for the 65 nm and the 130 nm nodes)
- Critical issues for the choice of the new technology are :
  - ➔ radiation tolerance
  - ➔ metal lines resistance and capacitance (RC delay)

# Technology comparison

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| Foundry | *Process* | *Engineering run relative price* | *Metal resistance* | *Metal capacitance* | *Radiation tolerance* |
|---|---|---|---|---|---|
| *A* | *0.13 µm* | *1 (2014)* | *1 (Cu)* | *1* | *Tested @ CERN* |
| *B* | *0.13 µm* | *0.78 (2012)* | *1.5 (Cu)* | *1.2* | *Tested @ CERN* |
| *C* | *0.11 µm* | *0.36 (2015)* | *3.5 (Al)* | *1.1* | *Not tested* |
| *C* | *0.13 µm* | *0.40 (2011)* | *1.9 (Cu)* | *1.4* | *Not tested* |

*Important : price figures are just for 1st order comparison – no exact values*

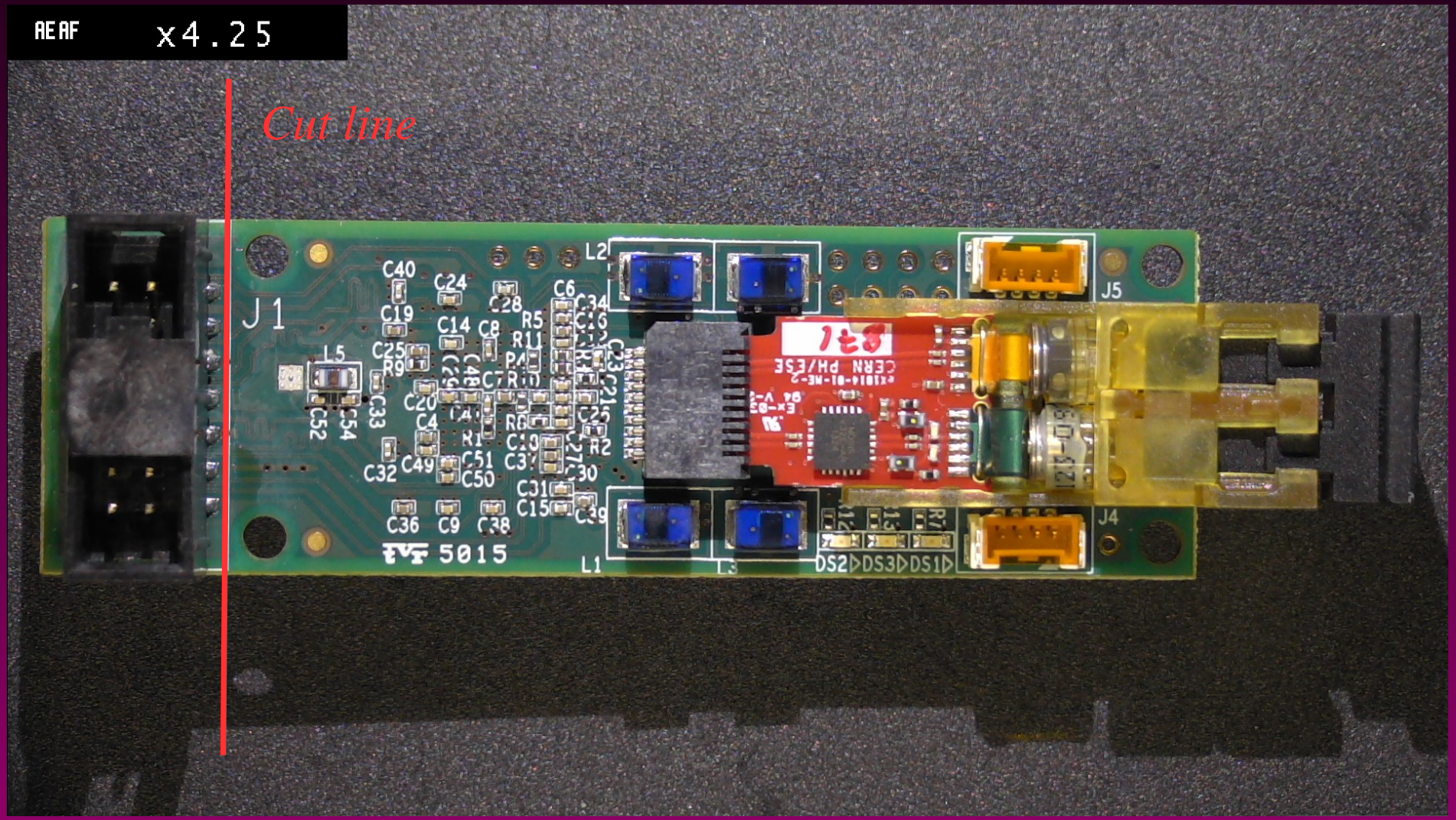
# PANDA GBTx board

*Sezione di Torino*

- Design based on the CERN VLDB board
- Board size : 70 mm × 25.5 mm
- GBTX and VTRx mounted on opposite sides for cooling reasons *(via on the 4.8 Gb/s line required)*
- Simulations show that the effect of vias on the high speed path is not dramatic
- *Test started*

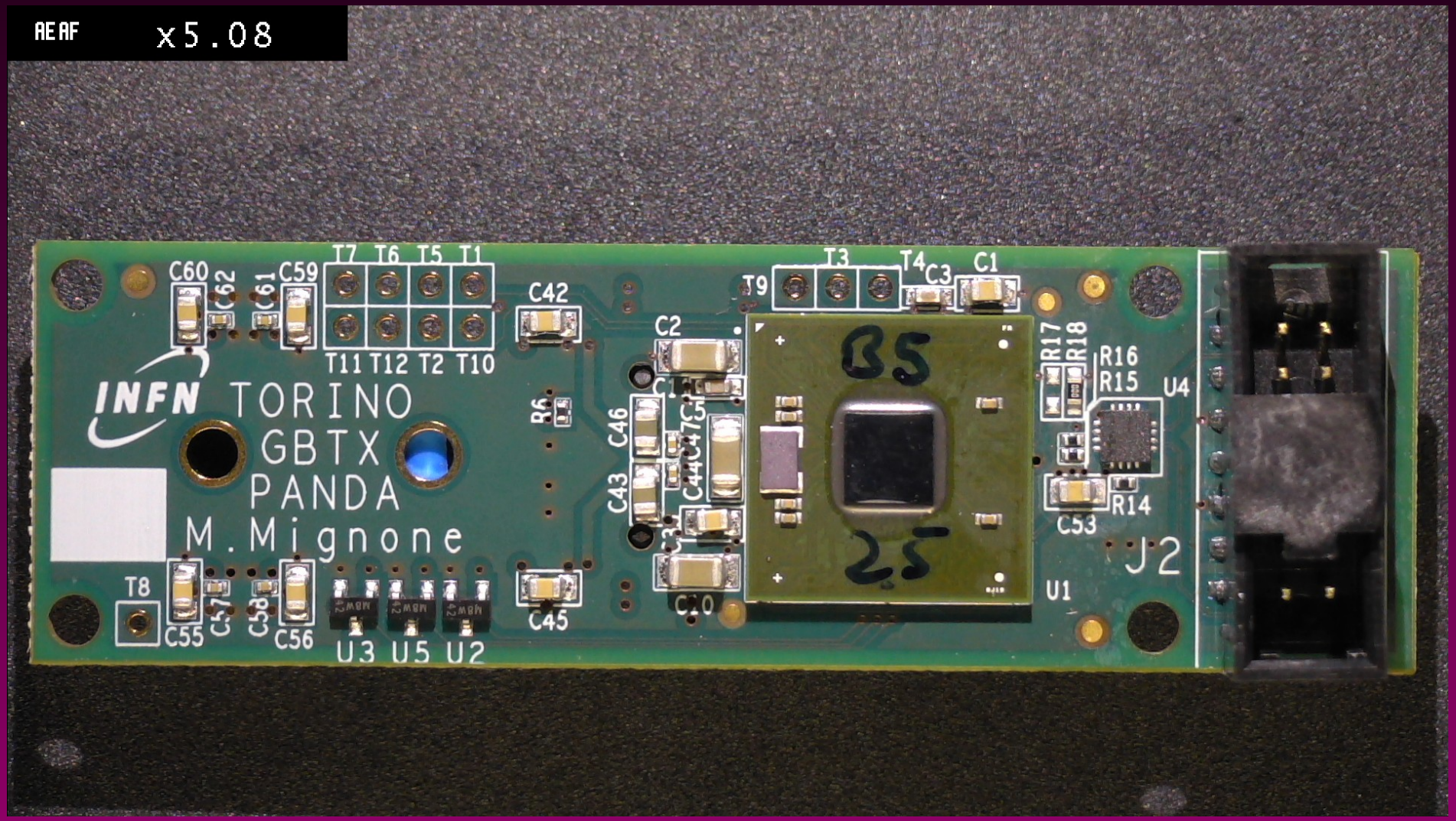
# PANDA GBTx board top side

Sezione di Torino



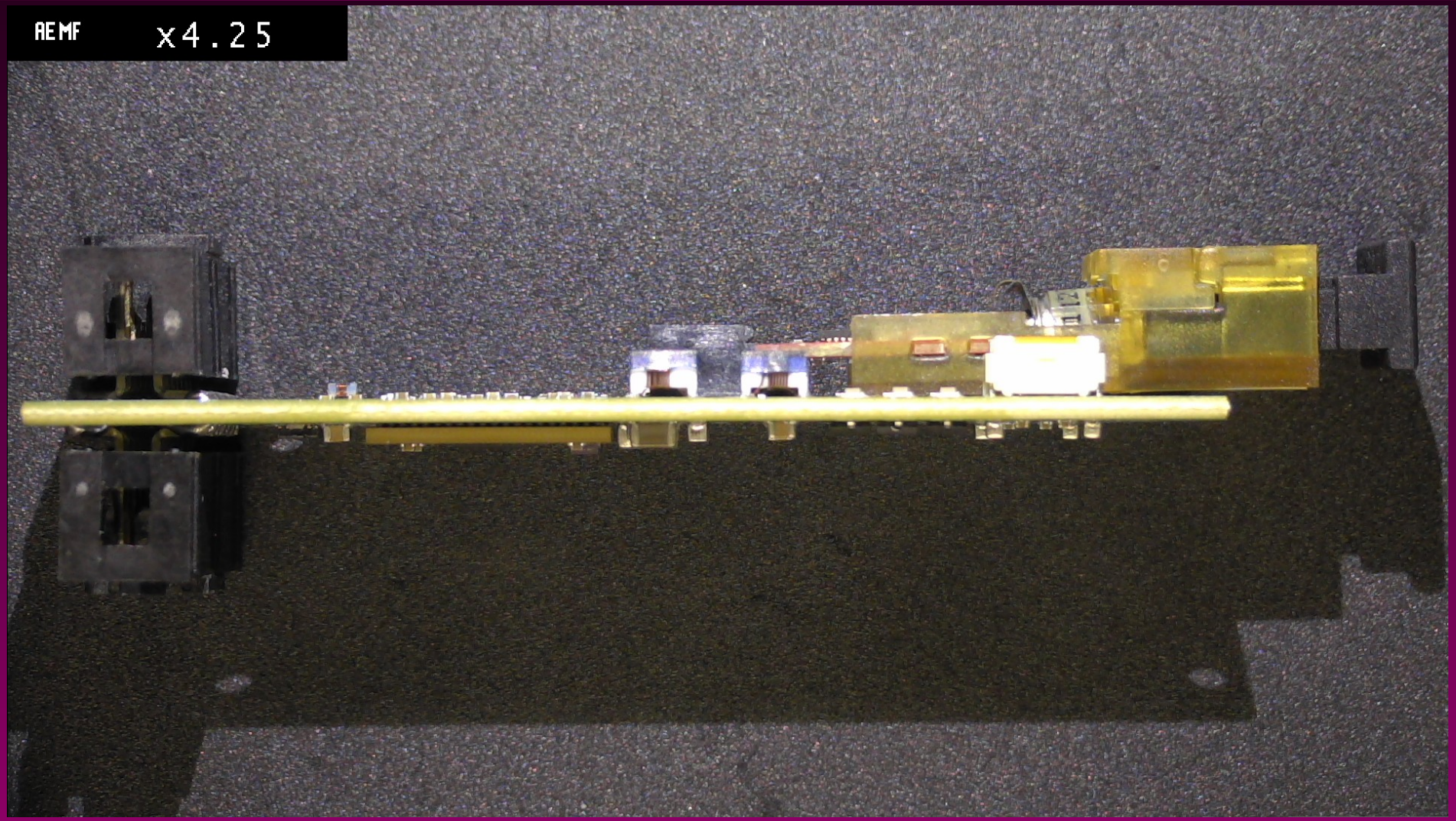
# PANDA GBTx board bottom side

Sezione di Torino



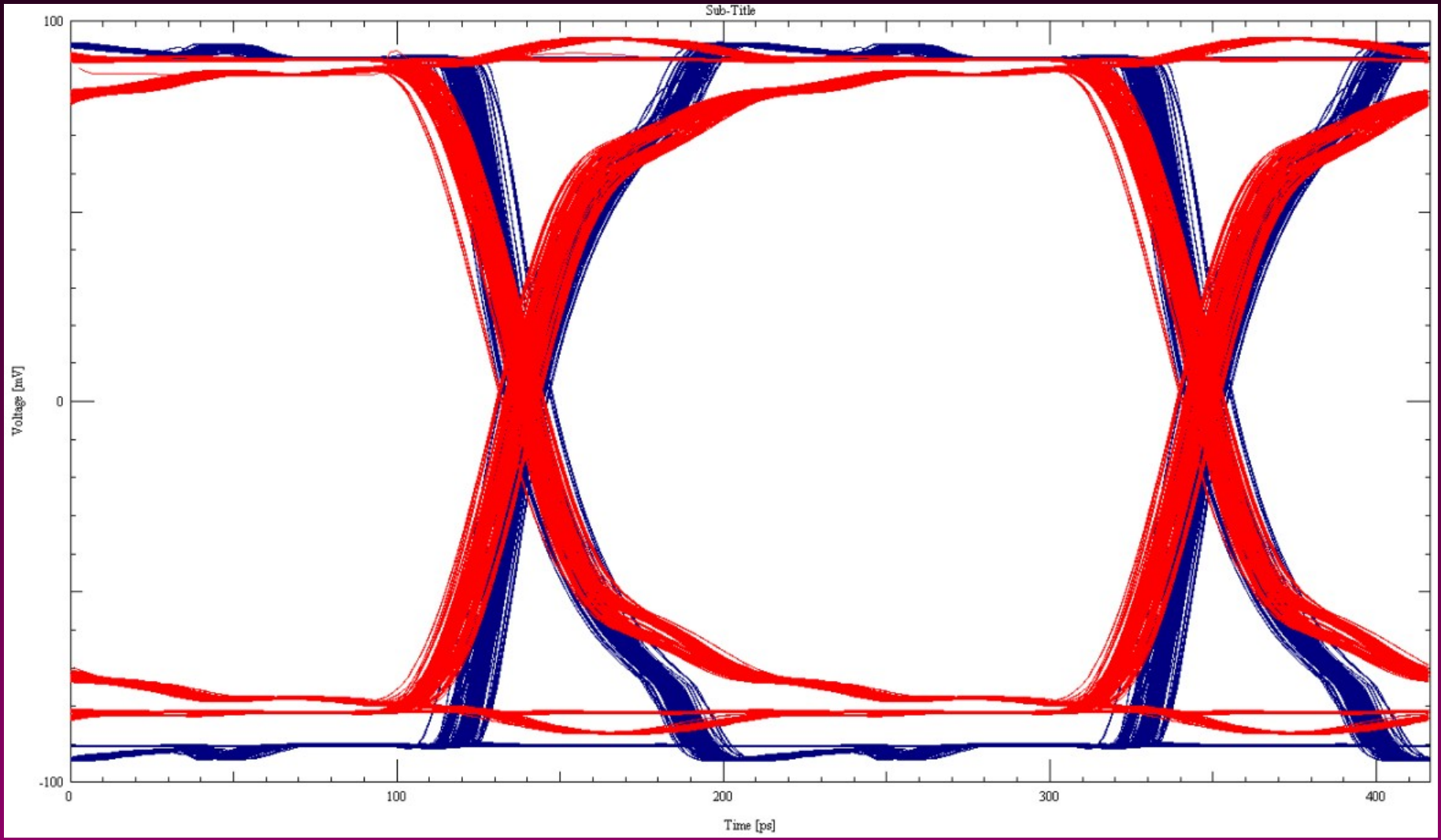
# PANDA GBTx board lateral view

Sezione di Torino



# Effect of via on the high speed line

Sezione di Torino



# Power regulator

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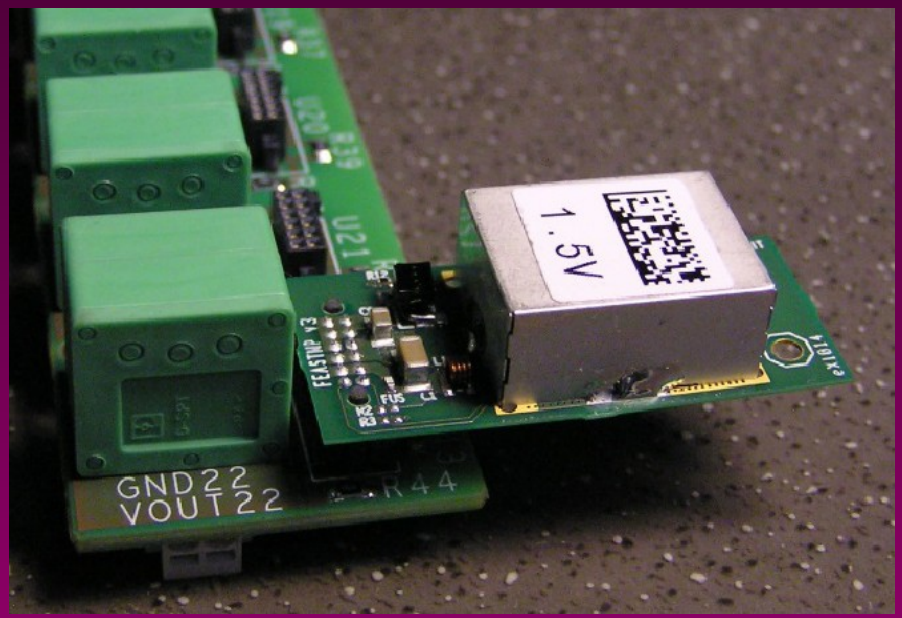
- ToPiX power supply 1.2 V – $I_{DC}$ ~ 1 A ( estimated )

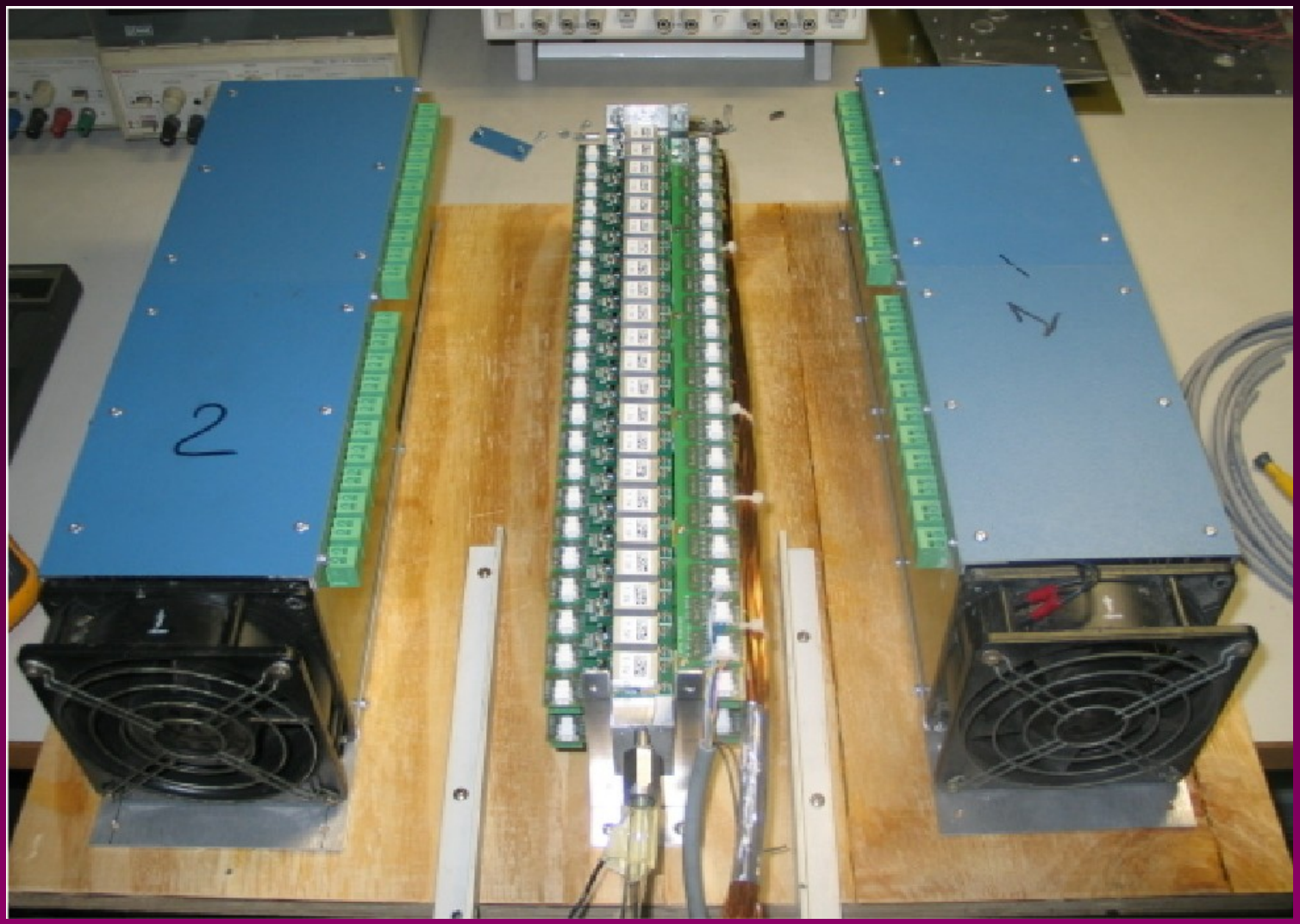
  → *voltage drop on cables is not negligible*

- A DC-DC converter solution compatible with the radiation levels and the magnetic field of a silicon tracker is under development @ CERN for sLHC
- $V_{OUT}$ = 1.5 V, $I_{OUT}$ < 3-4 A
- Tests with ToPiX v4 ok



# Power rod tests

Sezione di Torino



# Conclusions

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- ToPiX v4 has been extensively tested and is basically ok. ToPiX v5 (full size) design stopped after problems in the FAIR schedule
- It is possible a phase out of the current 0.13 μm process in 2017 – it is suggestable to move to a different technolog.A new reduced size prototype (ToPiX_v4b) will be required
- 3 processes under evaluation w.r.t. radiation tolerance, RC delay and price
- PANDA GBTx board just received – test started
- study of cooling of the DC-DC regulators bar ongoing – *first tests with 8 regulators ok.*

# PANDA FEE_DAQT Meeting

Sezione di Torino

*Backup slides*

*Gianni Mazza*

# Data format

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| 2 | 12 | 8 | 12 | 6 | |
|---|---|---|---|---|---|
| 01 | Chip address | FC | Not used | ECC | *Frame header packet* |

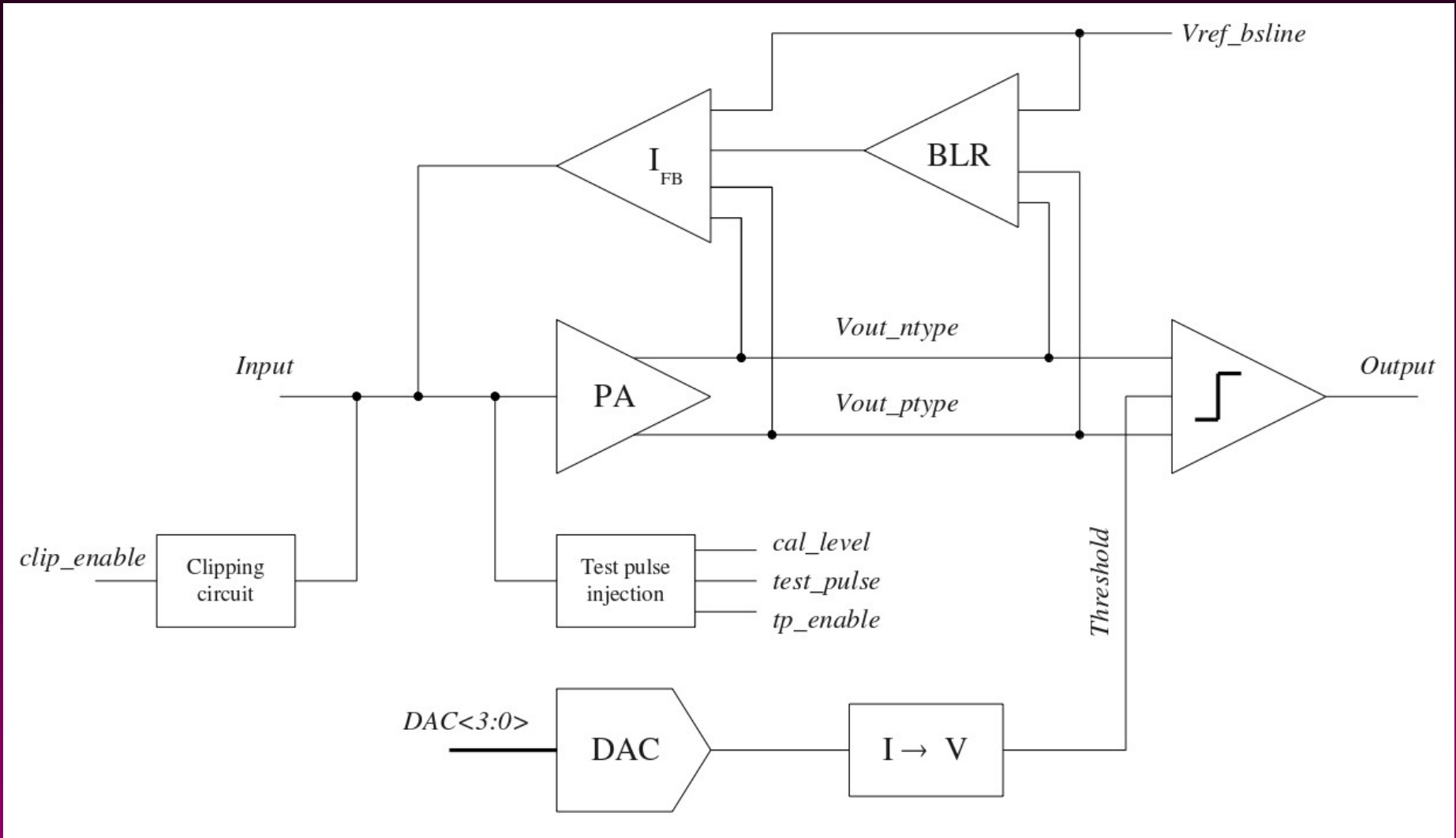
| 2 | 14 | 12 | 12 | |
|---|---|---|---|---|
| 11 | Pixel address | Leading edge time | Trailing edge time | *Data packet* |

| 2 | 16 | 16 | 6 | |
|---|---|---|---|---|
| 10 | # of events | CRC | ECC | *Frame trailer packet* |

| 2 | 38 | |
|---|---|---|
| 00 | idle code (Hex 3A55AA55AA) | *Idle packet* |

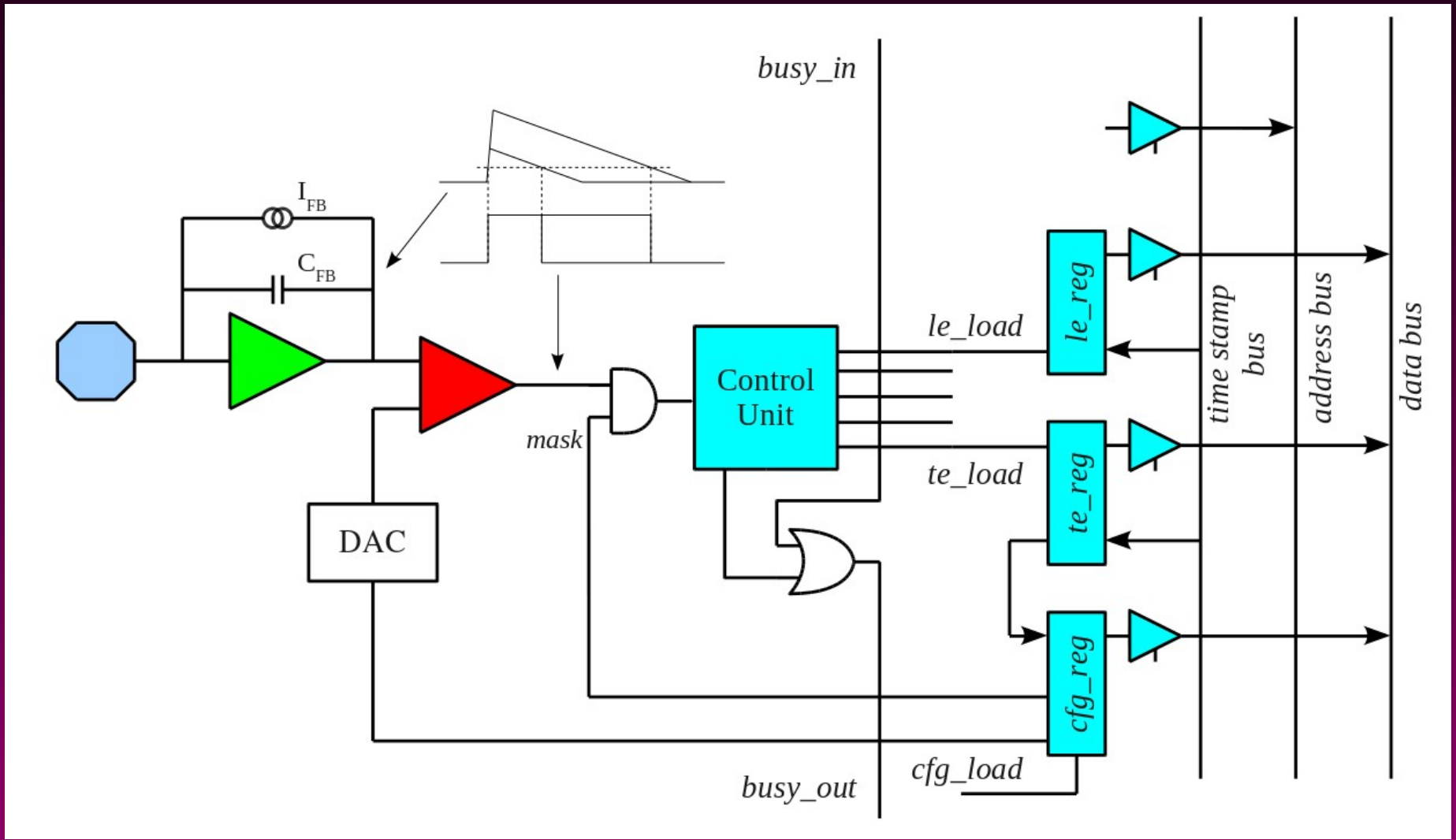
# F/E schematic

Sezione di Torino



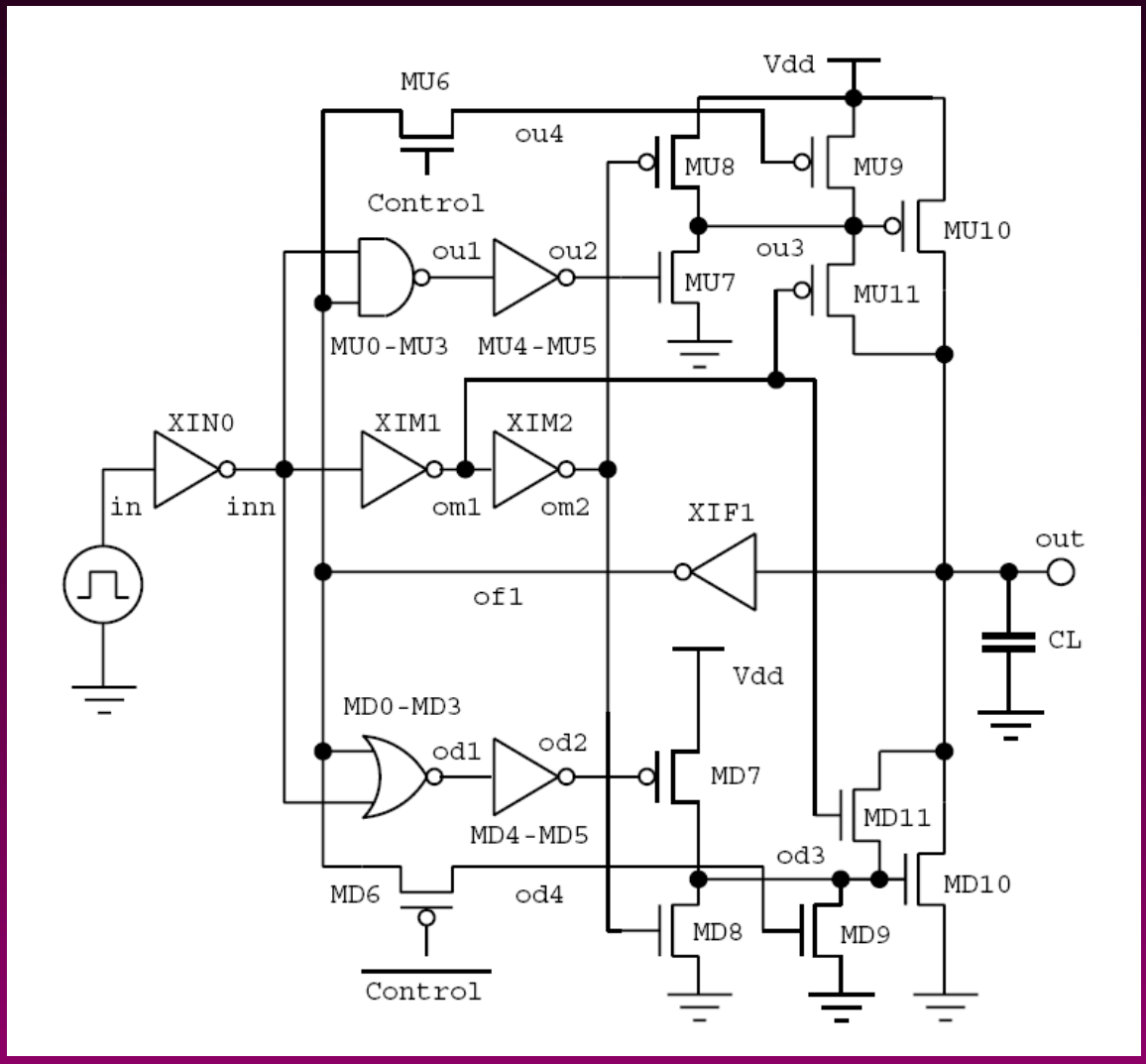
# Pixel cell schematic

Sezione di Torino



# Line driver

Sezione di Torino




Bus capacitance : 49.9 fF/cell
Bus resistance : 9.3 Ω/cell

Provides both reduced voltage swing and pre-emphasis or full voltage swing

*J.C.Garcia, J.A.Montiel, S.Nooshabadi*
Adaptive Low/High Voltage Swing CMOS Driver for On-Chip Interconnects
*ISCAS 2007*

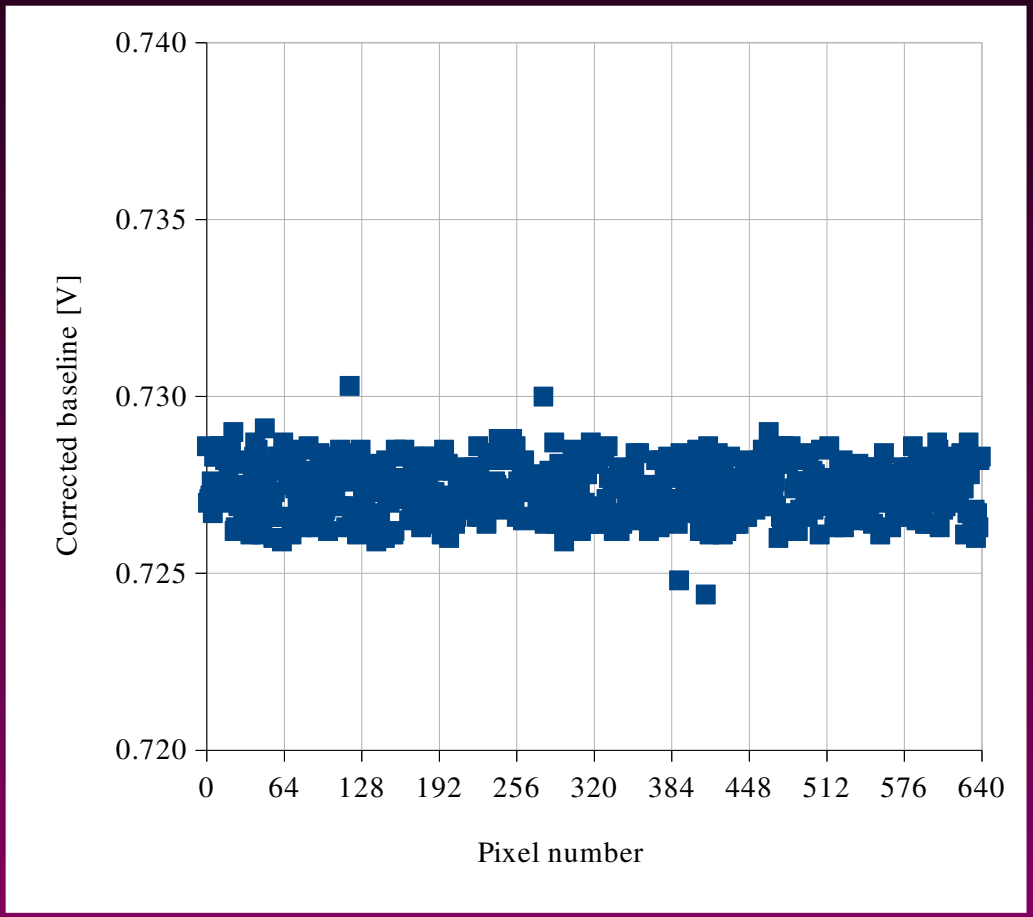
# On ToPiX data rates capabilities

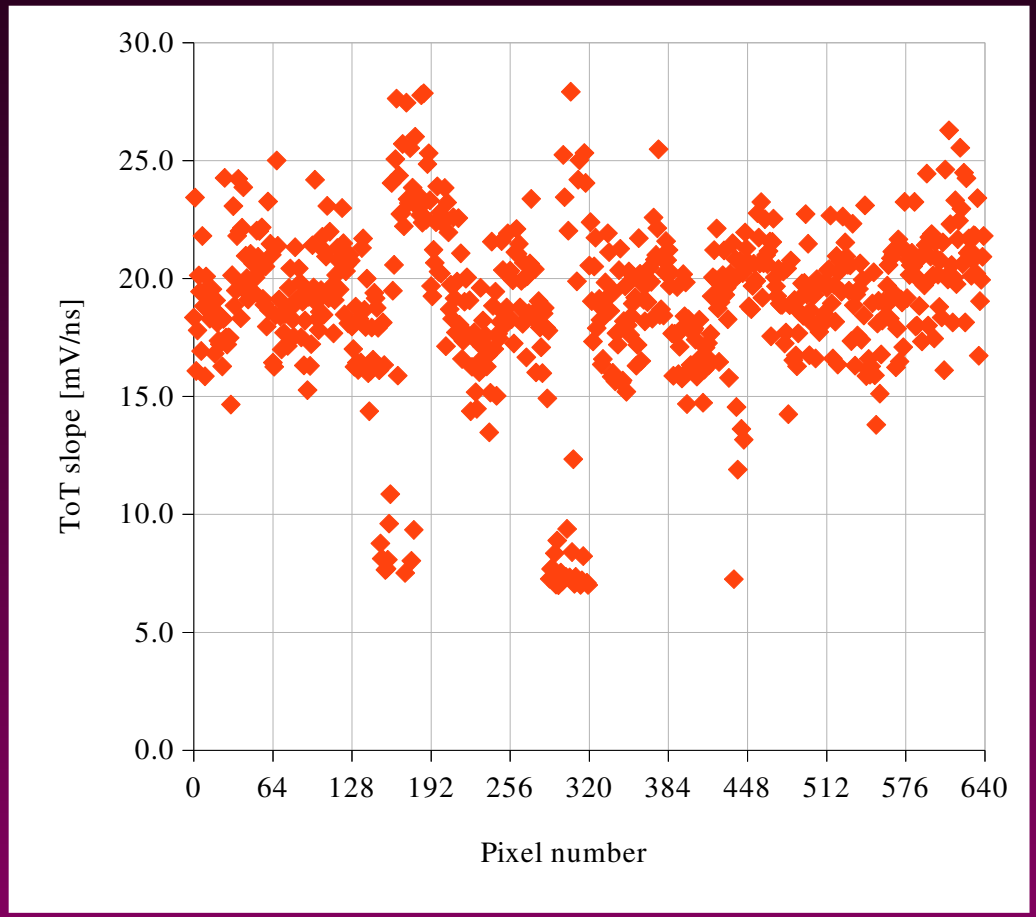
Sezione di Torino

| | # links | Clock freq. | Event size | Rate/chip (SDR) | Rate/chip (DDR) | # pixels | Rate/px (SDR) | Rate/px (DDR) | Rate/cm$^2$ (SDR) | Rate/cm$^2$ (DDR) |
|---|---|---|---|---|---|---|---|---|---|---|
| | | [MHz] | bits | Mev/s | Mev/s | | kev/s | kev/s | Mev/s | Mev/s |
| ToPiX v3 | 1 | 50 | 32 | 1.43 | - | 640 | 2.23 | - | 22.32 | - |
| ToPiX v4 | 1 | 50 | 40 | 1.11 | 2.22 | 640 | 1.74 | 3.47 | 17.36 | 34.72 |
| ToPiX v4 | 1 | 160 | 40 | 3.56 | 7.11 | 640 | 5.56 | 11.11 | 55.56 | 111.11 |
| ToPiX v5 | 1 | 160 | 40 | 4.0 | 8.0 | 12760 | 0.31 | 0.63 | 3.13 | 6.27 |
| ToPiX v5 | 2 | 160 | 40 | 8.0 | 16.0 | 12760 | 0.63 | 1.25 | 6.27 | 12.54 |
| ToPiX v5 | 3 | 160 | 40 | 12.0 | 24.0 | 12760 | 0.94 | 1.88 | 9.40 | 18.81 |
| ToPiX v5 | 4 | 160 | 40 | 16.0 | 32.0 | 12760 | 1.25 | 2.51 | 12.54 | 25.08 |

# Baseline & ToT

Sezione di Torino



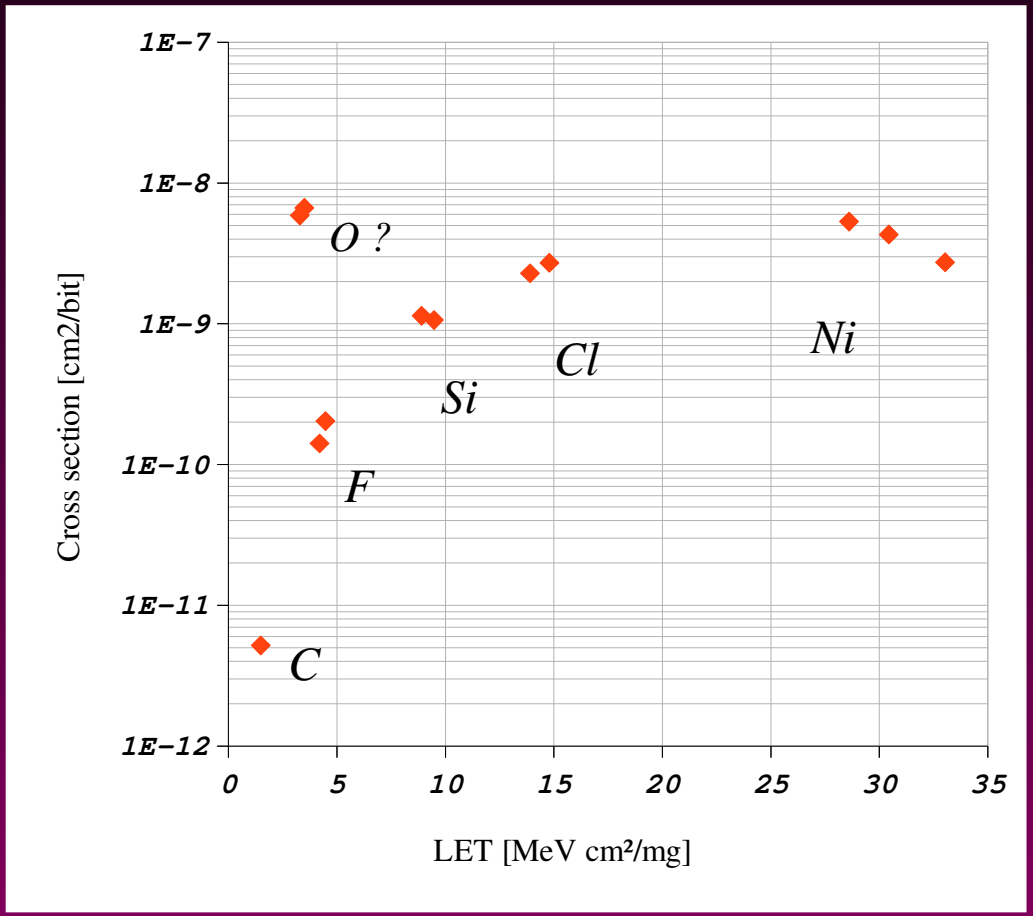



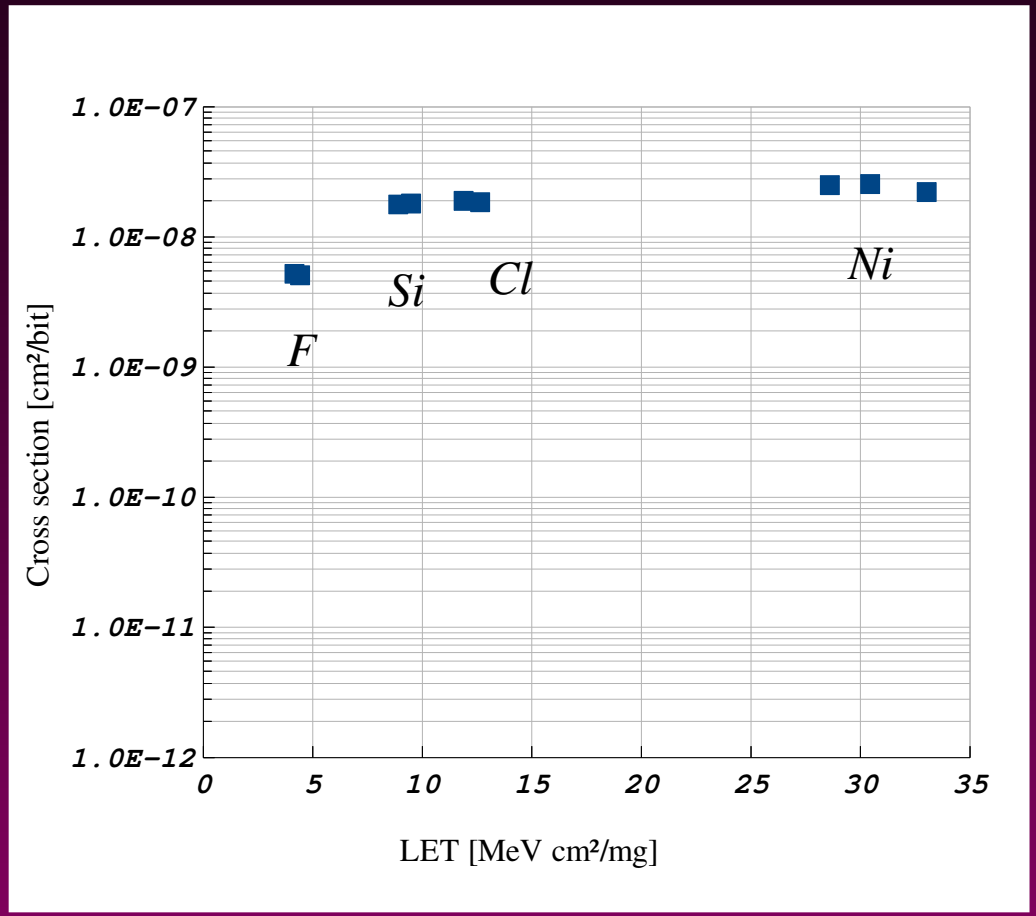

*Baseline average value : 727 mV*

*Baseline sigma : 0.73 mV*

# SEU test

Sezione di Torino




*Pixel configuration registers*

*Hamming-corrected errors*
*No uncorrected errors detected*