Status of GSI Microelectronics Developments

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Outline

APFEL

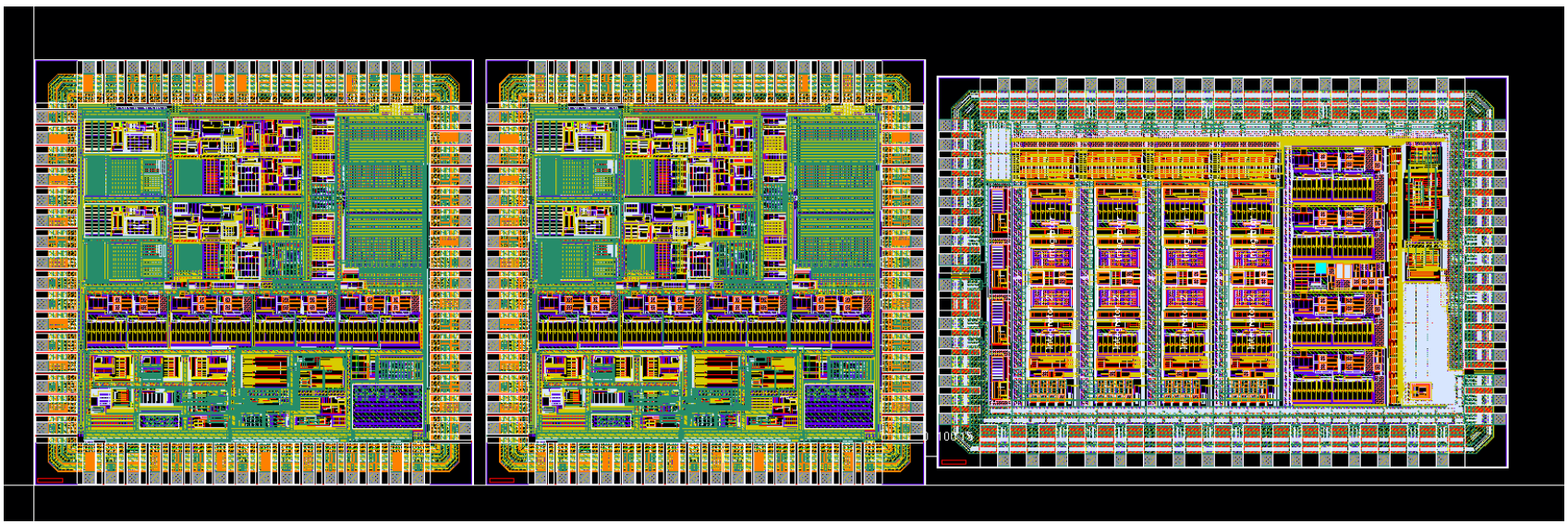
HitDetection
- ADC
- Pulse Transients
- HitDetection and other Experiments
- Schedule

Conclusion and Outlook

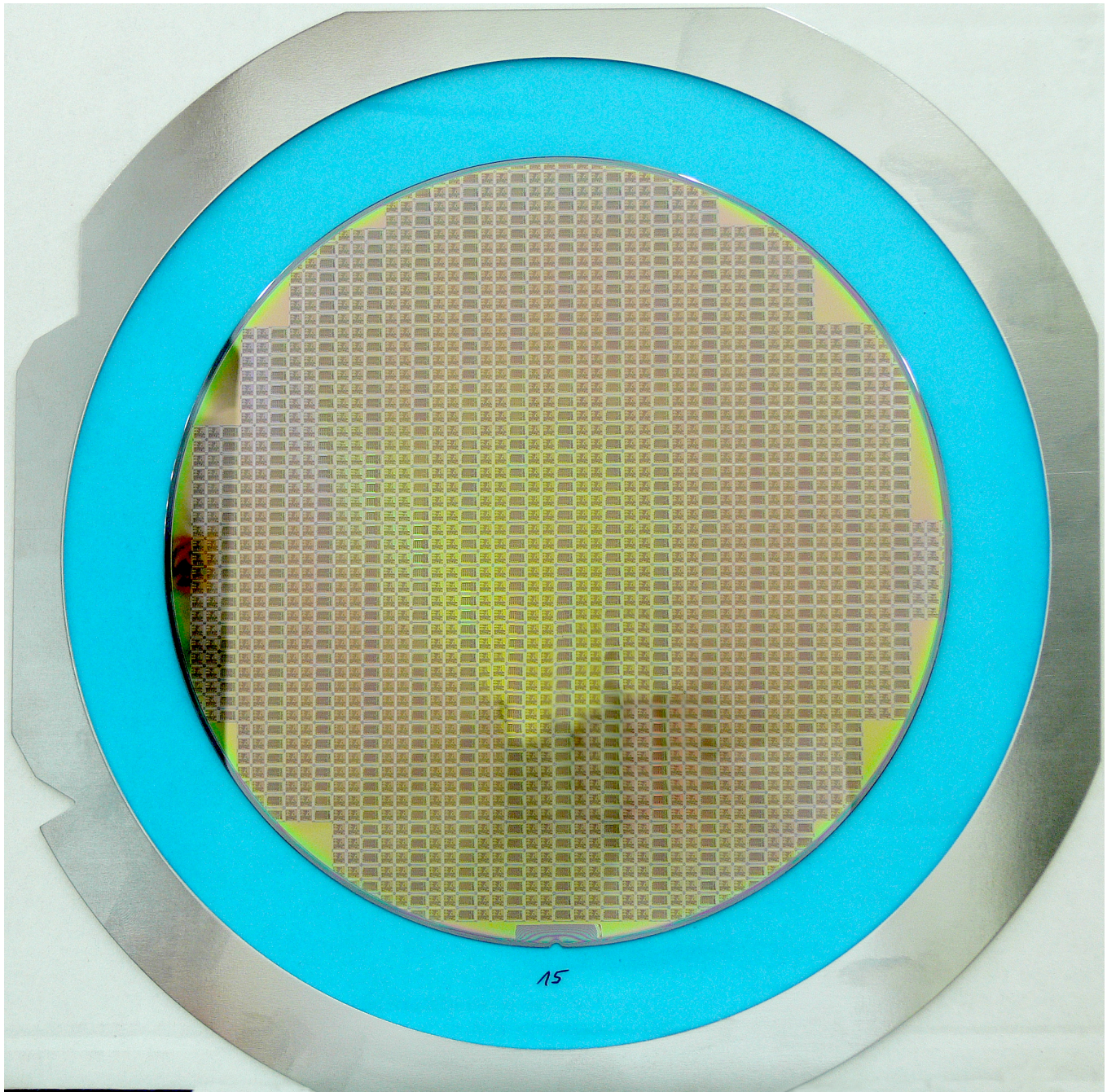
APFEL

APFEL

- 2015: Production of APFEL 1.5
- Common engineering run for APFEL and QFW2 @ Austria Microsystems
- 17994 APFEL chips are available
- Marginal note: Usage of APFEL for FAIR proton pilot beam diagnostics is under evaluation $\rightarrow$ +1283 chips packaged in QFN64



APFEL



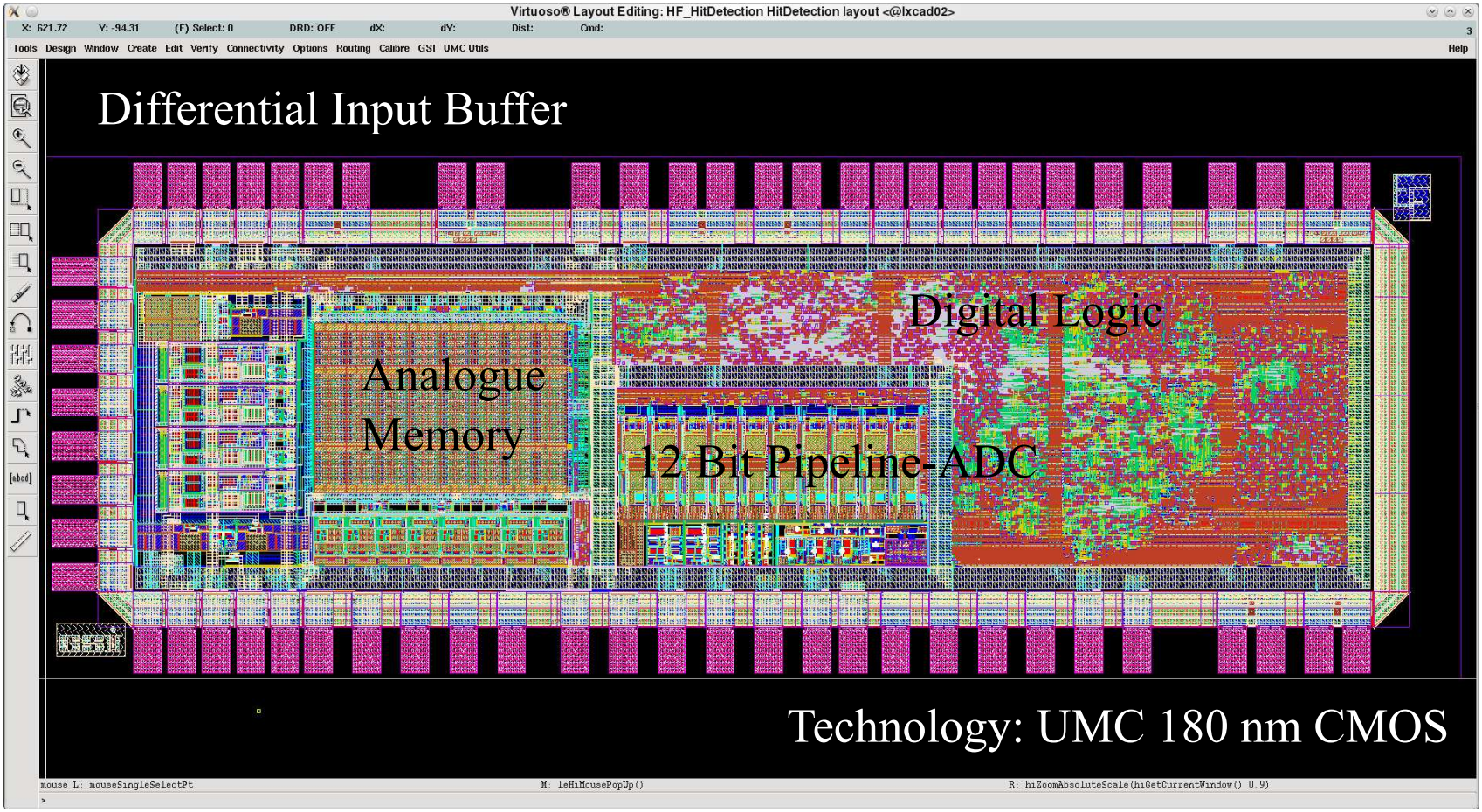
HitDetection

HitDetection ASIC

- HitDetection = Self triggered analogue transient recorder
- Motivation
  - Digitisation close to detector $\Rightarrow$ Reduction of pick up
  - Integration inside magnet
  - Reduction of needed connecting lines $\Rightarrow$ Cable cross section
  - Reduction of power consumption
  - Reduction of number of Components $\Rightarrow$ Higher reliability
- More Information:
  - https://wiki.gsi.de/foswiki/pub/EE/EEMeetVortragArch/HitDetEEMeeting1410.pdf (german)
  - ASIC manual in preparation ($\rightarrow$ h.flemming@gsi.de)

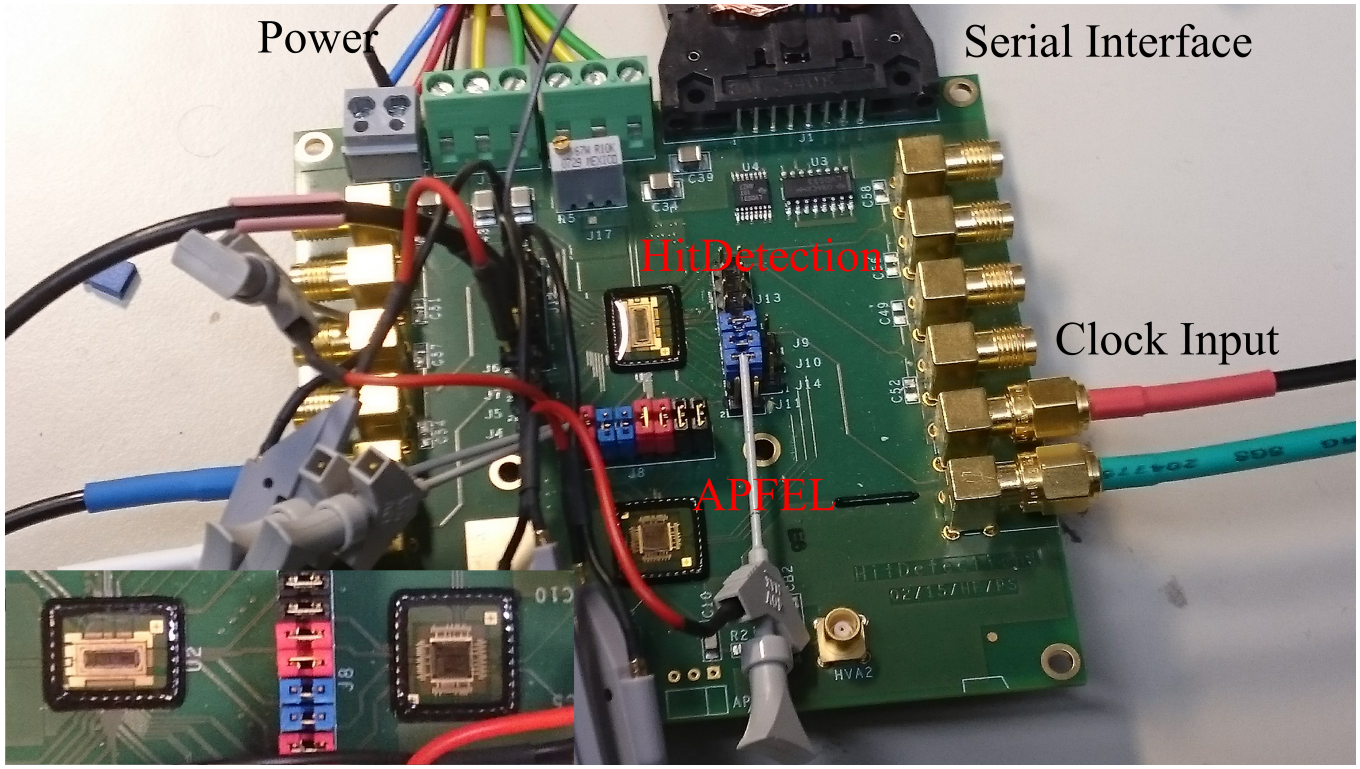
HitDetection ASIC

- Tape out end of 2014



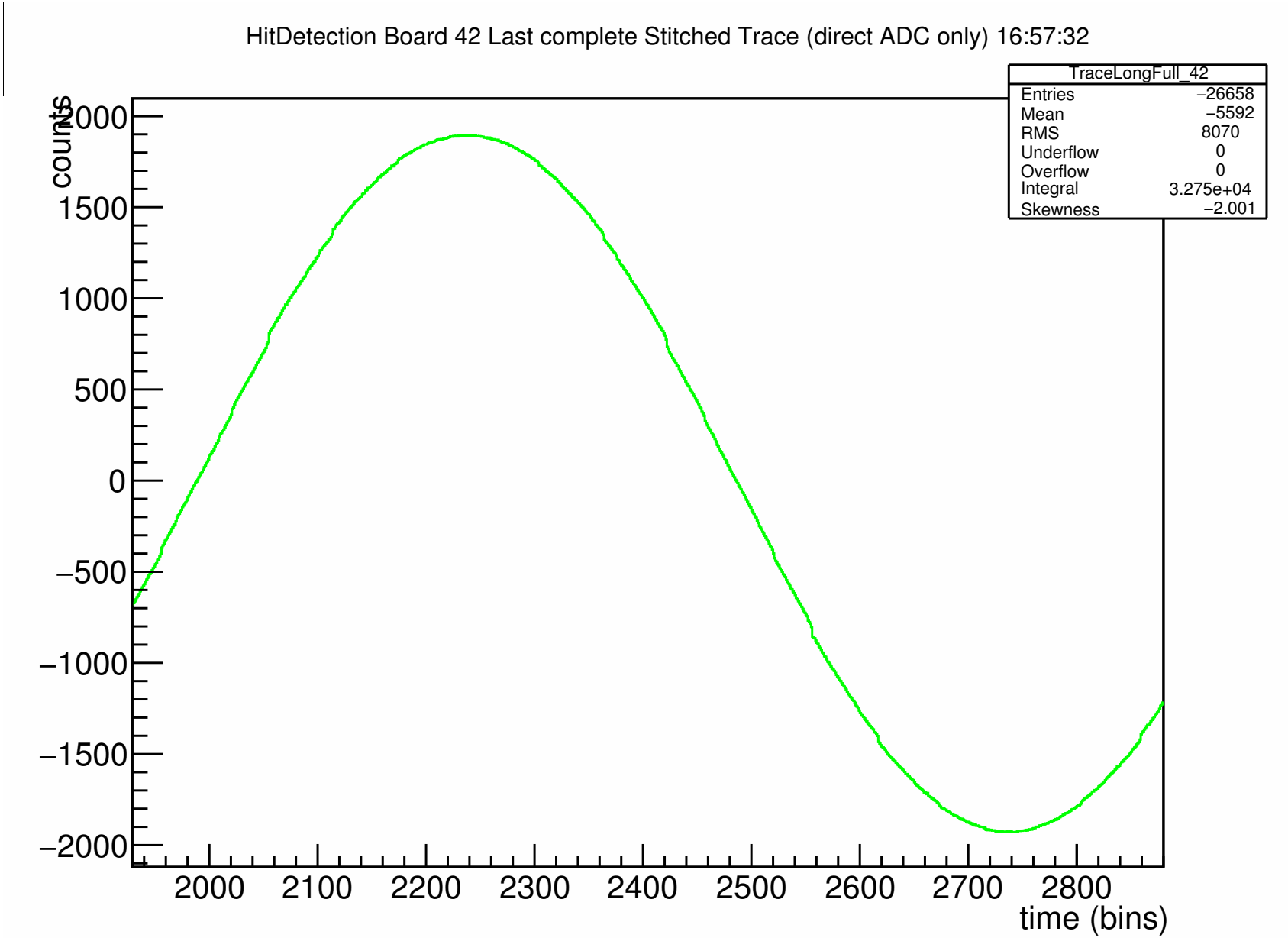
HitDetection ASIC

- Test setup : HitDetection V10 and APFEL ASIC as signal source
- DAQ interface: Vulom (VME based multi purpose FPGA board)
- DAQ and Analysis: MBS and Go4



ADC Tests

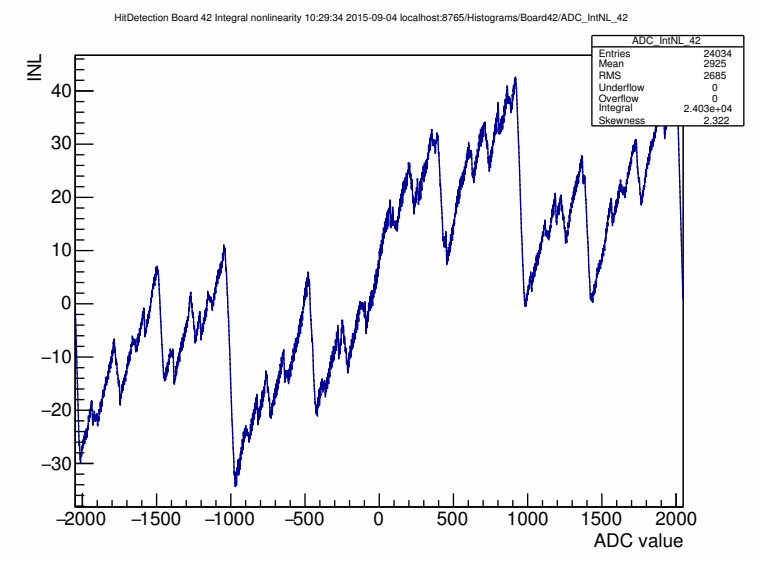
Test of on chip 12 Bit Pipeline ADC



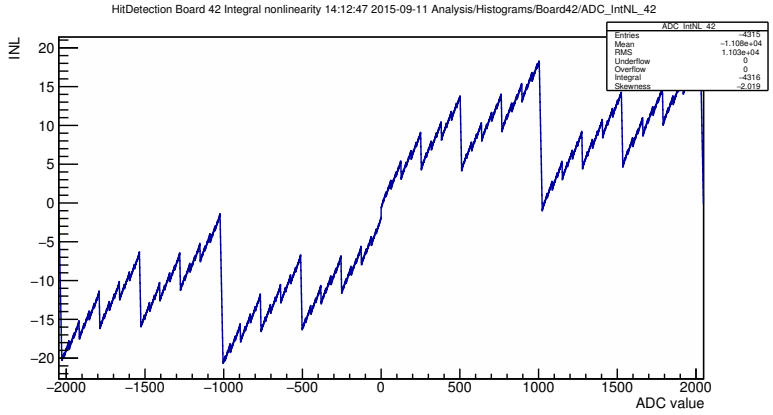
ADC-Tests

Integrated Non Linearity of ADC

Measured integral non linearity fits to simulation of Pipeline ADC with limited open loop gain in MDAC-OTA



Measured INL of HitDetection ADC

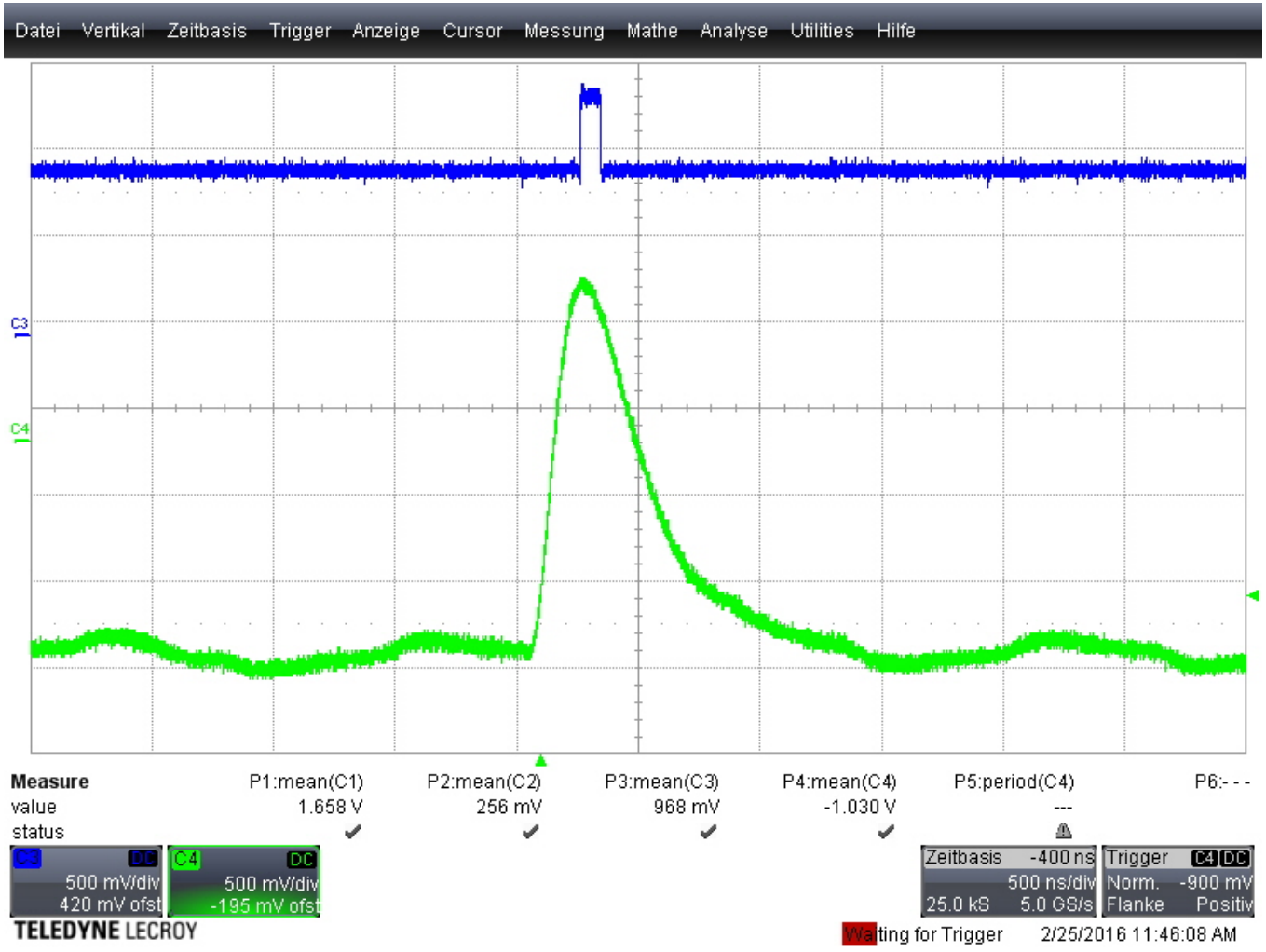


INL of simulated ADC

Pulse Transients

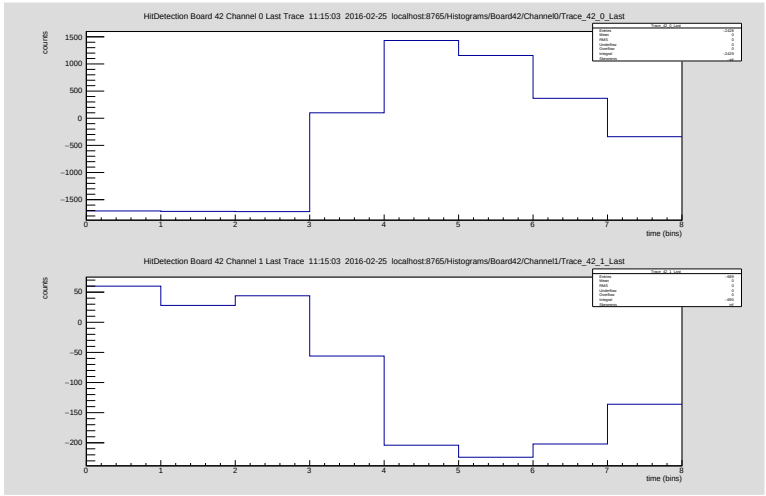
Signal Source

Using APFEL ASIC test pulse generator as signal source

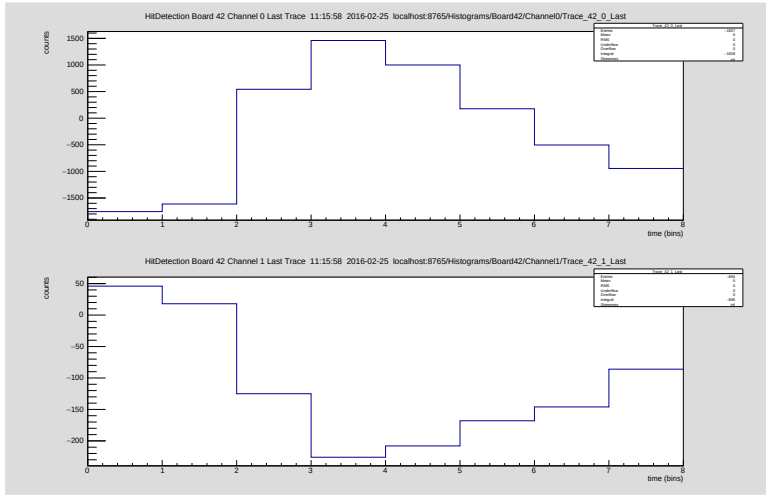


Pulse Transients

- Analogue recording of 8, 16 or 32 samples
- On chip digitisation with 12 bit ADC
- Sampling rate up to 100 MS/s (here: 10 MS/s)
- Configurable trigger delay
- Here: Channel 0: high amplification, Channel 1: low amplification

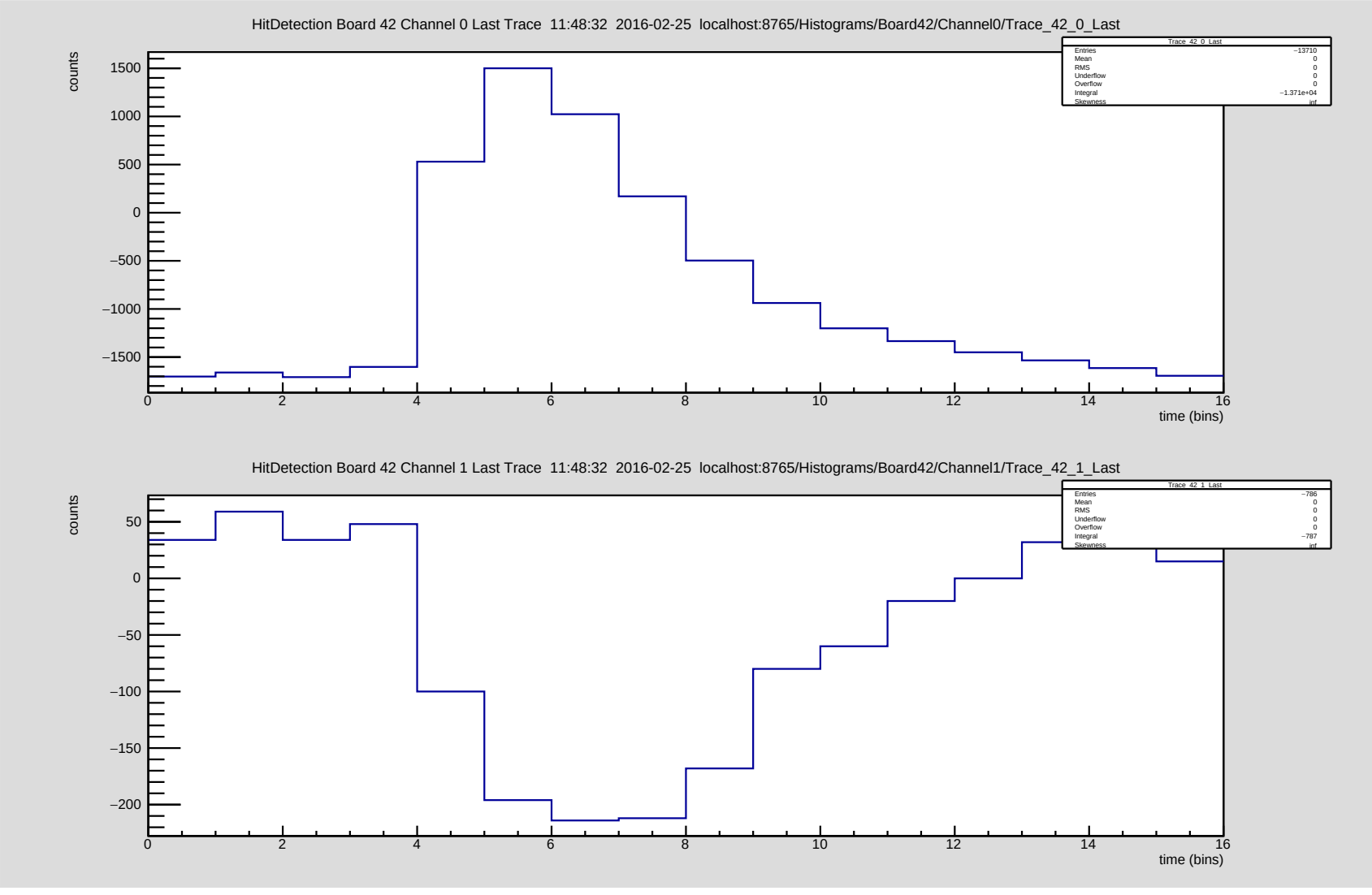


8 sample mode, 4 samples trigger delay



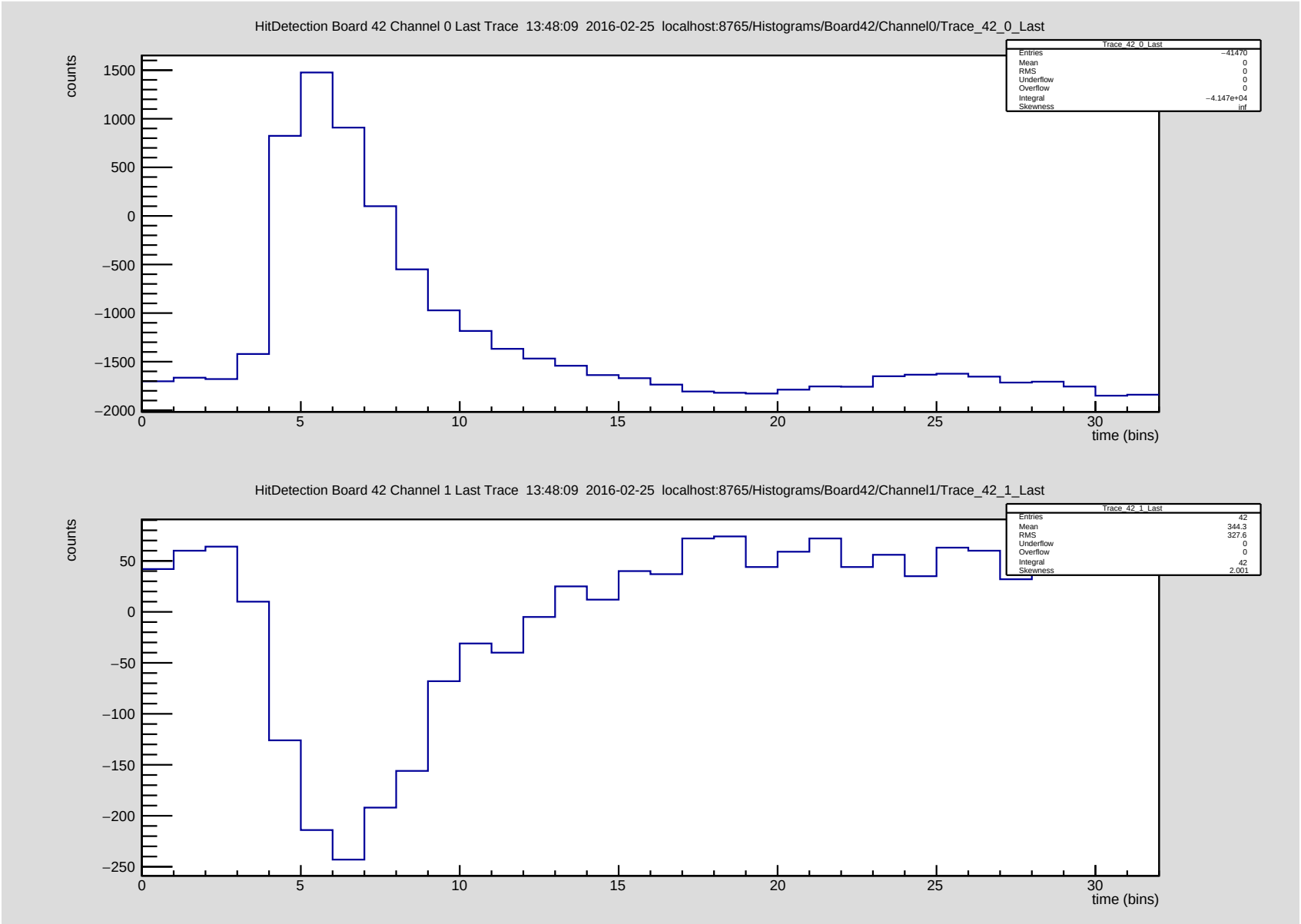
8 sample mode, 2 samples trigger delay

Pulse Transients



16 sample mode

Pulse Transients

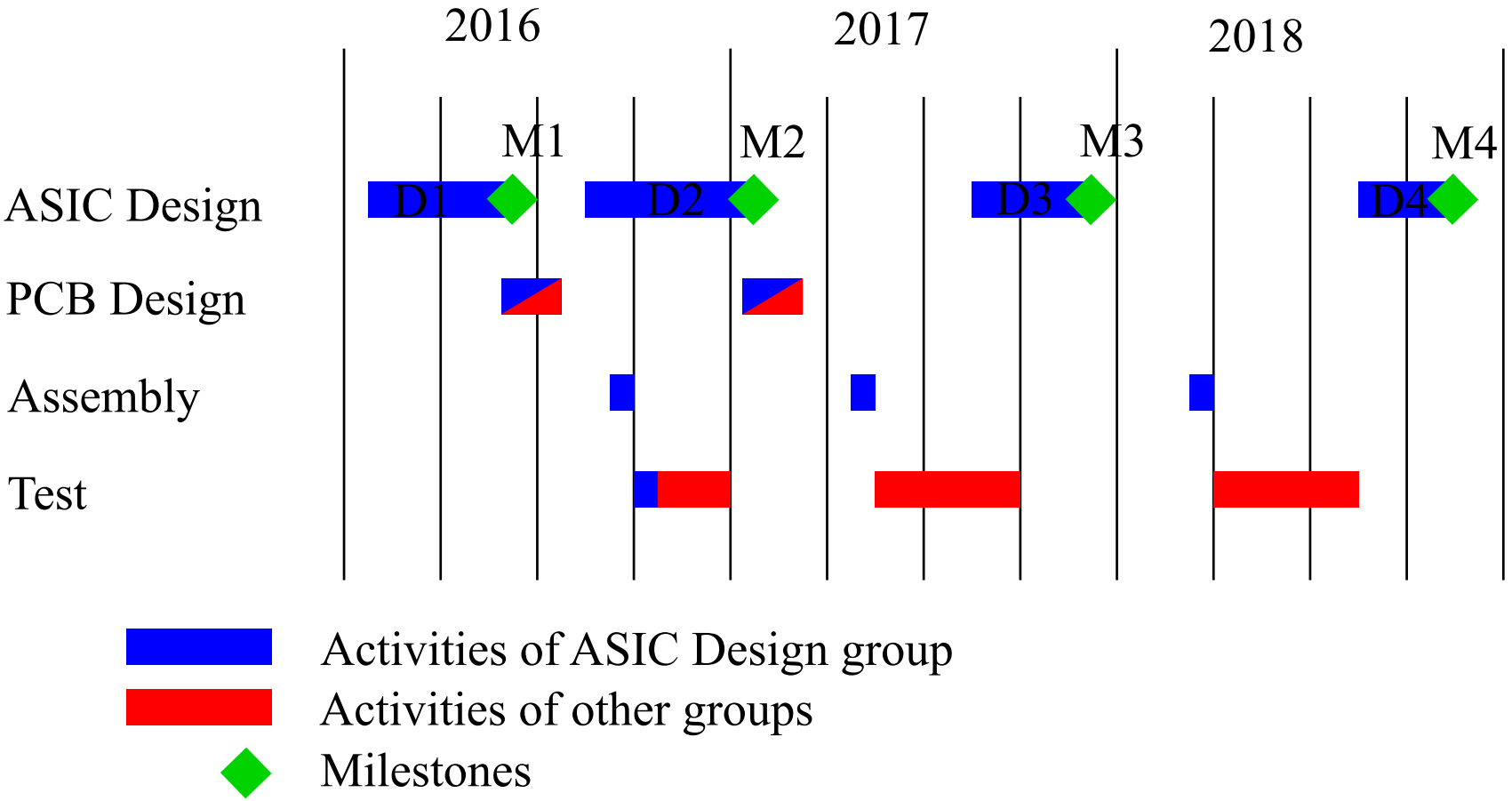


32 sample mode

HitDetection and other Experiments

- GEM-TPC at Super Fragment Separator @ FAIR
  - Currently read out is based on nXYter ASIC
    originally designed for neutron detectors at Uni HD and AGH Cracow
  - But: nXYter has a slew of drawbacks, e.g. insufficient dynamic range, power consumptions, radiation hardness...
    $\Rightarrow$ Question of a replacement raised up
  - Our proposal: Using the HitDetection architecture and replacing the input buffer by a charge sensitive Preamplifier
  - Would be also useful for PANDA GEM Forward tracker

Schedule



M1: 2nd 4 channel prototype, M2: 1st 32 channel prototype,
M3: 2nd 32 channel prototype, M4: final design

Conclusion and Outlook

- APFEL
  - Approx 18000 Chips are delivered and ready for use
- HitDetection
  - HitDetection Prototype is fully operational
  - Strong non linearities observed at Pipeline-ADC $\Rightarrow$ Problem of the used OTA
  - Self triggered transient recorder is working. Detailed investigations are ongoing
  - Strong interest in HitDetection architecture by other experiments (e.g. SFRS)
  - Next Steps:
    - Redesign of the Pipeline-ADC
    - Design of a CSA for GEM readout
    - Common tape out in May
    - Test with PWO crystal / Proto120?

Thank you