ALICE Read-out Upgarde for Run3
(CRU Project)

and

Alternative Solutions

Presentation of the DAQ group of the
Institute of Particle and Nuclear Physics
of the
Wigner Research Center for Physics

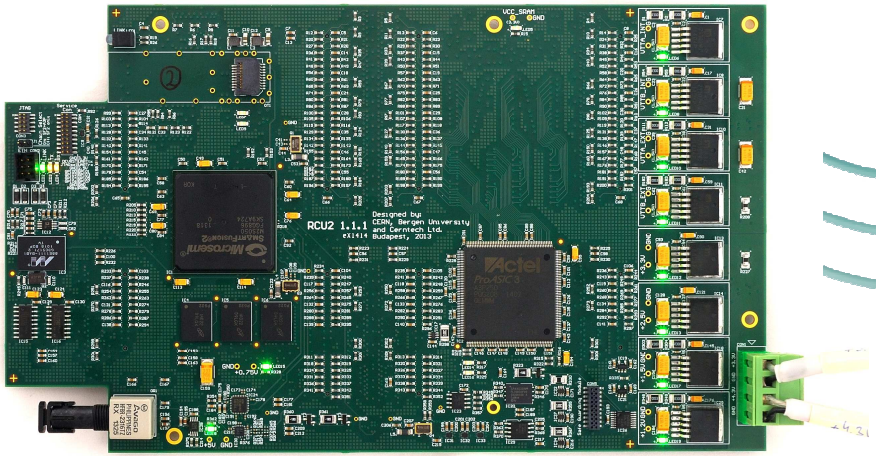
T. Kiss, E. David
IPNP, Wigner RCP

Present (Run2) ALICE Read-out System

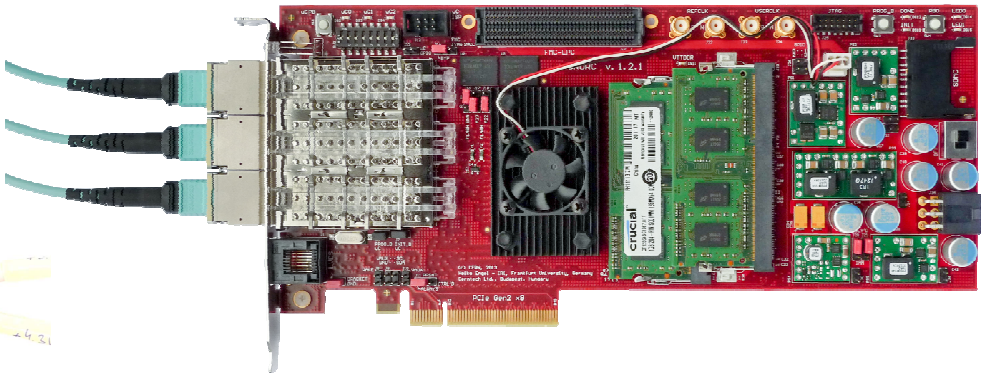
1. During LS1, the TPC Detector Read-out Consolidation Project had been decided.

The Read-out Concentrator Units (RCU) were completely re-designed → RCU2

- **Instead of having 3 different FPGAs, we now have only one, radiation tolerant, system-on-chip FPGA**
- **Splitting up of the two front-end branches to four → more parallel read-out**
- **Increasing the DDL speed to 4.25 Gb/s (→ DDL2).**
- **A new Read-out Receiver Card, the C-RORC reads out these DDL2 links**
  - **„C"ommon receiver card for DAQ and HLT farms**

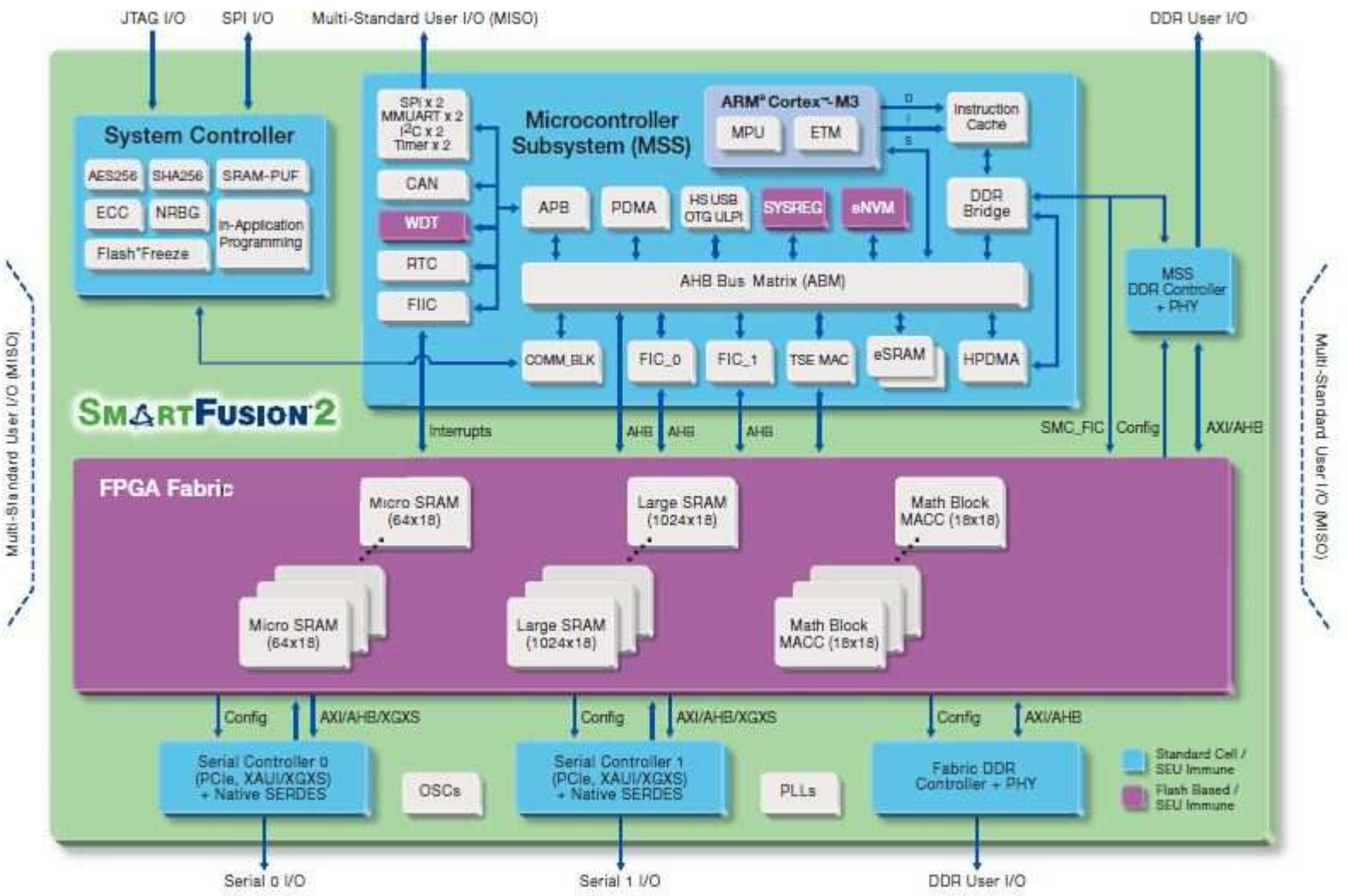


RCU2



C-RORC

RCU2: SmartFusion2 SoC FPGA

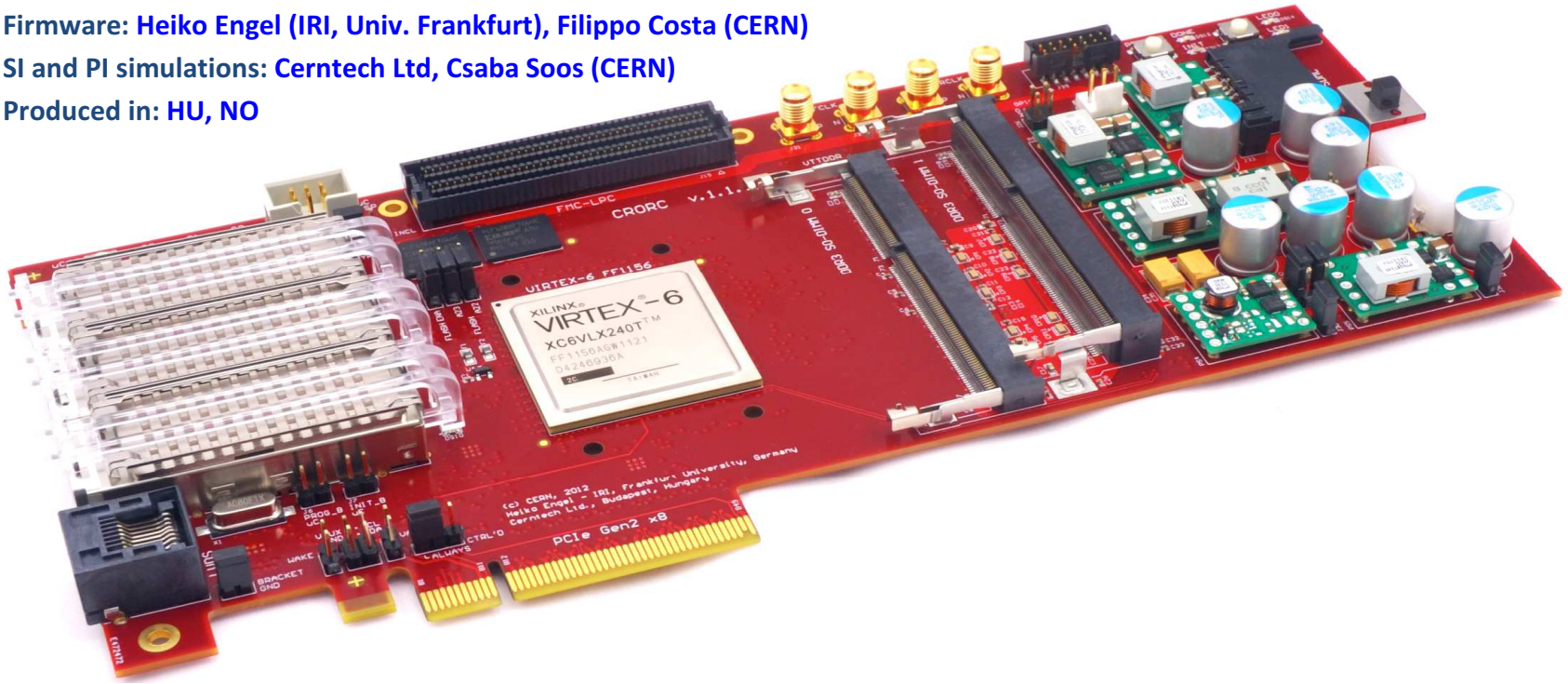


- **2 SERDES interface: 4 lanes /each**
- **SERDES interface working modes: XAUI, Gen2 PCI Express end-point, Custom modes**

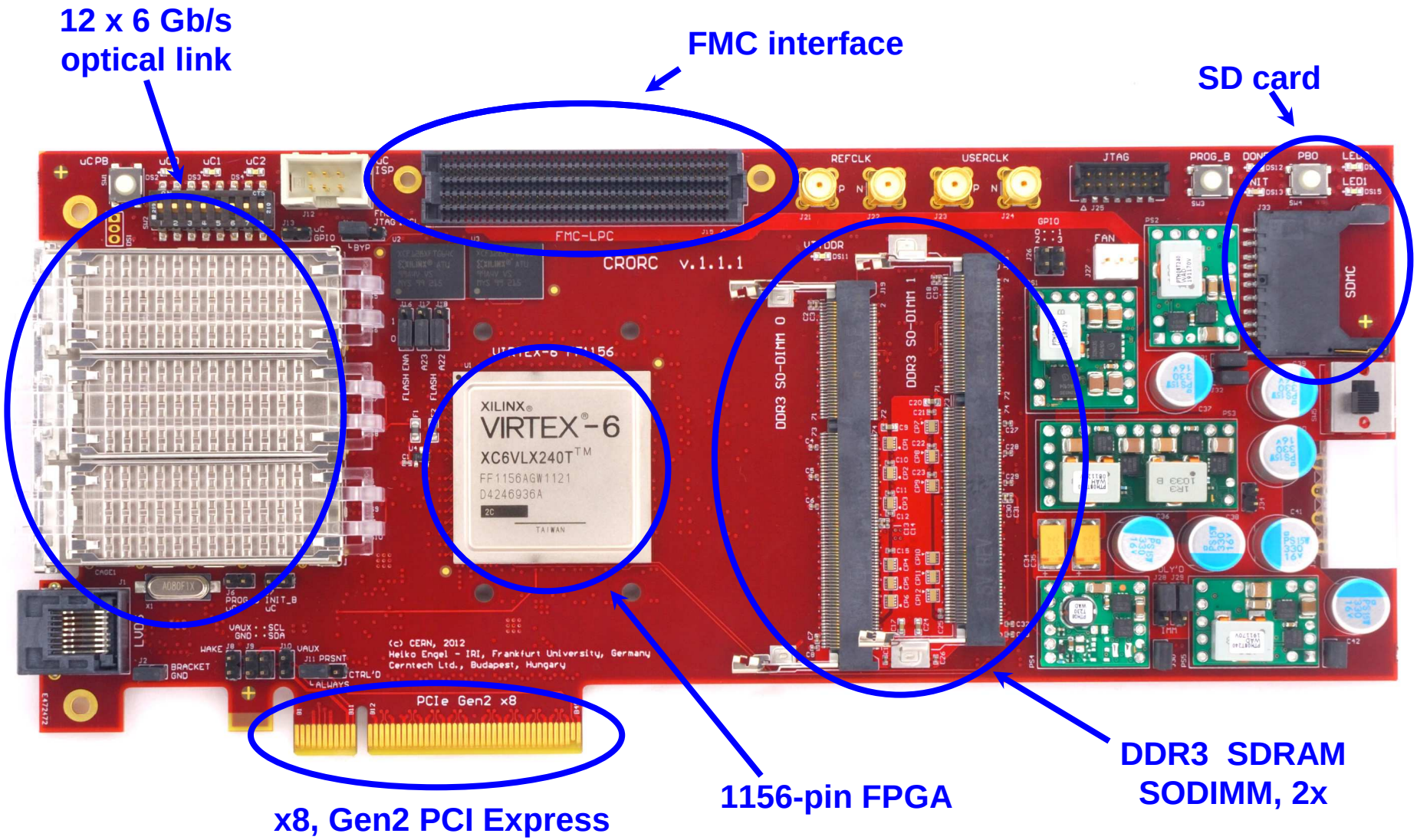
Present Read-out Receiver Card for ALICE DAQ and HLT … also used by ATLAS

- **For LHC Run2, FE Read-out Cards with new, 4.25 Gb/s ALICE Detector Data Link (DDL2) had been developed. This required a new PCI Express read-out receiver (RORC) card, too.**
- **The new common read-out receiver card called (C-RORC) for the DAQ and HLT farms was developed by Frankfurt University, CERN, and Cerntech Ltd.**

- **Conceptual design: CERN DAQ&HLT teams, Heiko Engel (IRI, University of Frankfurt)**
- **Schematics: Heiko Engel (IRI, UNiversity of frankfurt)**
- **PCB design: Cerntech Ltd. (Budapest)**
- **Firmware: Heiko Engel (IRI, Univ. Frankfurt), Filippo Costa (CERN)**
- **SI and PI simulations: Cerntech Ltd, Csaba Soos (CERN)**
- **Produced in: HU, NO**



C-RORC


12 x 6 Gb/s optical link
FMC interface
SD card
FMC-LPC
CRORC v.1.1.1
XILINX
VIRTEX-6
XC6VLX240T
FF1156AGW1121
DDR3 SO-DIMM 0
DDR3 SO-DIMM 1
SDHC
PCIe Gen2 x8
x8, Gen2 PCI Express
1156-pin FPGA
DDR3 SDRAM SODIMM, 2x

ALICE Read-out Upgrade Plans - LHC Run3

- the CRU Project -

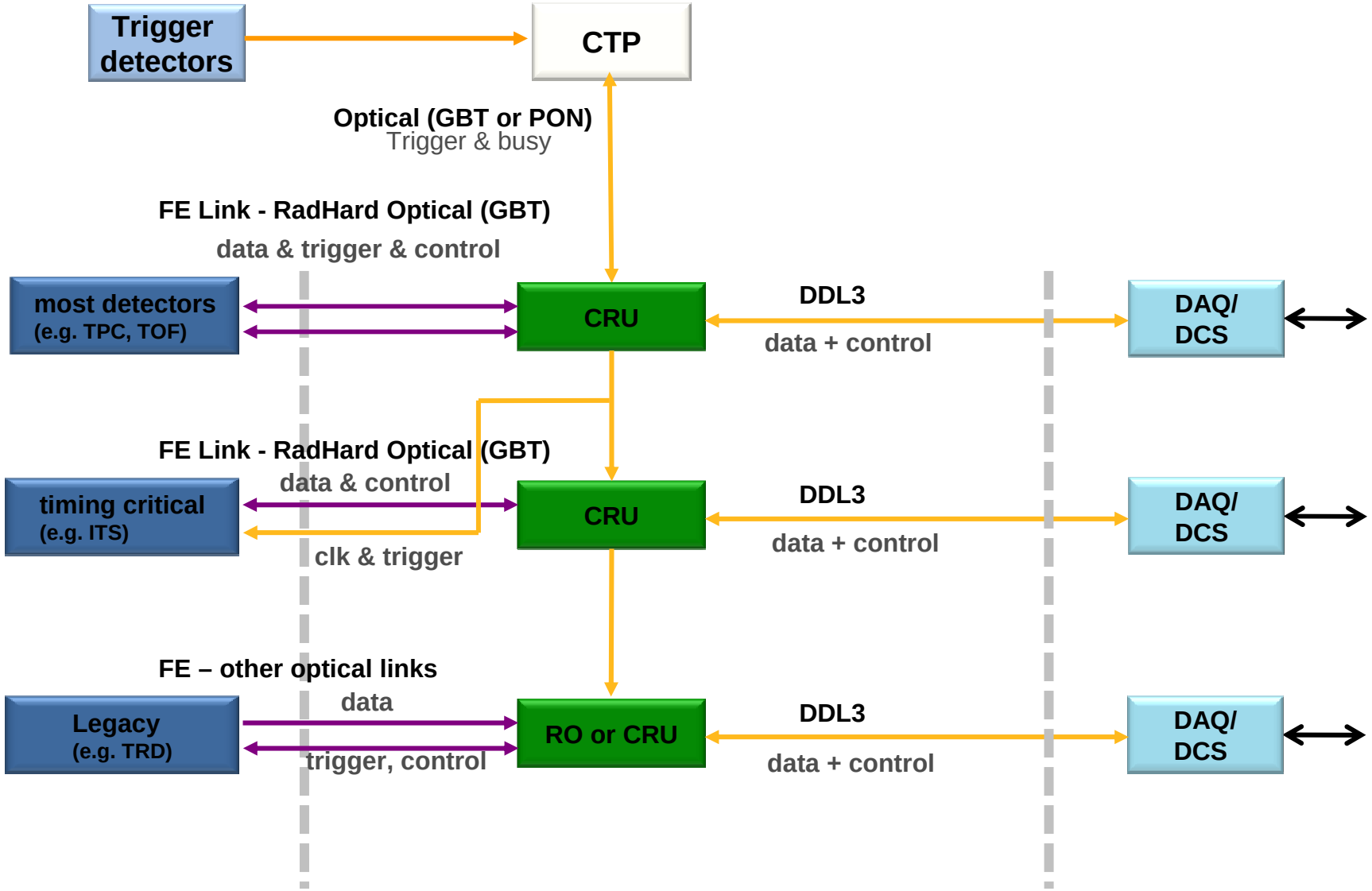
Main points of the *system requirements* for the Upgare for LHC Run3

- **Concentrating of data, multiplexing of links – reduce the number of the DAQ computers needed**
- **Integrating Data, Control, and whereever it is possible, Trigger and Timing links into one physical links**
- **Provide a single interface between the common DAQ and the subdetectors (as before)**

There is a need for a new *Common Read-out Unit* (CRU)

- **As a link multiplexer (for FE cards with local FPGAs)**
  - **these FE cards can send formated data packets**
- **As a remote read-out controller for FE cards with read-out ASICs (ADCs) only**
  - **receiving raw data, typically with continuous read-out**

CRUs in ALICE Read-out



ALICE DAQ Upgrade Plans - LHC Run3

- the CRU Project -

Two technical options were investigated:

- A) CRUs in the cavern, close to the detectors (radiation)
  - Flash memory based FPGA (e.g. Microsemi SmartFusion2 (SF2)
  - Custom hardware development
- B) CRUs in the counting rooms, far from the detectors (no radiation)
  - More powerful SRAM based FPGA (Altera or Xilinx)
  - First idea was the TELL40/AMC40 system developed by CERN LHCb

- ALICE chose Case B) and co-operates with LHCb to use a common hardware
  - LHCb changed the form factor to PCI Express: AMC40 →PCIe40
  - ALICE contributes to the CRU hardware testing and verification
  - The ALICE CRU project became mainly a FW project

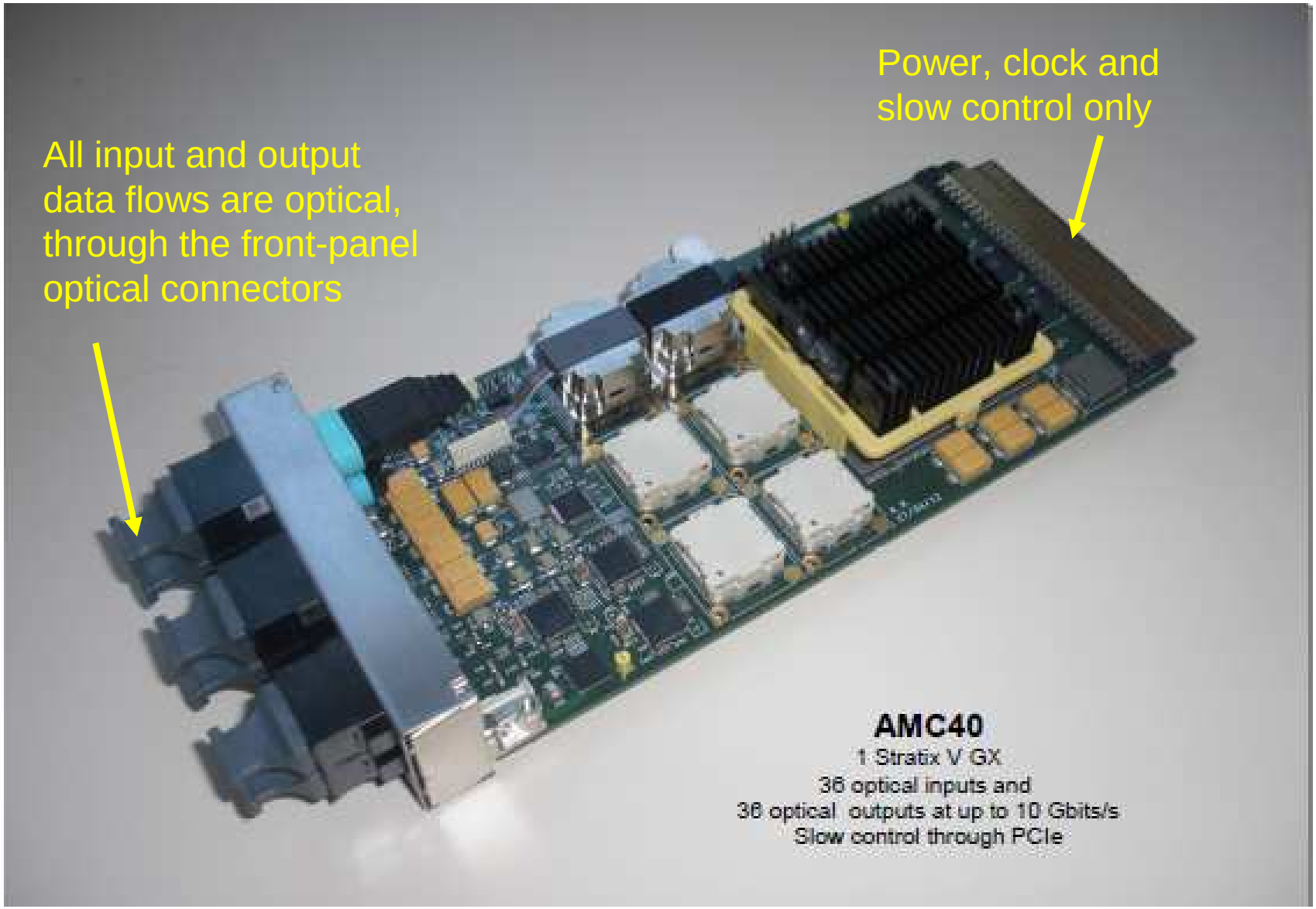
ALICE DAQ Upgrade Plans - LHC Run3

- the CRU Project -

All CRUs are connected to the Trigger and Timimg System (TTS) and to the Detector Control System (DCS)

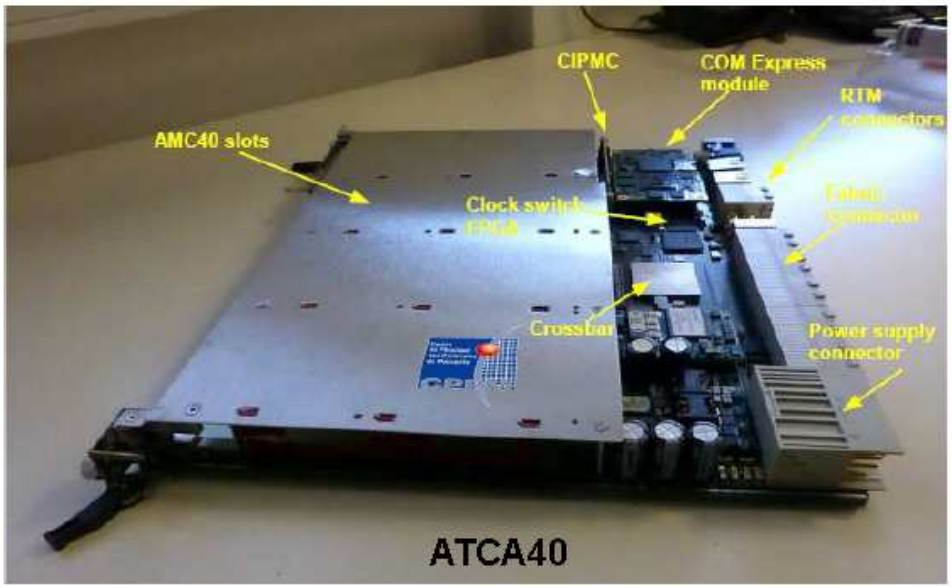
- **CRUs are aware of all trigger information (heartbeat or trigger, event IDs, etc.)**
- **CRUs perform the final packetizing and formatting of data streams writing data to the First Level Processing nodes (FLP computers) in the standard ALICE data format. (Common for all subdetectors.)**
- **DAQ and CRU must always be on to have control access to the detector FE.**
- **CRU firmware is divided into a common layer (physical interafces, common features) developed by a central team, and a user logic handling the detector specific features (developbed by the detector teams)**

AMC40 Mezzanine Board

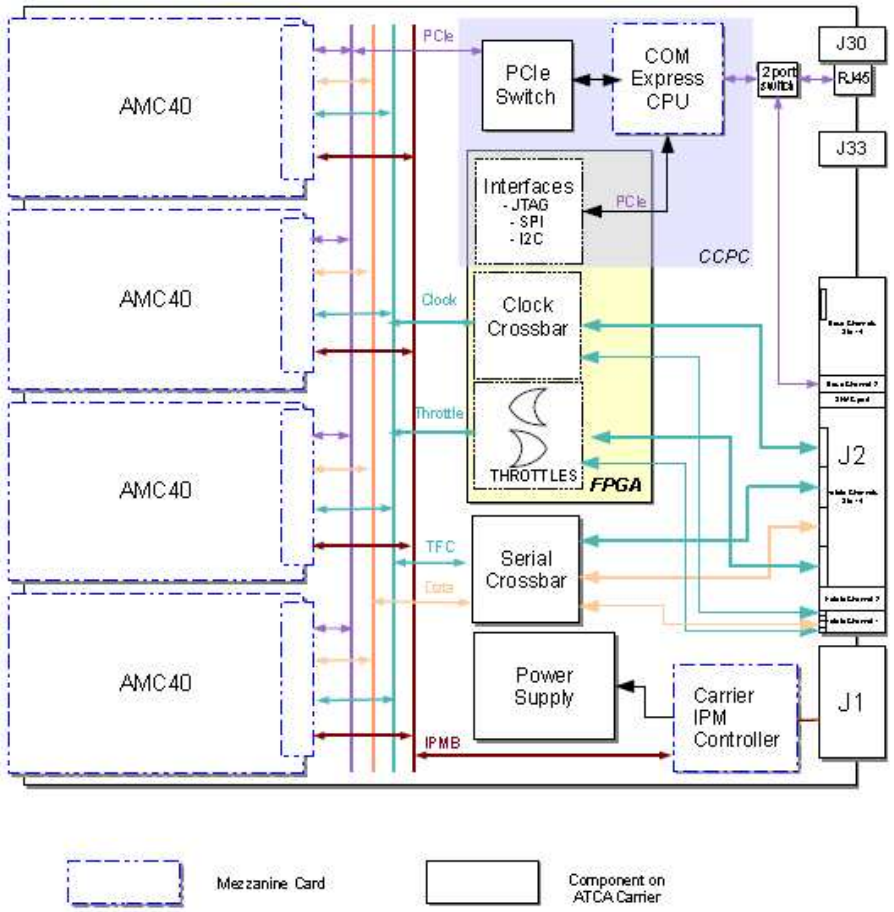


CRU - Case B) Using the LHCb System

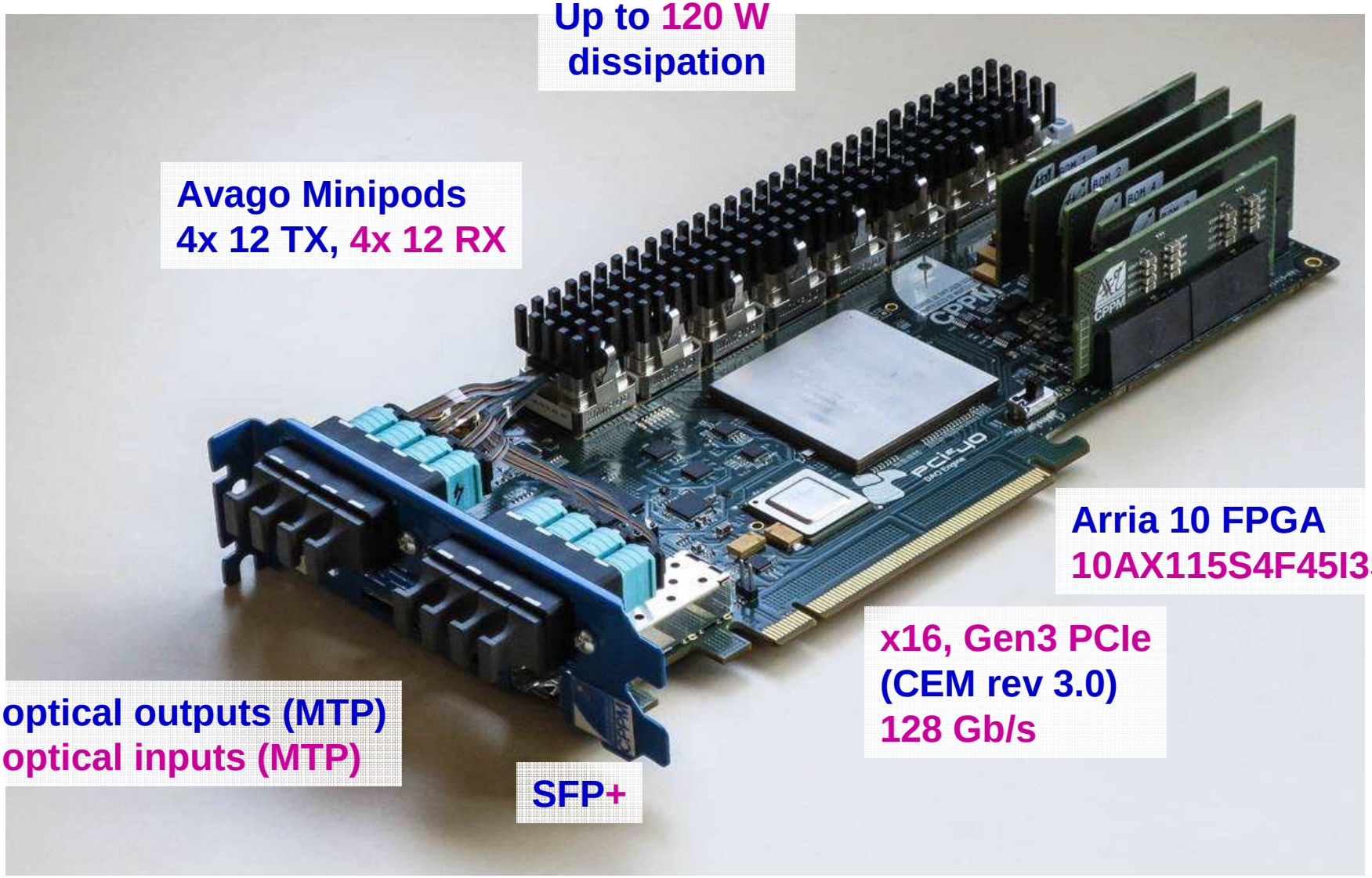
**If the CRUs will be placed in the counting rooms, (no radiation,)
we can use the LHCb ATCA40/AMC40 system as a hardware platform**



ATCA40 carrier board and AMC40 modules have been developed for LHCb in CPPM, Marseille

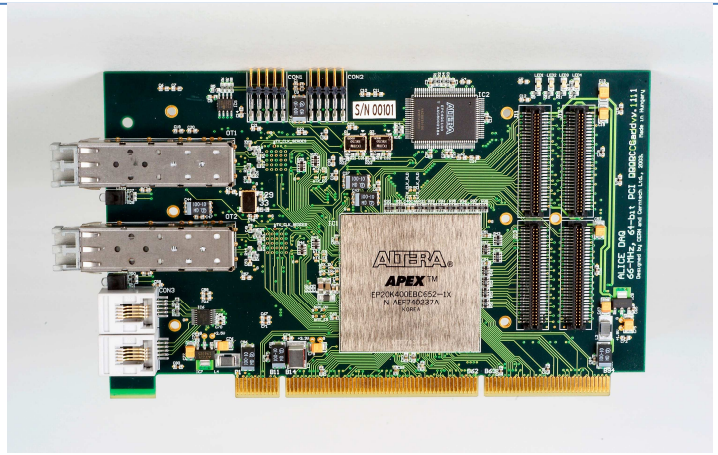


PCIe40 Card of LHCb

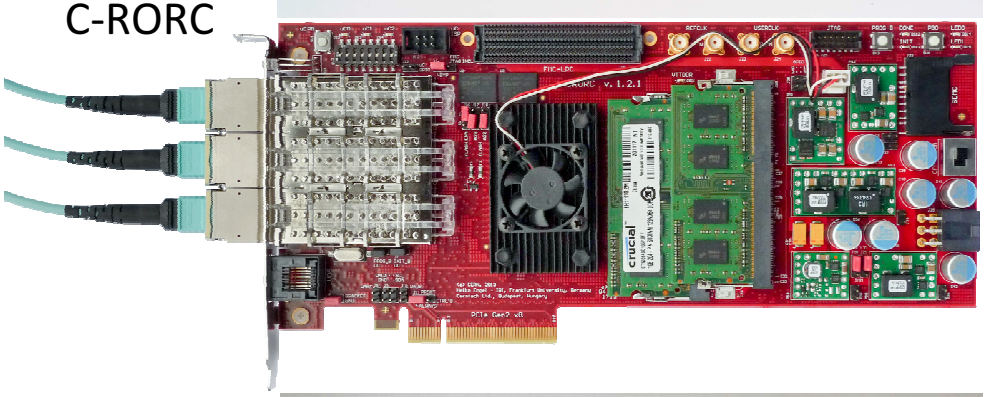


Evolution of the ALICE Data Link Receiver Cards

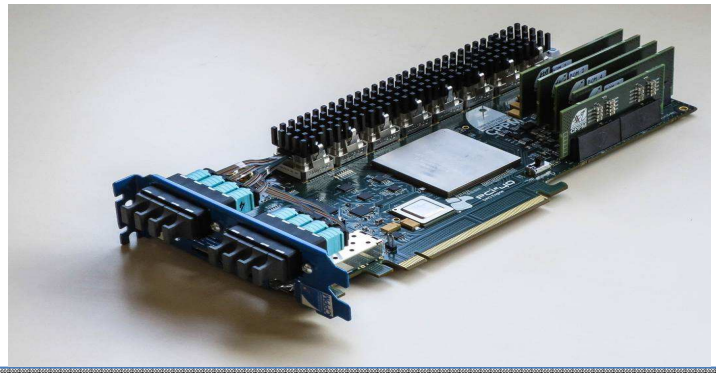
D-RORC



C-RORC



PCIe40
(LHCb)



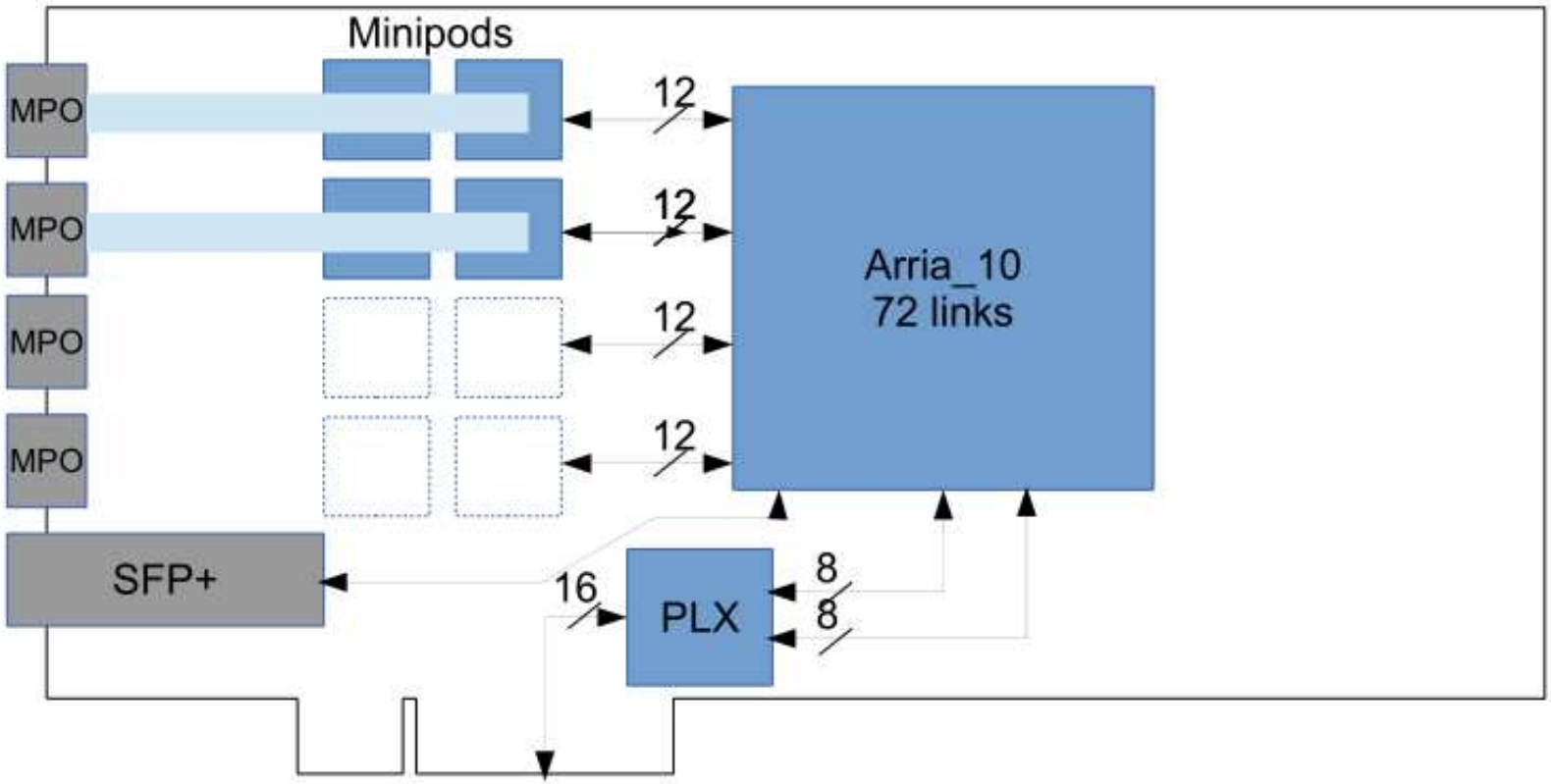
- **Standardised detector data links (DDL) as the common interface between the detectors read-out and the DAQ (online system)**

- Run1:
- **2.125 Gb/s custom DDL & D-RORC**
- **x4, Gen1 PCIE**

- Run2:
- **4.25 Gb/s custom DDL2 & C-RORC**
- **x8, Gen2 PCIE**

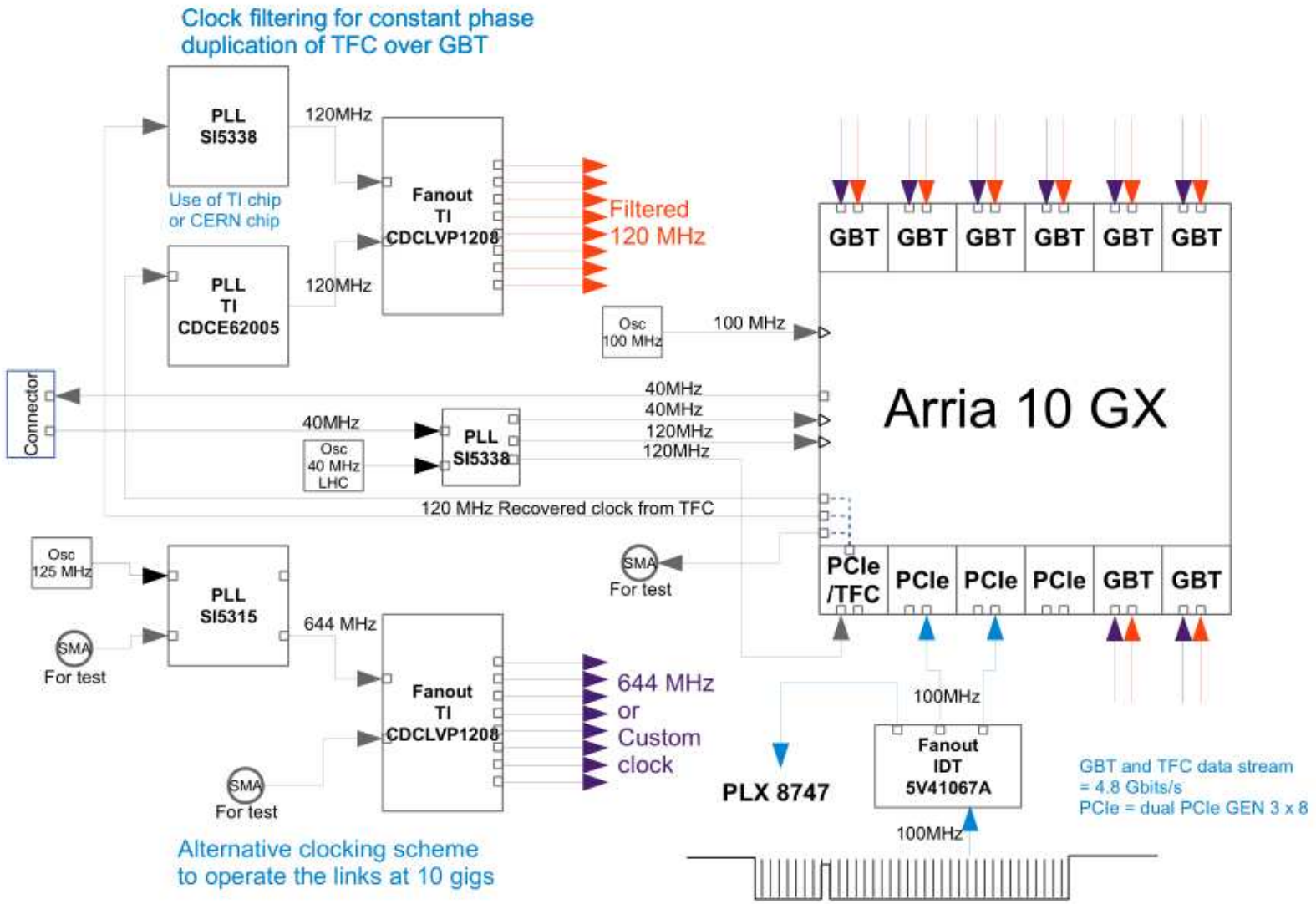
- Run3:
- **4.8 Gb/s GBT and CRU (PCIe40)**
- **x16, Gen3 PCIE**

Block diagram of the PCIe40



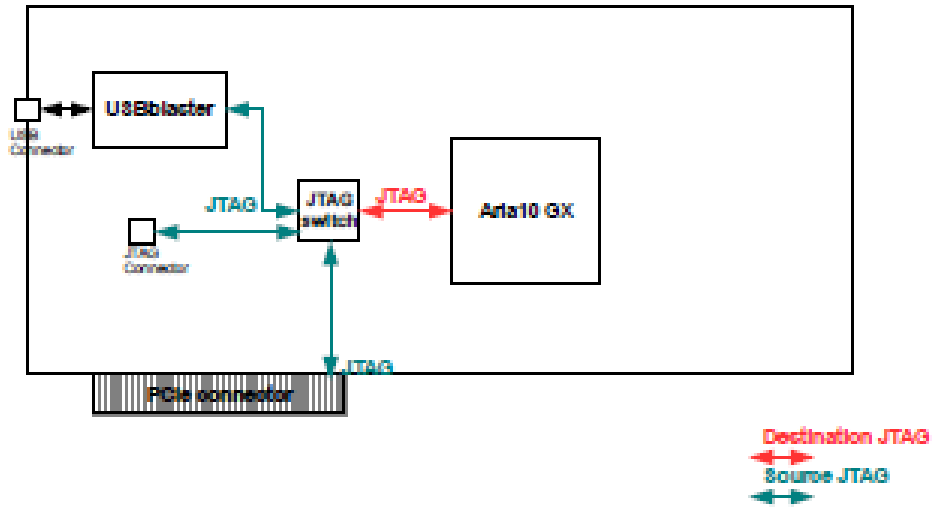
PCIe40_Specification_Draft0, rev1, LHCb Technical Note

PCIe40 Clock Paths



PCIe40_Specification_Draft0, rev1, LHCb Technical Note

Configuration options



- **JTAG programming through JTAG connectors**
- **On-board USB blaster**
- **Remote configuration from SW through the PCIe interface with CvP protocol**

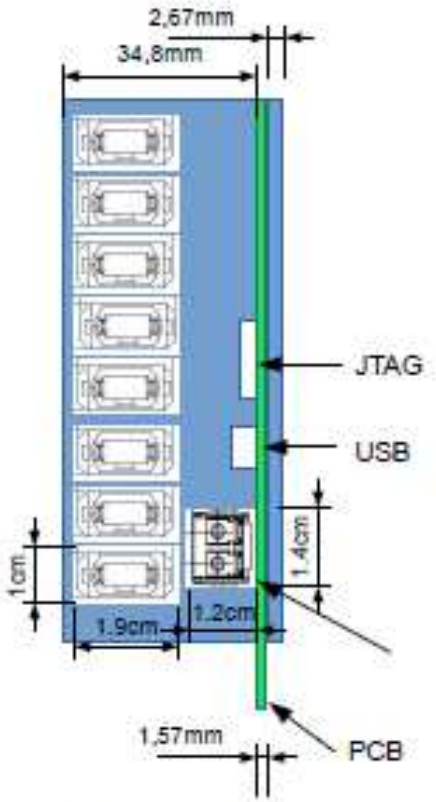


Figure 12: Face plate

PCIe40_Specification_Draft0, rev1, LHCb Technical Note

Installation, Power and Cooling

- Dual Slot card with Standard Height
- PCIe auxiliary power supply cable with 2x4 pin connector
- Dissipation up to 120 W
- Proper cooling is neeed (to be finalized)
- Airflow of 2 m/s is required

Recommended Servers

- Developers strongly recommend to use a well tested, proven server machine for all users
- Recommended server: ASUS

PCIe40_Specification_Draft0, rev1, LHCb Technical Note

Alternative Read-out Soultions

- In most collaborations there is a strong interest in minimizing the use of custom hardware and custom protocols
- There are 1 GbE data acquisition systems. Usually they are small scale ones and there are now high sustainable performance requirements
- GbE read-out systems have been earlier investigated in ALICE, too. (A 1GbE pilot project.)
- Wigner RCP is interested in R&D in this field, collaborating with possible future users. Aim:
  - 10 GbE based links from detectors, all commercial HW
  - Mid or large scale system with optimized, high sustainable perfromance
- A R&D Project Proposal has been written and sent to ALICE, and PANDA (open to others, as well.)
  - The present ALICE upgrade for Run3 is based on custom hw solutions, and in ALICE it is now too late to change concept

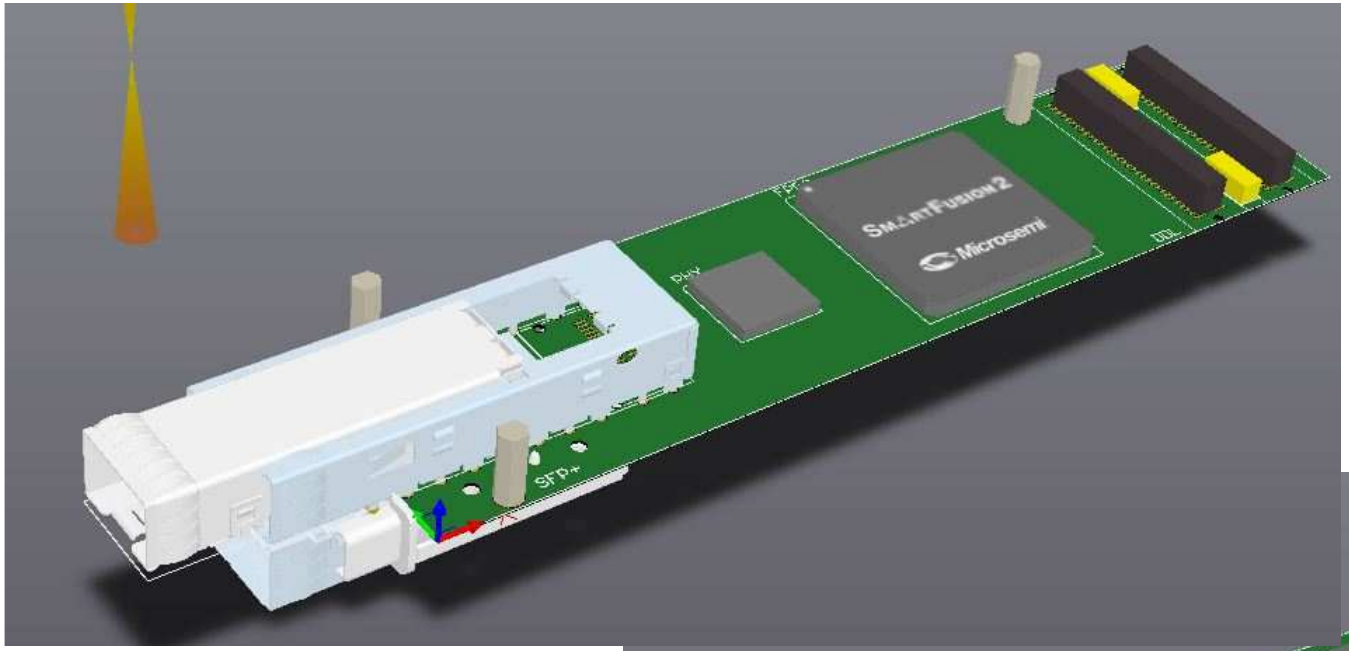
Project Proposal

Contents

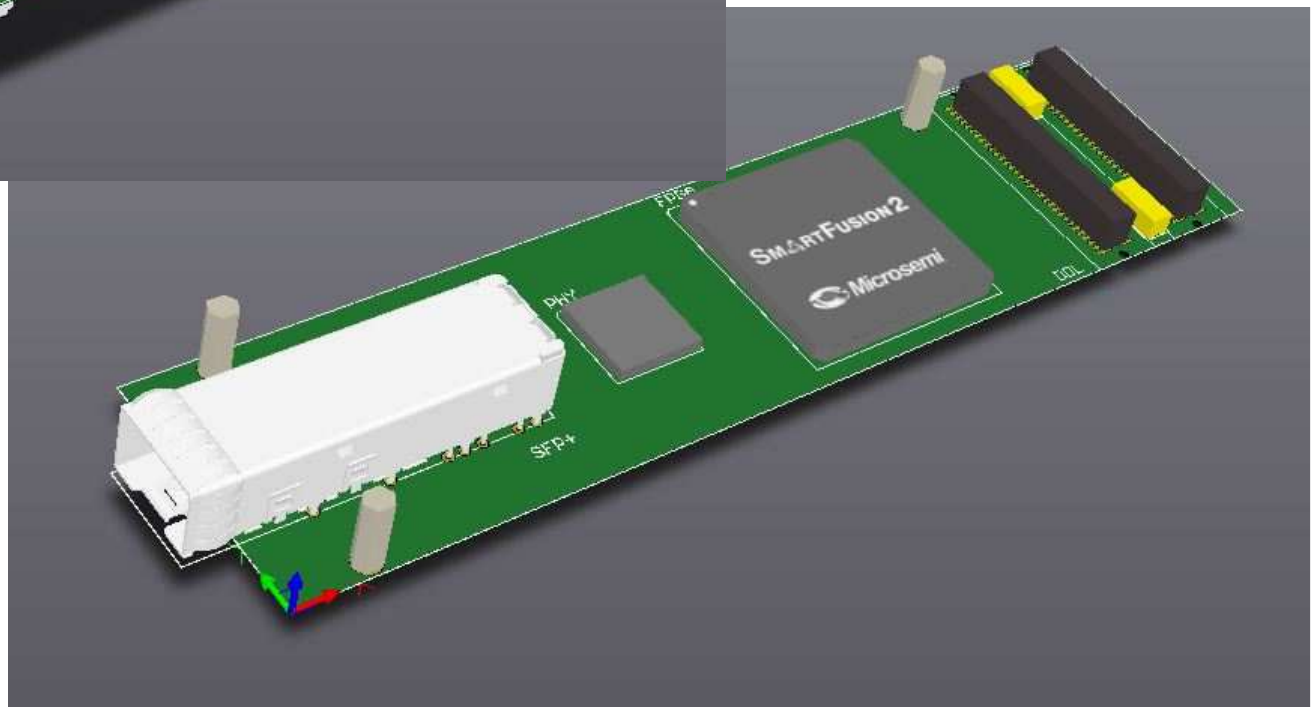
Thank you!

reserved slides

SIU+ with SmartFusion2 FPGA



Such evaluation card can be designed with other RadTol FPGAs (e.g. Kintex)



...we can have a lot of 10G interafce options:

- **SFP+**
- **QSFP**
- **iPass (PCIe External cabling)**

...even two in the same time!

SIU+ Logic Diagram