Cross-Vendor FPGA Design Using HDLMake

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introduction

- motivation: Intellectual Property (IP) reuse
- preferably across vendors (the good, the bad and the ugly)
  - Microsemi: *Currently Microsemi does not support custom/user created IPs in Libero Core Packager, i.e. adding them to vault not possible. There is no future plan to support this.* 08 Jan 2015
- standards for sharing IP blocks - not there yet
  - IEEE 1685-2014: Standard .. for Packaging, Integrating and Re-Using IP
  - IEEE 1735-2014: ... Encryption and Management of Electronic Design IP
- vendors' IP cores: restrictive license
  - Altera copyright header: *...that your use is for the sole purpose of programming logic devices manufactured by Altera and sold by Altera...*
  - Xilinx End User License Agreement: *...program only a Xilinx Device...*
- abstraction vs efficiency - always a tradeoff

about HDLMake

- generates `Makefile` from descriptor files (`Manifest.py`)
- supports multiple vendors: ISE, PlanAhead, Vivado, Quartus, Libero, Diamond
- supports modules ($\approx$ VHDL libraries), with cascading
- support for simulation, checking out files from git & SVN

Manifest.py for module / top level synthesys

counter_v1_00_a/Manifest.py

```
library = "counter_v1_00_a"

files = [
        "hdl/vhdl/counter.vhd",
]
```

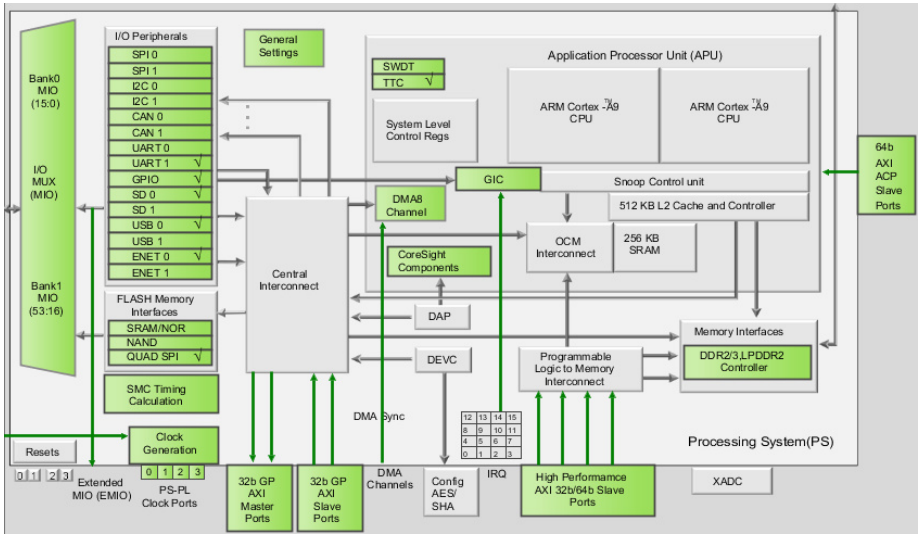
project/syn/Manifest.py

```
target = "xilinx"
action = "synthesis"

syn_device = "xc6slx150"
syn_grade = "-3"
syn_package = "fgg484"
syn_top = "top"
syn_project = "system.xise"
syn_tool = "ise"

modules = {
        "local" : [
                "../../pcoresng/counter_v1_00_a",
                "../../pcoresng/bsp_te0600_v2_00_c",
         ],
}

files = [
        "../hdl/vhdl/top.vhd",
]
```

sample command line log

```
[user@host syn]$ . /opt/Xilinx/14.7/ISE_DS/settings64.sh
...

[user@host syn]$ hdlmake auto
INFO    __main__.py:122: main() import tool module: ise
INFO    __main__.py:155: main() Running automatic flow.
INFO    synthesis_project.py:158: _generate_synthesis_project() Generating project for ISE v. 14.
...

[user@host syn]$ make
...
/opt/Xilinx/14.7/ISE_DS/ISE/bin/lin64/xtclsh run.tcl

Started : "Synthesize - XST".
Running xst...
Command Line: xst -intstyle ise -ifn "/home/mazsi/hardware/counter-te0600/syn/top.xst" -ofn "/hom
Reading design: top.prj

=========================================================================
*                          HDL Parsing                                  *
=========================================================================
Parsing VHDL file "/home/mazsi/hardware/pcoresng/bsp_te0600_v2_00_c/hdl/vhdl/mdioreg.vhd" into li
Parsing entity <mdioreg>.
Parsing architecture <imp> of entity <mdioreg>.
Parsing VHDL file "/home/mazsi/hardware/pcoresng/bsp_te0600_v2_00_c/hdl/vhdl/anegfixup.vhd" into
...
Process "Generate Programming File" completed successfully
```

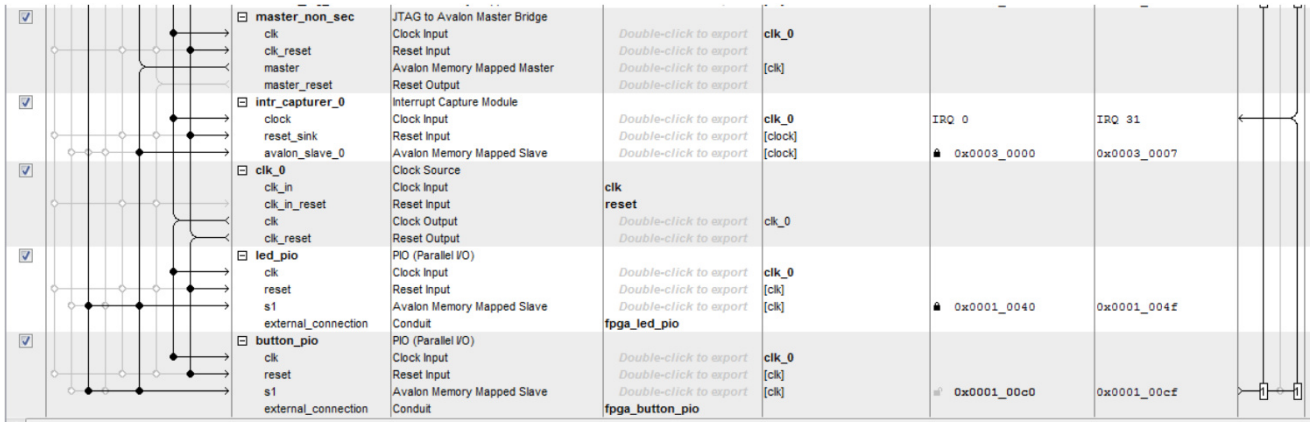
vendor block to HDL - Xilinx Zynq PS




```
library = "processing_system7_v4_03_a"

import os
xilinxedk = "../../../../../../../../../../../../" + os.environ['XILINX_EDK']
xilinxpcores = xilinxedk + '/hw/XilinxProcessorIPLib/pcores/'

files = [
        xilinxpcores + library + "/hdl/verilog/atc.v",
        ...
        xilinxpcores + library + "/hdl/verilog/processing_system7.v",
        xilinxpcores + library + "/hdl/verilog/trace_buffer.v",
        xilinxpcores + library + "/hdl/verilog/w_atc.v",
]
```

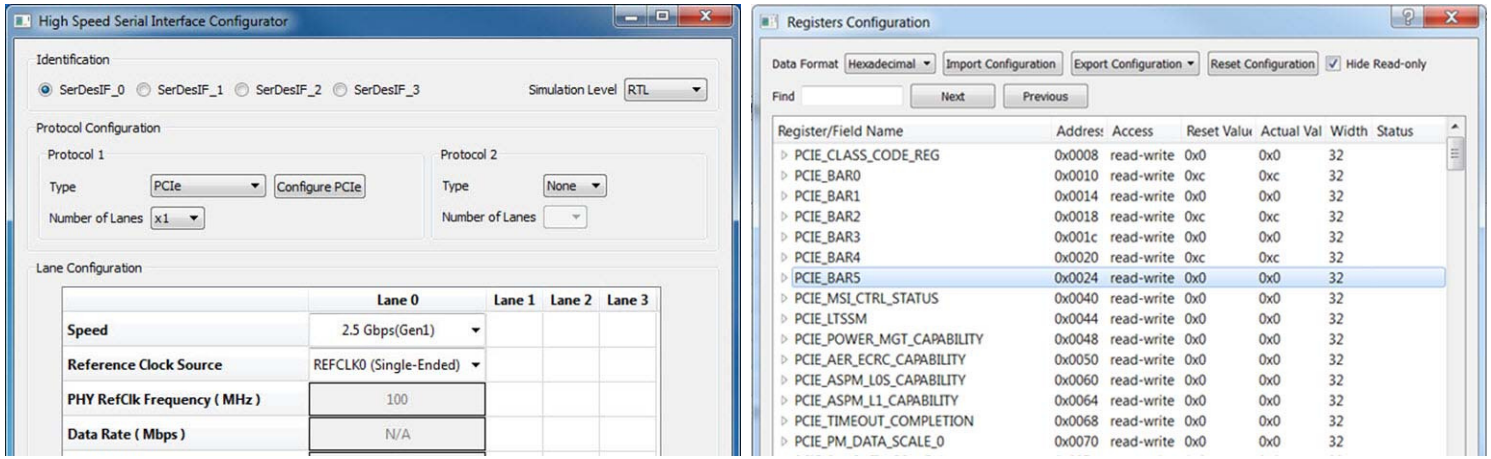
vendor block to HDL - Altera Qsys

http://free-electrons.com/wp-content/uploads/2013/06/




```
files = [
        "hdl/verilog/altera_avalon_packets_to_master.v",
        "hdl/verilog/altera_avalon_sc_fifo.v",
        "hdl/verilog/altera_avalon_st_bytes_to_packets.v",
        "hdl/verilog/altera_avalon_st_clock_crosser.v",
        "hdl/verilog/altera_avalon_st_idle_inserter.v",
        "hdl/verilog/altera_avalon_st_idle_remover.v",
        "hdl/verilog/altera_avalon_st_jtag_interface.sdc",
        ...
        "hdl/verilog/altera_merlin_master_translator.sv",
        "hdl/verilog/altera_merlin_slave_translator.sv",
        "hdl/verilog/altera_reset_controller.sdc",
        ...
]
```

vendor block to HDL - Microsemi

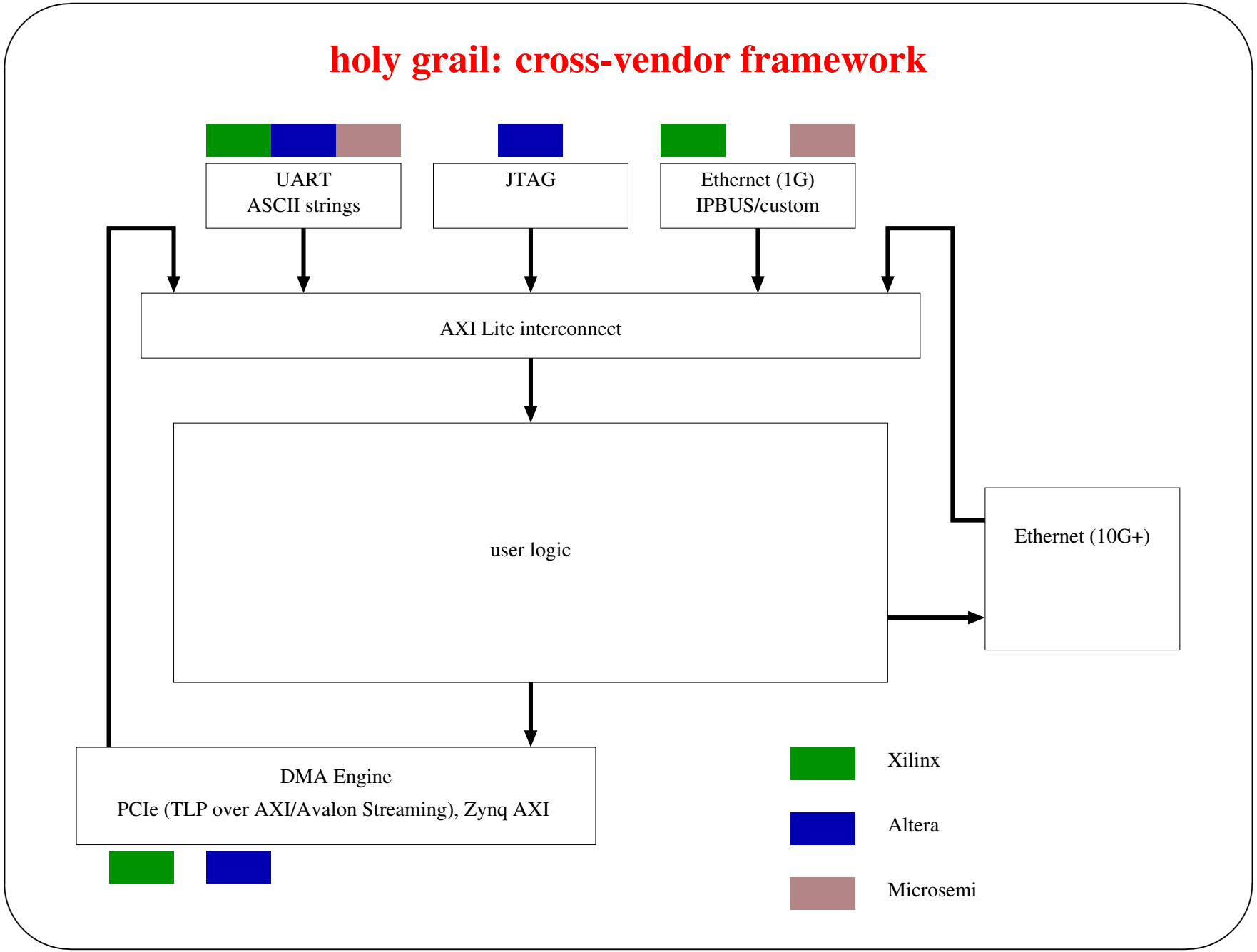



```
-------------------------------------------------------------------------------
-- config memory: 1 bit valid + 16 bit address + 32 bit data
-------------------------------------------------------------------------------

process (PCLK) is
  variable addr : std_logic_vector(7 downto 0);
begin
  if PCLK'event and PCLK = '1' then
    ...
    case addr is
      when X"00"  => memout <= "1" & X"A028" & X"0000_010F";
      when X"01"  => memout <= "1" & X"9198" & X"0000_0030";
      when X"02"  => memout <= "1" & X"9000" & X"0000_0080";
      when X"03"  => memout <= "1" & X"9004" & X"0000_0020";
      ...
```

FPGA families tested

Vendor	Family	Dev Board	Toolchain	Design
Xilinx	Spartan 6	TE0600	ISE 2014.7	Ethernet TX (GMII)
Xilinx	Virtex 6	CRORC	ISE 2014.7	PCIe (EPEE v2)
Xilinx	Kintex 7	KC705	ISE 2014.7	PCIe (EPEE v2)
Xilinx	Zynq	Red Pitaya	ISE 2014.7	PS $\rightarrow$ AXILite
Altera	Cyclone IV E	DE0-Nano	Quartus 15.1	SysConsole $\rightarrow$ AXILite
Altera	Cyclone IV GX	Transc. Starter	Quartus 15.1	PCIe (Altera refdesign)
Altera	Stratix V GX	AMC40	Quartus 15.1	Blinking LEDs
Actel	IGLOO 2	MPC-EX FE	Libero 11.4	Ethernet TX (SGMII)

EPEE - An Efficient and Flexible Host-FPGA PCIe Communication Library


holy grail: cross-vendor framework
UART
ASCII strings
JTAG
Ethernet (1G)
IPBUS/custom
AXI Lite interconnect
user logic
Ethernet (10G+)
DMA Engine
PCIe (TLP over AXI/Avalon Streaming), Zynq AXI
Xilinx
Altera
Microsemi

thank you!