Where now for FEE in FutureDAQ and NUSTAR DAQ?

White papers/specifications needed:

1. Slow Control for FEE
2. Timestamp and clock (does it need a trigger in/out too?)
3. Data output

3 groups of people to work on the interface specifications:

1. List of names and emails of people ready to work
2. Deadline for first draft of the interface specifications

Where now for ASICs?

ASIC:

1. List of names and emails
2. List of ASICs discussed here available to everyone in FAIR (and Spiral 2?). 1 page summary including:
   a) Description of device with block diagrams
   b) Measured (or simulated) performance
   c) Status:
      - Proposal?
      - Under design?
      - Prototype made?
      - Production?