# DLL based TDC's

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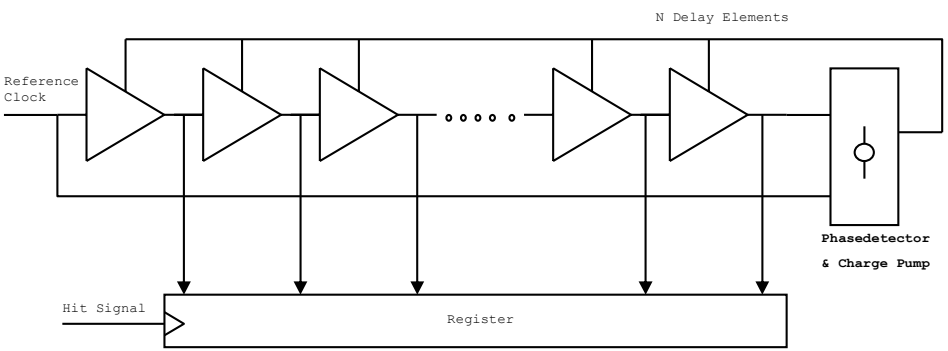
# Overview

- DLL based TDC's
  - Principle of DLL
  - Intrinsic Resolution
  - Concepts for improved Resolution

# A DLL based TDC




**D**elay **L**ocked **L**oop :

Closed regulation loop

Chain of N identical delay elements with adjustable delay each, phase detector and charge pump.

1 Register with Width N

Intrinsic resolution of a DLL is determined by the delay of a basic cell :

$$T_{Bin} = T_{ref} / N$$

Advantage:

Self Calibration to compensate temperature and process variations.

Dead Time free operation possible

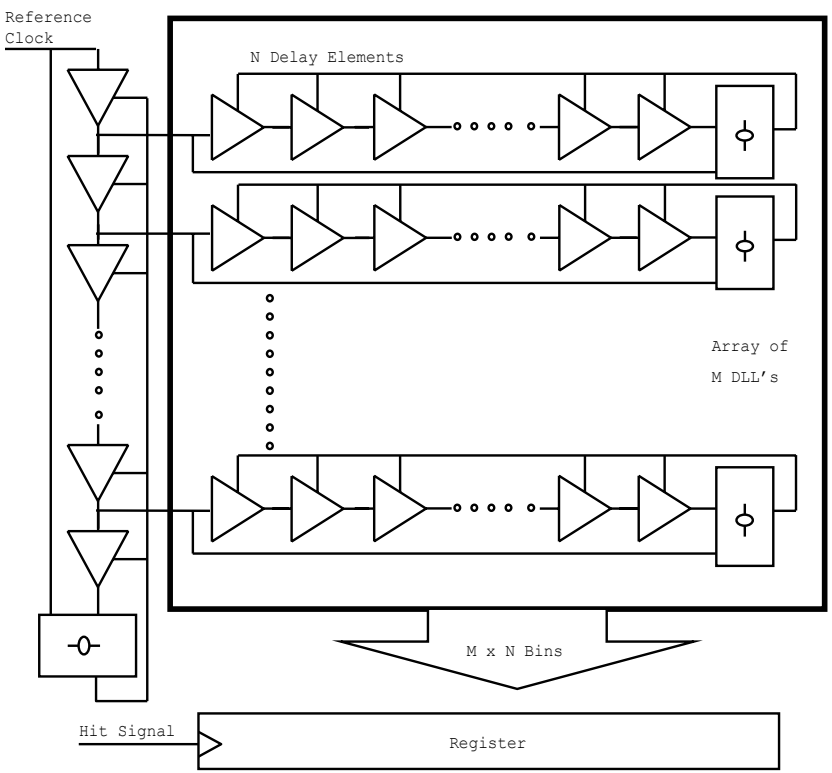
# Simulation results on UMC 180nm

- DLL with 128 DE
- Ref. Clock = 80 MHz
- Power 1.8V
- Corner
  - Temp. 20°C - 70°C
  - Process variations best & worst Case

=> Yields in an intrinsic resolution of $T_{Bin}$ ~ 100ps
Power Consumption /Channel ~ 2.8mW for an 8 Channel Core
(Hitregister & Encoding & Time over Threshold Encoding incl.)

How to improve the resolution……..

# An Array of DLL's




Running an array of M DLL's each with N Elements and – also DLL controlled -- phase shifts

Resolution determined by

$T_{Bin} = T_{Ref} / N – T_{Ref} / M$

N number of DE

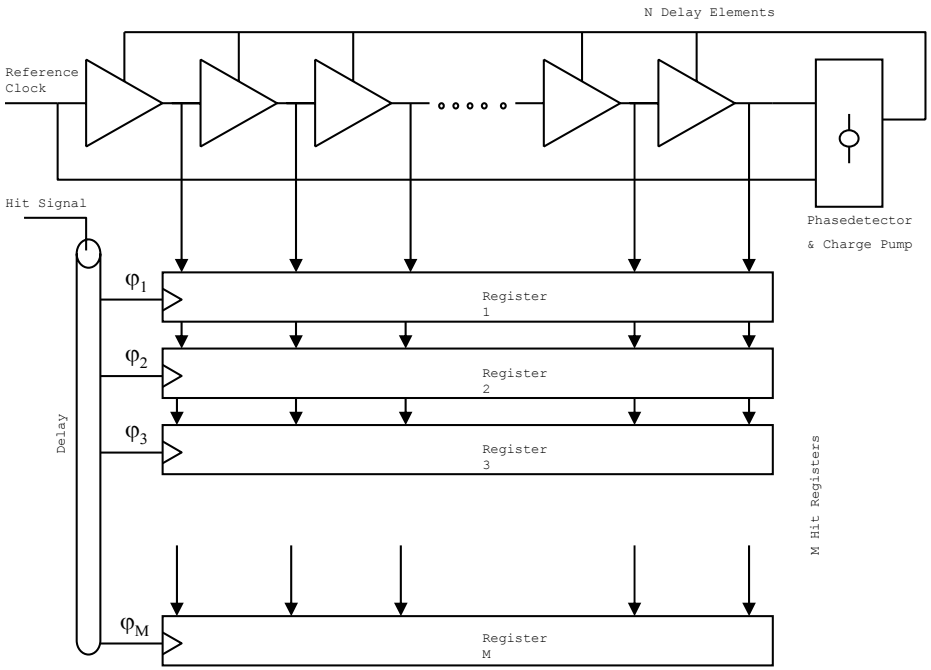
M counts of DLL's

1 register with width N * M

E.g.: 25ps intrinsic resolution

=> ~ 6mW/Chan.

# Time Interpolation cuircuit




Delay of ONE DE has been divided in M subdivisions by an RC-delay line resulting in an overall resolution determined by

$T_{Bin} = T_{Ref} / N * M$

N number of DE

M subdevision delay

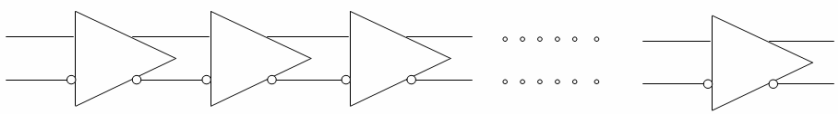
M registers with width N

Backdraw:

Badly controlled RC-Delay

Calibration necessary

# Differential Delay Chain



Using fully differential delay elements based on CML

Intrinsic resolution ~ 35 - 40 ps

But: higher power consumption

# Prototyp Submission

- Participation on UMC Mini-ASIC run in June 2005
  - DLL with 128 Delay Elements @ 80MHz
    - Hit-Register & Encoding for 1 Channel
    - 8 Bit parallel ReadOut

# Open Questions

- TDC resolution required?
- Single / double hit resolution
- (double hit only flagged??)
- Integration Level (Geometry)
- Event rate to cope with (100kHz)
- Discriminator spec's (time over threshold?)

  min. + max. signal length, double Hit resolution
- Data format : timestamp (Nr. of Clk Cycle)

  + 8bit Hit Position w.r.t. Clk (rising edge)

  + 8bit Hit Position " (falling " )

Or build difference on Chip: 8bit Hit Pos. (rising)

+ 8-9 bit Hit Length