Time measurement with differential ring oscillators

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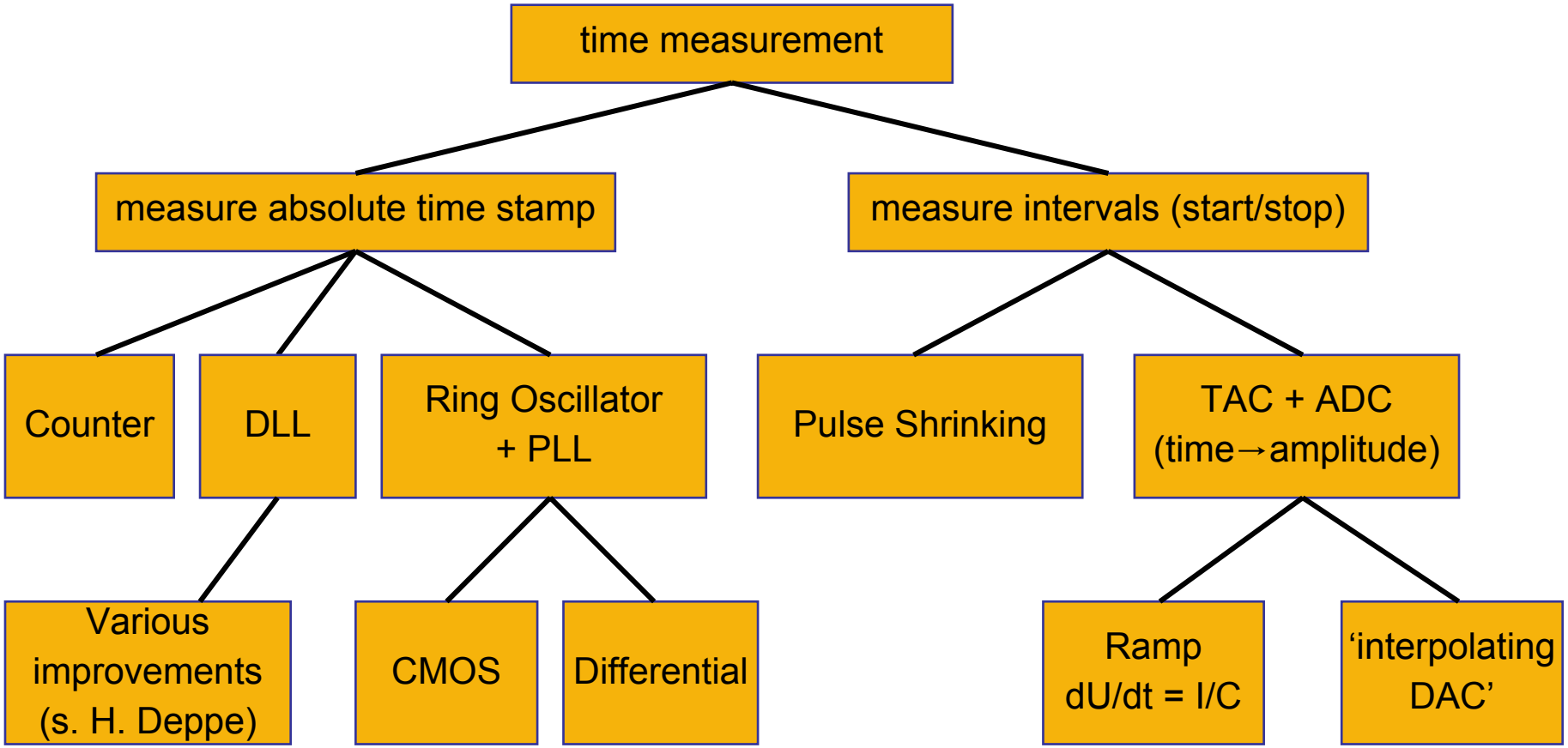
Talk Outline

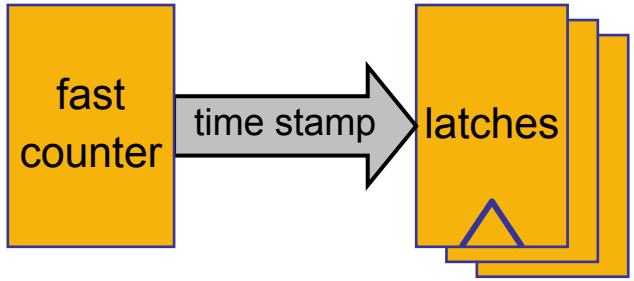
- Overview of common circuit concepts for time stamping
- Design issues
- Recent results with a ring oscillator test chip
- Summary and next steps

Overview of Circuit Concepts



…and mixtures of these concepts

Fast Counter

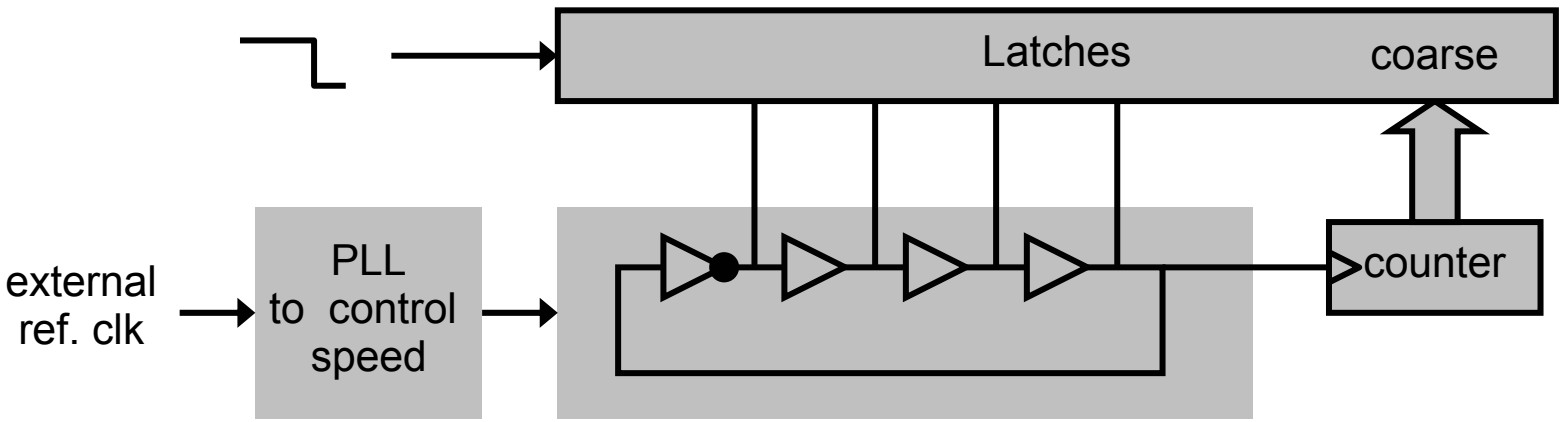


- Counter must use Gray coding or similar to avoid scrambled bits when latches jitter
+ very simple concept
+ stable and predictable bins
+ low power

- may reach some GHz in 0.18µm, i.e. bin widths of some ~200ps

- Improvement with staggering of several counters possible

Ring Oscillator: Principle



- Principle:
  - a ring oscillator generates thermometer code time stamps. Needs overall inversion!
  - a (‘slow’) coarse counter generates the MSBs
  - input signal is used to latch values
  - Ring oscillator can be locked to a reference clock with a PLL

\+ fairly simple, ‘digital’ design

\+ ‘infinite’ dynamic range

\+ no calibration required (with PLL), guaranteed stability

\- limited bin size (but several times better than with counter: only ‘inverter’ delay)

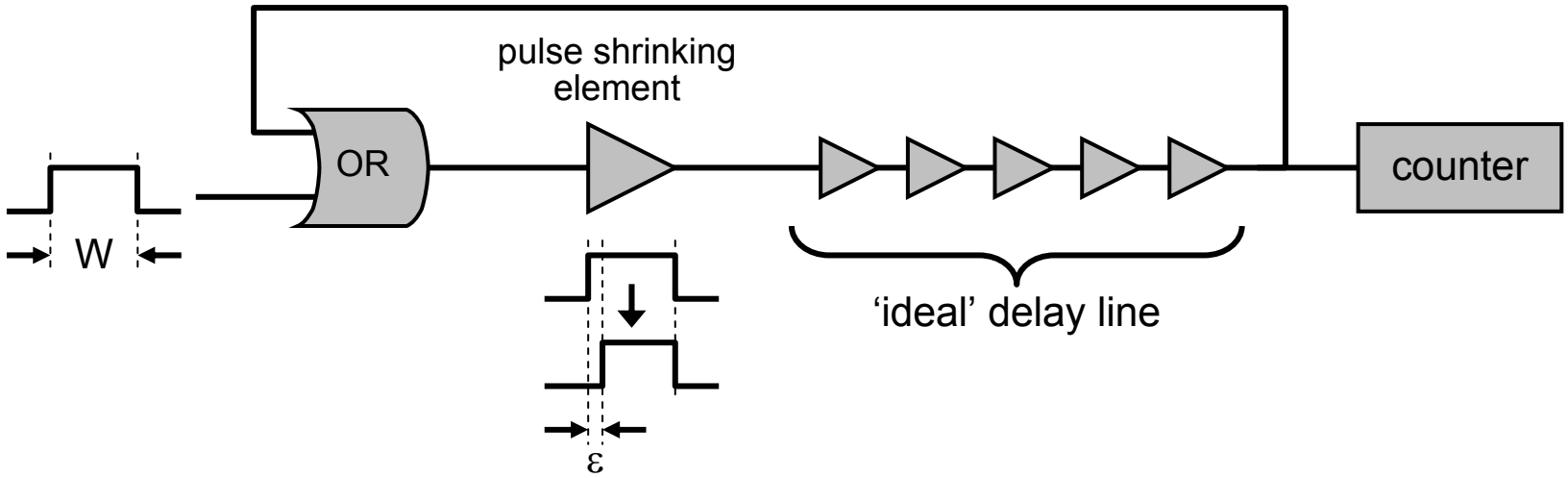
Ring Oscillator / DLL: Design variations

- Resolution can be increased by:
  - using multiple channels with delayed stop signals
  - running several phase coupled ring oscillators
  - ⇒ using slow / fast buffers between ring oscillator and latches
  - …

- Can use ‘single ended’ CMOS logic (see H. Deppe, GSI)
  - simple
  - issues: supply sensitivity, ring oscillator frequency range, linearity (inversion!)

- Or can use differential logic
  - uncommon
  - more complex, if everything (also PLL etc.) is done differentially
  - trimming simpler (change bias current)

Pulse Shrinking



- Principle:
  - Pulse is circulated in an (ideal) delay line.
  - **One** pulse shrinking element makes pulse shorter by constant ε with every 'turn'
  - Width is determined by counting 'turns' until pulse vanishes. W = N x ε
- Delay line must be longer than max. pulse width W_{max}

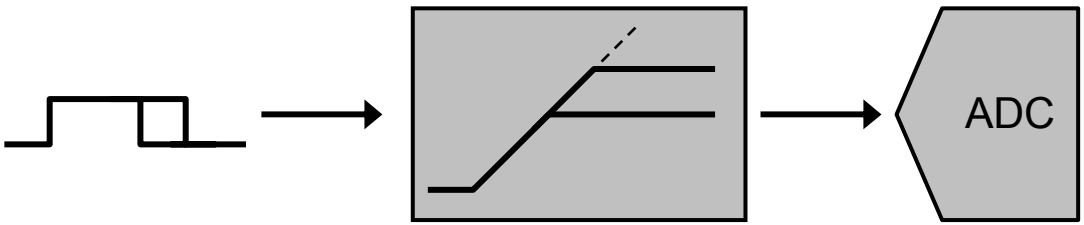
\+ Very low power

\- Conversion time is long and linked to resolution: $T = W_{max} \times W_{max} / \varepsilon$

\- Difficult calibration

\- Sensitive to matching and noise (?)

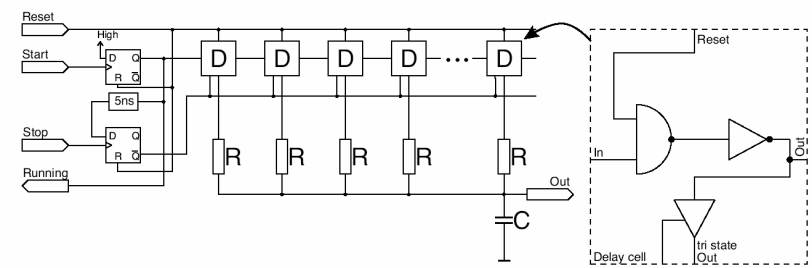
TAC + ADC



ramp generation

- Principle:
  - generate a linear voltage ramp during the strobe signal
  - convert the voltage to a digital value with an ADC
- Ramp can be generated with
  - constant current charging of a capacitor
  - an ‘interpolating DAC’ (see H. Flemming, GSI)

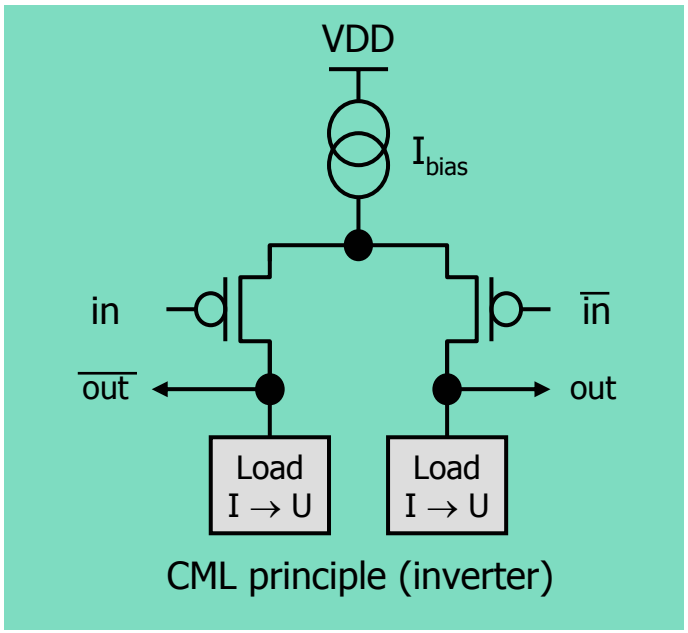
+ very high resolution
- needs ADC (space, power, calibration!)
- extra circuitry needed to generate MSBs
- Issues are calibration and stability



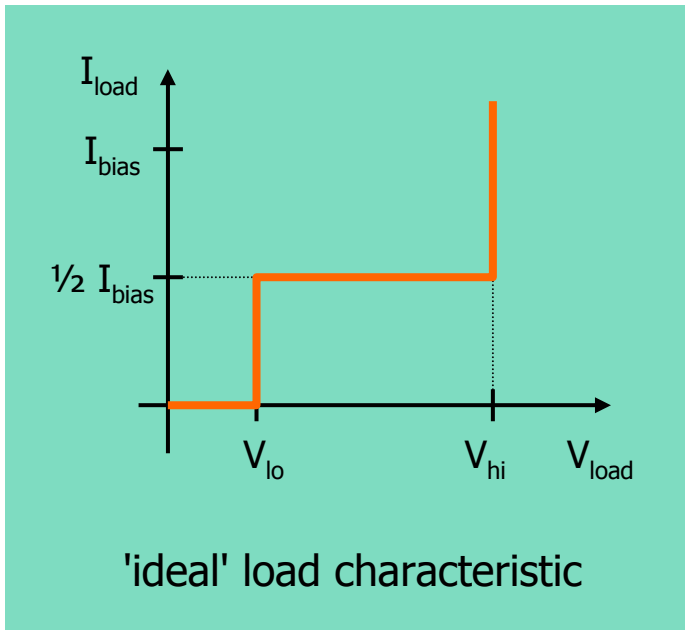
from CBM TSR

Differential Logic

- Current I_{bias} is steered to left or right load circuit with a differential pair
- The load circuit converts to current step to a voltage step
- **'ideal' load** circuit:
  - The V_{hi}-level is fixed by the maximum possible input voltage to the switch block (~VDD-V_{TP}-V_{DSat})
  - The V_{lo}-level is fixed by the voltage swing required to 'fully' switch current in the switch block.
  - The plateau at ½ I_{bias} guarantees equal rise and fall times (C_{load} is charged/discharged with ±½ I_{bias})
- If V_{hi} and V_{lo} are independent of I_{bias}, the speed of the gate can be varied significantly with I_{bias}



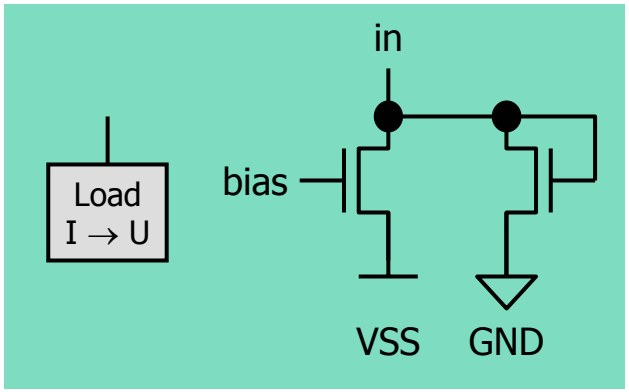
CML principle (inverter)

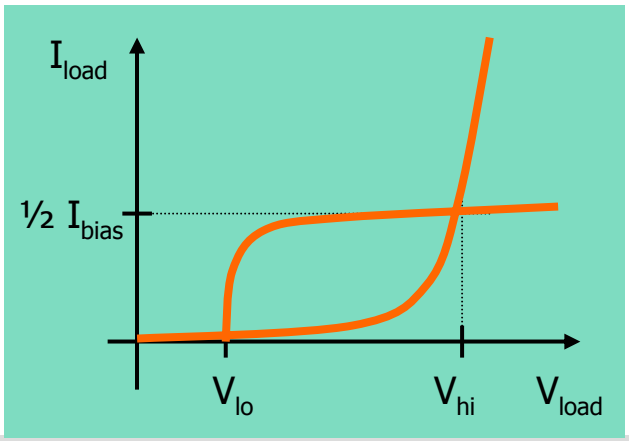


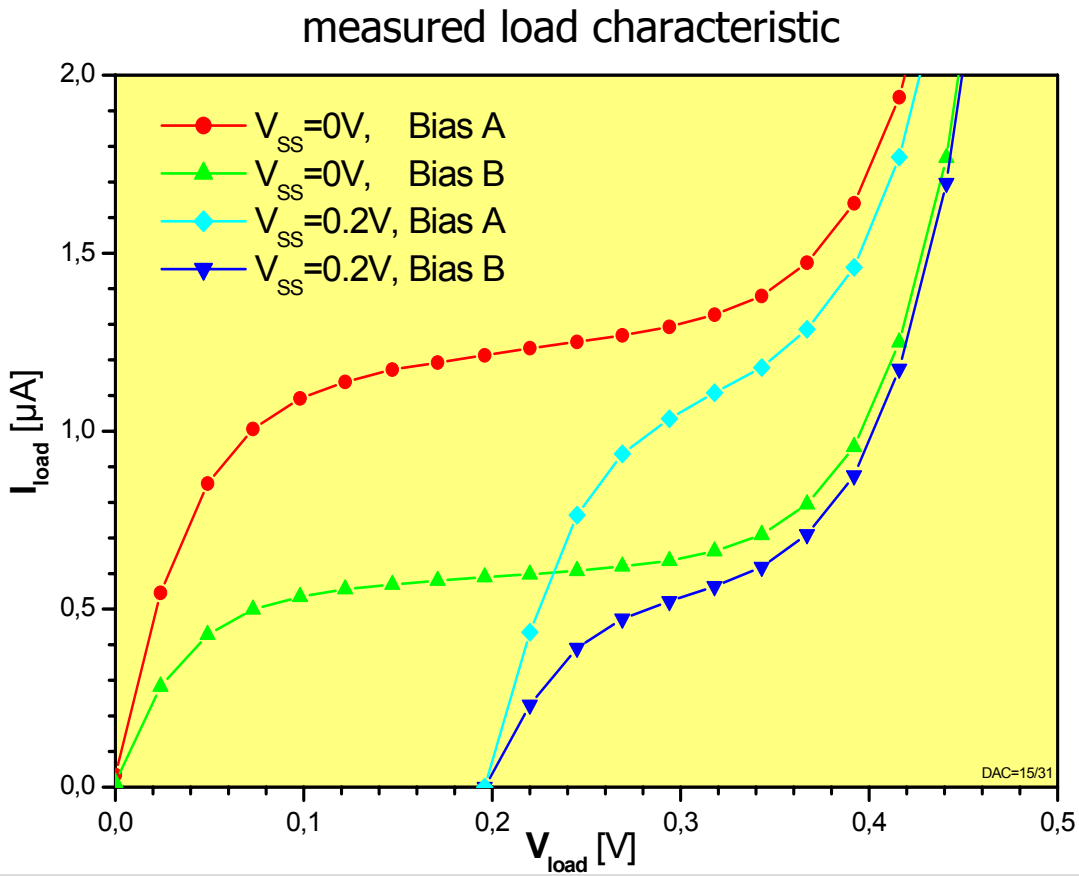
'ideal' load characteristic

Proposed Load Circuit (I→U converter)

- Parallel connection of:
  - NMOS operated as a current source with adjustable source voltage VSS
  - diode connected NMOS (other solutions are possible)



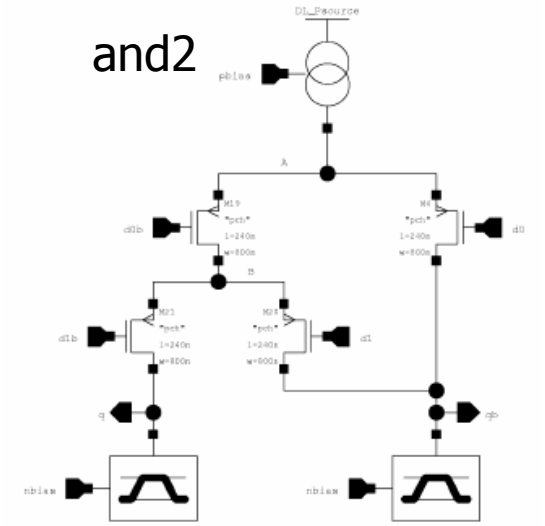




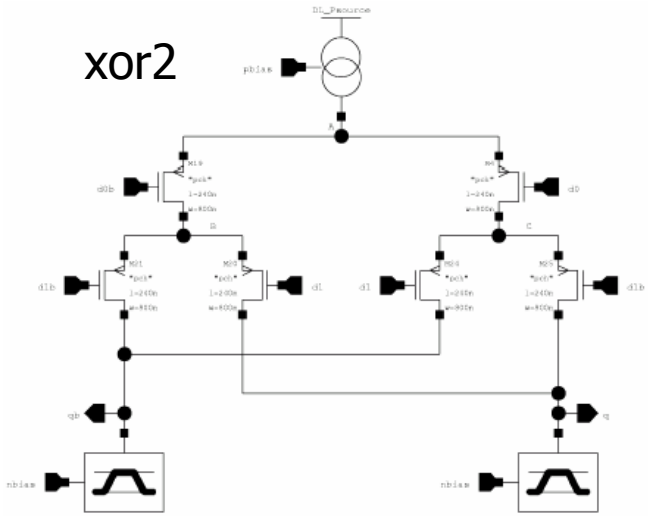
Differential Gates

- Logic function is implemented in a switch tree
- Complex functions can be implemented in one gate (saving current!)

and2



xor2



Function	CMOS		Differential	
	PMOS	NMOS	PMOS	NMOS
and2	2	2	4+1	4
and3	3	3	6+1	4
xor2	5(3)	5(3)	6+1	4
mux2	3	3	6+1	4
latch	4	4	6+1	4
Latch w. input MUX	7	**7**	10+1	**4**

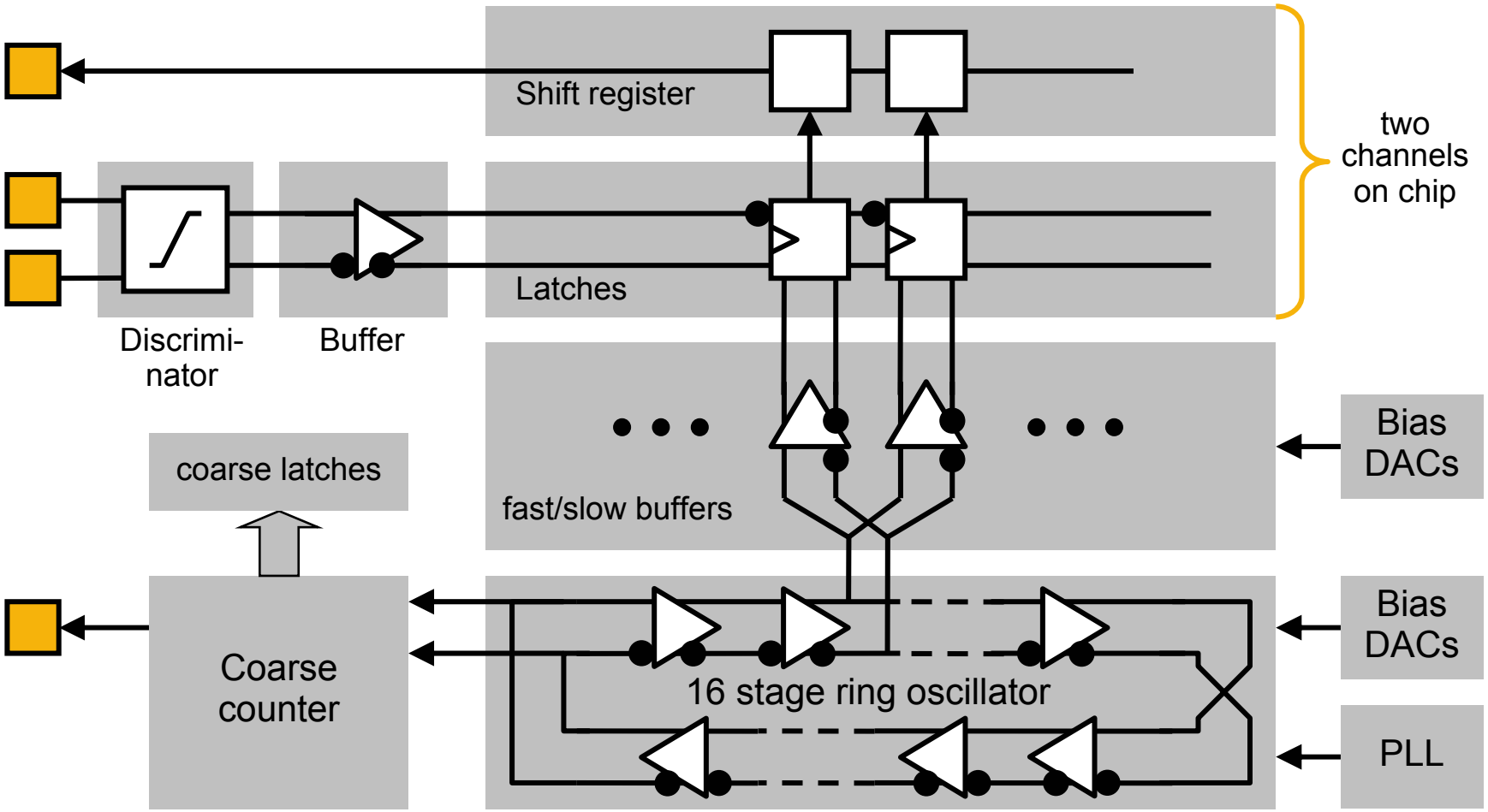
Design Issues

- Design goals are
  - minimal bin width = max. resolution
  - linearity
  - dynamic range
  - low dead time = high double hit rate
  - low power
  - easy calibration
  - stable operation (with temperature, power supply etc.)
  - multi-chip operation

- Watch
  - matching between devices:
    better for larger devices, but that costs power and/or speed…
  - radiation hardness
  - technology scaling (this favors ‘digital’ designs)

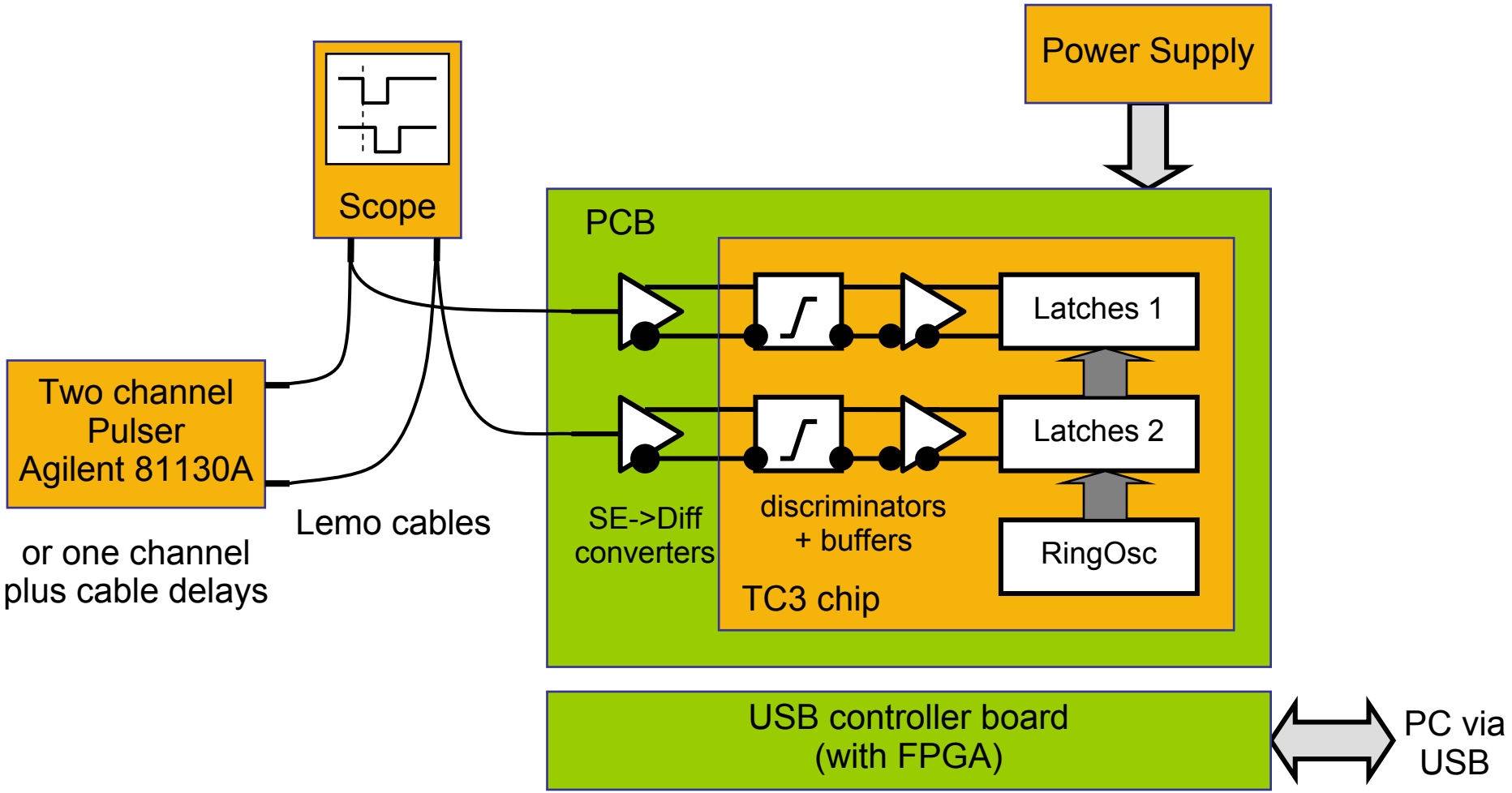
AMS 0.35µm Test Chip 'TC3'

- Block diagram shows only relevant parts
- **Note that the differential inputs have an additional (analog) discriminator on this chip**



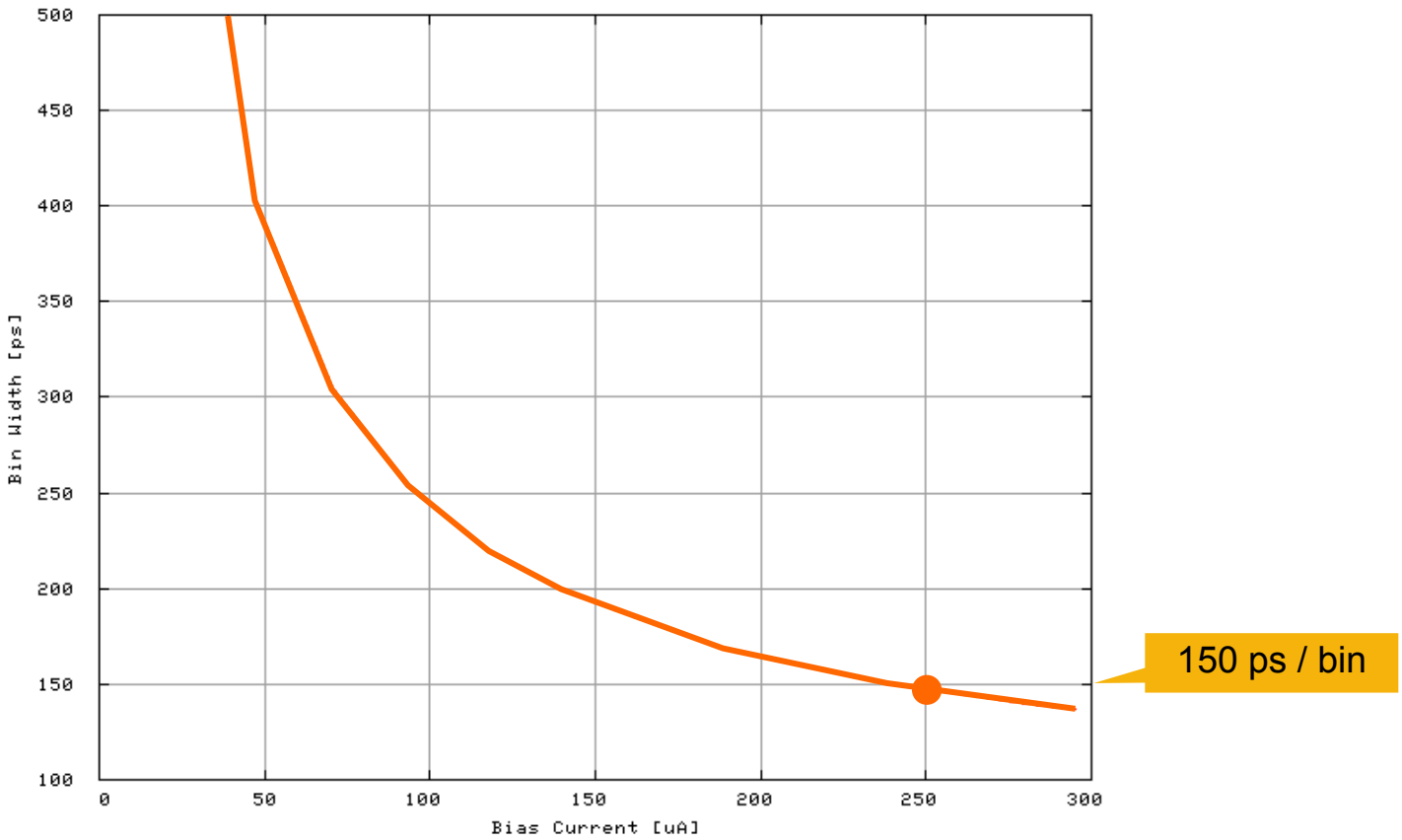
Test Setup

- We have developed a very compact USB based test setup.



Measurements: Ring Oscillator Speed

- 16 stage Ring oscillator speed can be measured accurately on a scaled down digital output
- Speed can be tuned in a wide range as a function of the bias current (per stage)
- Standard operation point: **150 ps / bin @ 250µA per stage**

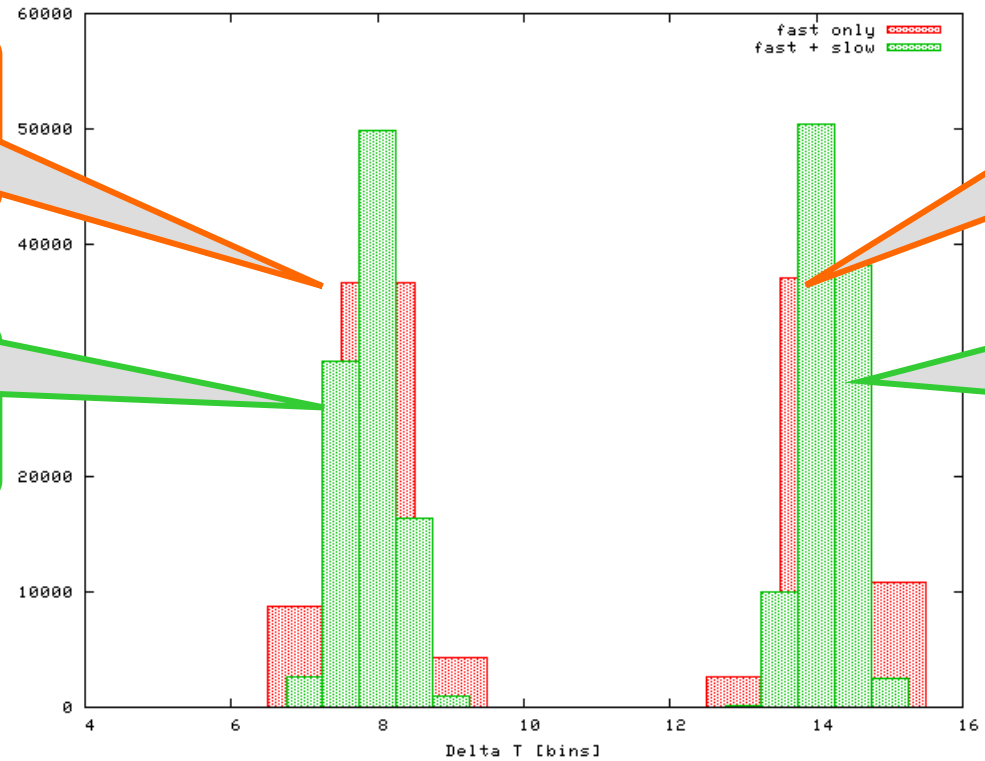


Hit bins for two different delays

- Inject in the **two channels** with a constant (cable) delay
- VCO speed: **150ps / bin** $\Rightarrow \sigma_{ideal}$ = 43.3 ps
- Plot time **difference** (here in bins) for two delays (red)
- Also plot fine grain result using (uncalibrated) 'slow' buffers (green)
- Note that measured **coincidence sigma = √2 x single channel sigma**

Only coarse:
σ_{coin} = 0.506 bins
σ_{single} = 54 ps

+ slow (uncal.):
σ_{coin} = 0.382 bins
σ_{single} = **41 ps**

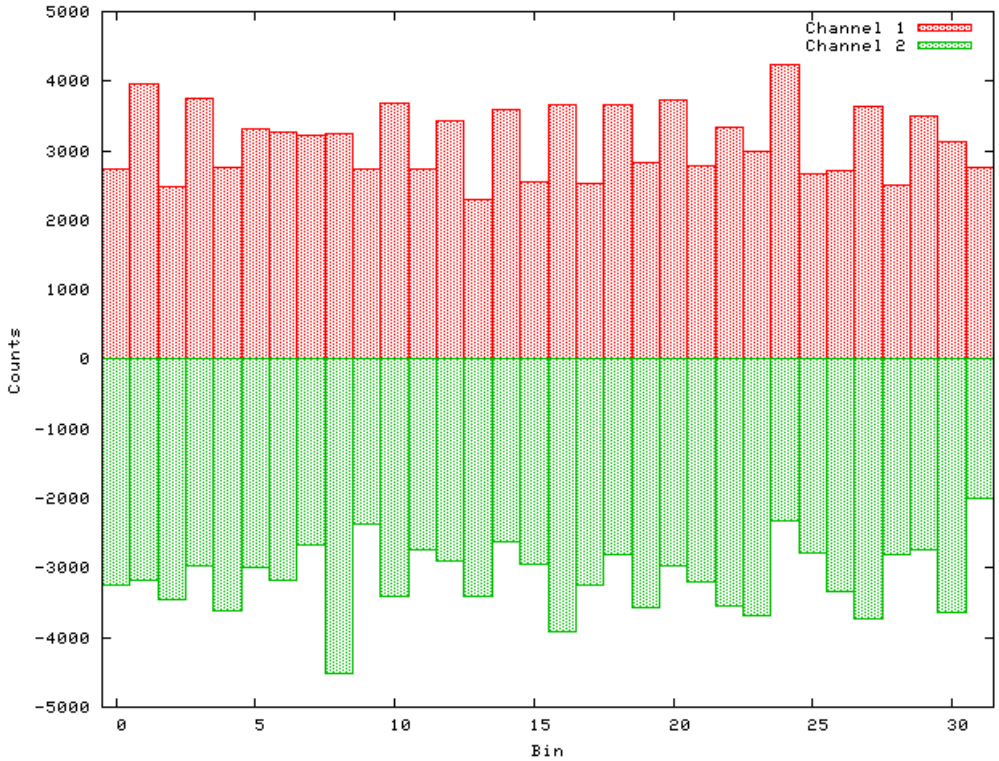


Only coarse:
σ_{coin} = 0.494 bins
σ_{single} = 52 ps

+ slow (uncal.):
σ_{coin} = 0.351 bins
σ_{single} = **37 ps**

Bin occupancies (i.e. relative bin width)

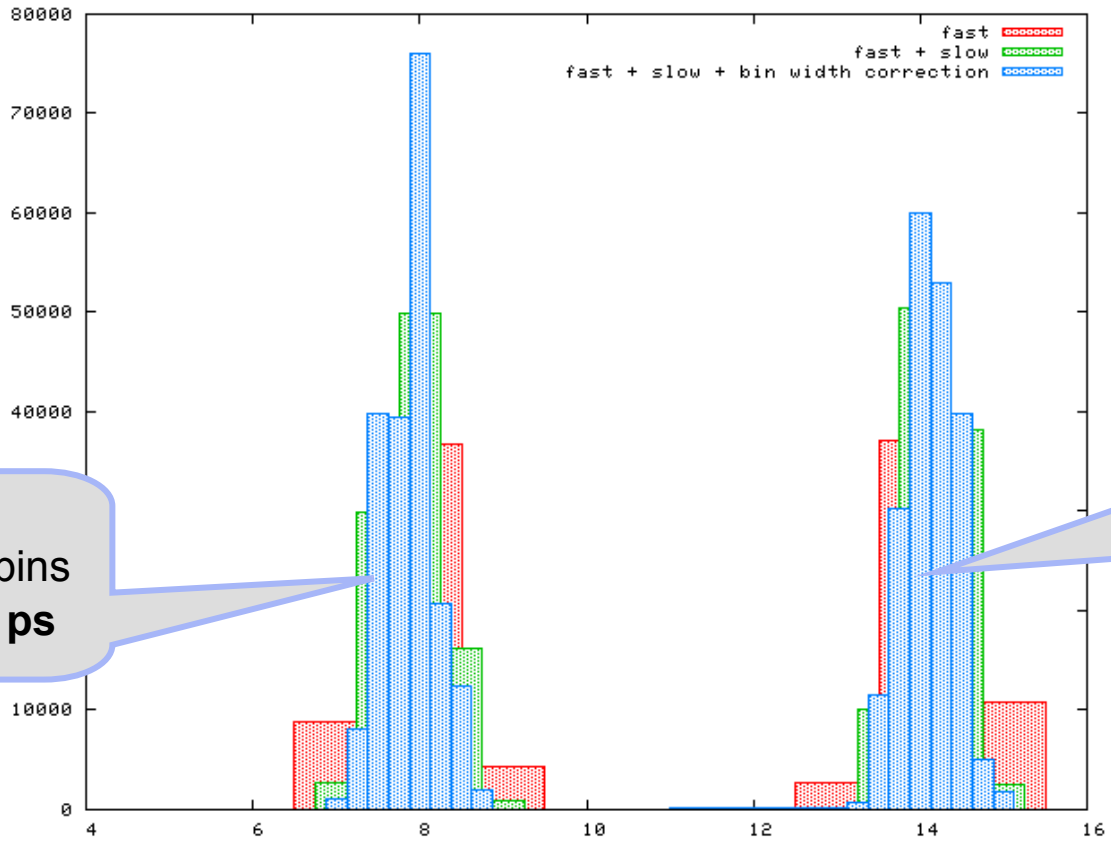
- Generate hits at random moments. Display counts for both channels
  - Equal time bin widths would give homogeneous bin occupancy
  - Shorter bins have lower occupancy



- This measurement can be used to **correct for bin size**
- Note: variations are from transistor mismatch and stable in time – a chip ‘fingerprint’

Bin width correction

- Use bin width information (fast / slow / mixed) for correction
- Maybe this result can still be optimized by adjusting the delay of the slow buffer…



corrected:
σ_{coin} = 0.323 bins
σ_{single} = **34.2 ps**

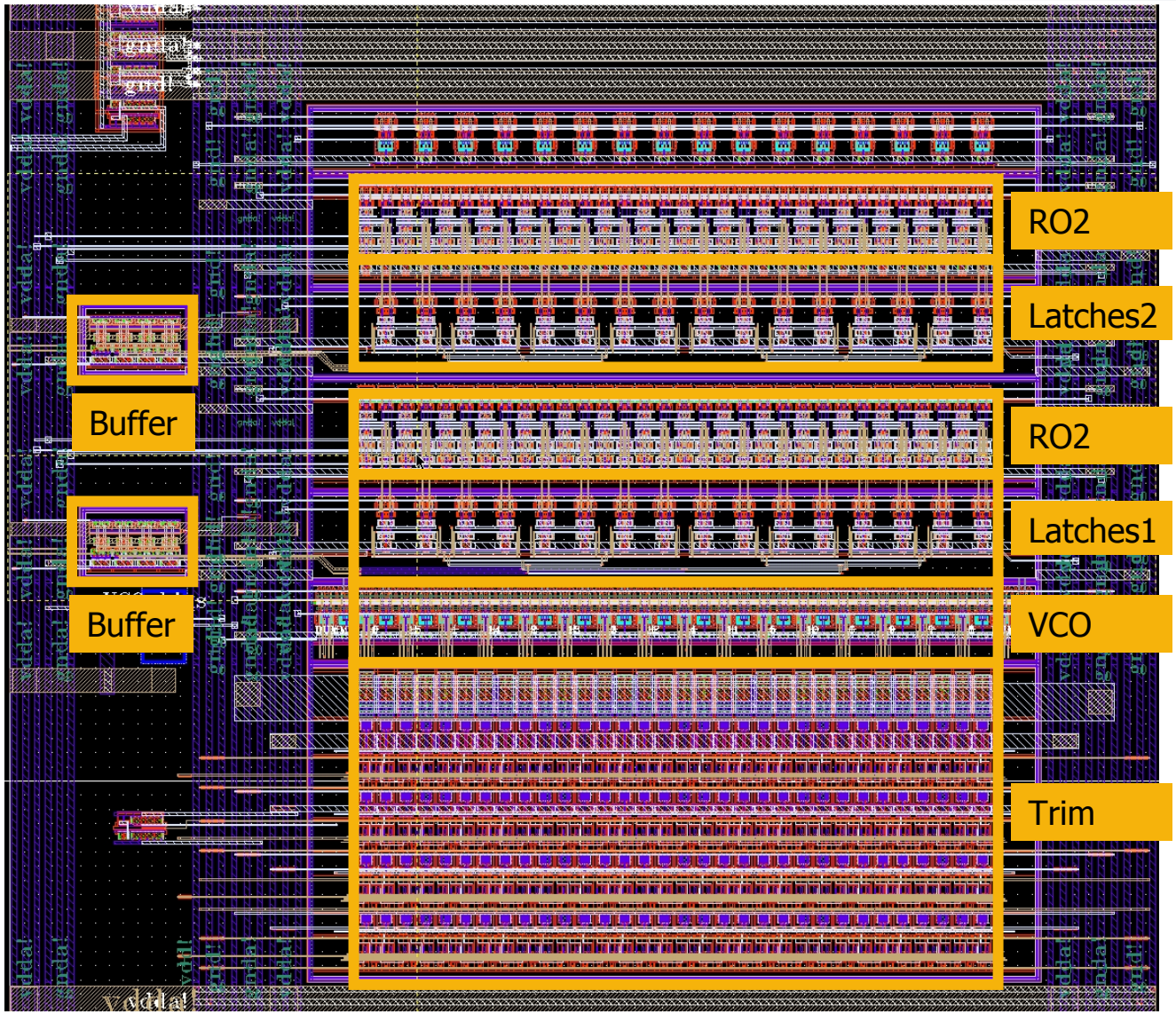
corrected:
σ_{coin} = 0.317 bins
σ_{single} = **33.6 ps**

- Note that any non-linearities are included in this measurement!

Next Test Chip: UMC 0.18µm (GSI Submission)

- 16 stages
- 2 groups of latches
- VCO with or without delay trim

- VCO: 260 x 30 µm²
- Trim: 260 x 120 µm²



Layout:
VCO with Trim

Summary and outlook

- We pursue a **ring oscillator** approach using **differential logic**
- Single channel resolution σ **~ 35ps** already reached in 0.35µm technology

- Advantages of the ring oscillator are:
  - stability (if locked to reference frequency with a PLL)
  - 'infinite' dynamic range (with wide 'coarse' counter)
  - very small dead time
- Is power consumption acceptable ? (<15mA @ 2V per channel + VCO…)

- Expect factor ~2 improvement in 0.18µm, i.e. σ **~ 25ps** (test chip has only fast bins).

- Next steps:
  - Test UMC chip (is back, but not tested yet due to bonding problems…)
  - Increase speed, linearity, resolution – work is in progress