Time Distribution System

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Outline:

- Concept
- COMPASS Trigger Distribution System
- Future TDS Components
- Prototype module
- Outlook

Concept

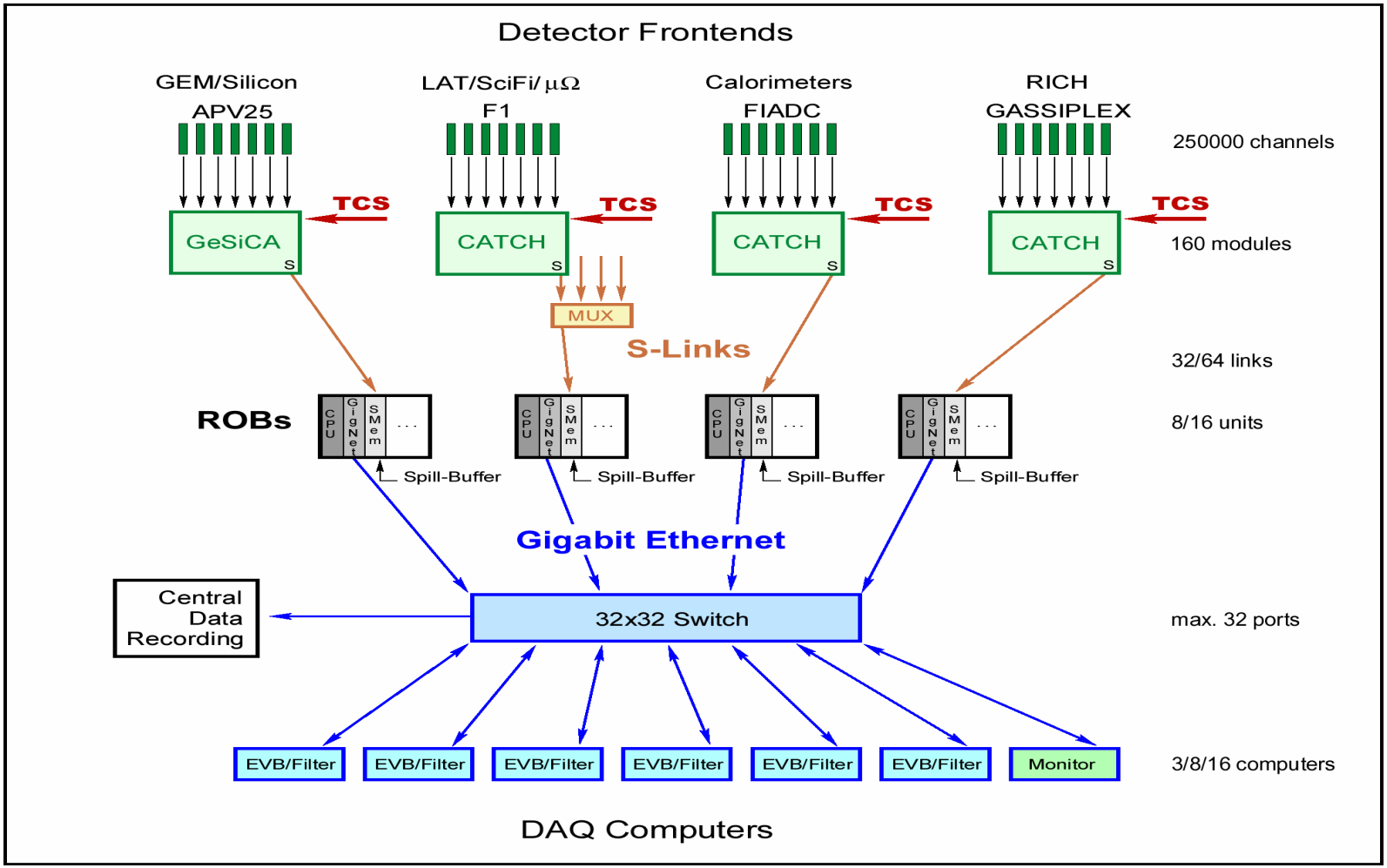
Distribute single clock to all FEE, the clock provides a common time reference

Clock distributed via optical network

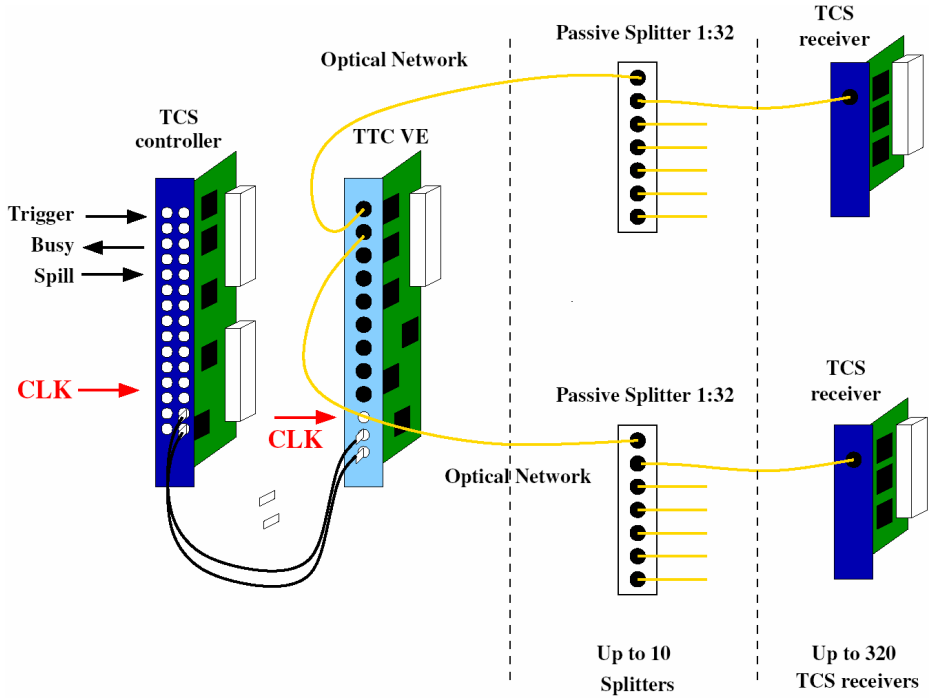
Clock is distributed together with control information

Architecture: Single source -> 1000 destinations

COMPASS DAQ


Detector Frontends
GEM/Silicon
APV25
LAT/SciFi/μΩ
F1
Calorimeters
FIADC
RICH
GASSIPLEX
250000 channels
TCS
TCS
TCS
TCS
GeSiCA
CATCH
CATCH
CATCH
160 modules
MUX
S-Links
32/64 links
ROBs
CPU
GigNet
SMem
8/16 units
Spill-Buffer
Spill-Buffer
Spill-Buffer
Spill-Buffer
Gigabit Ethernet
Central Data Recording
32x32 Switch
max. 32 ports
EVB/Filter
EVB/Filter
EVB/Filter
EVB/Filter
EVB/Filter
EVB/Filter
Monitor
3/8/16 computers
DAQ Computers

COMPASS Trigger Control System



Distributes:

155.52 (38.88) MHz clock , Jitter < 50 ps

Synchronous (fixed propagation time)
- RESET/Time ZERO
- Trigger
- Pre Trigger

Asynchronous(propagation time not fixed)
- Event #
- Spill #
- Control information
  ENABLE/DISABLE

Other features
- Multi DAQ support

Encoder components : PECL logic with dif. I/O
Receiver components : CLC016(NS) clock recovery chip + PECL logic with dif. I/O

Important for low jitter: DC/DC converter to power Optical receiver and Clock Recovery chip

Proposed Time Distribution System

Components :

- Master Module with SerDes IC , 2 GBd serial speed
- Passive optical splitters
- 1000 destinations with SerDes IC

Distribution :

Time Reference by distributing low jitter CLOCK

Synchronous signals with fixed propagation time

- Time Zero
- Enable/Disable – stop/start data taking
- EPOCH signal
- Control/calibration signal to FE/Detectors if needed

Other Features :

Fine CLOCK Phase Adjustment individually at each FE to compensate detector position and fibre length

Clock jitter requirements :

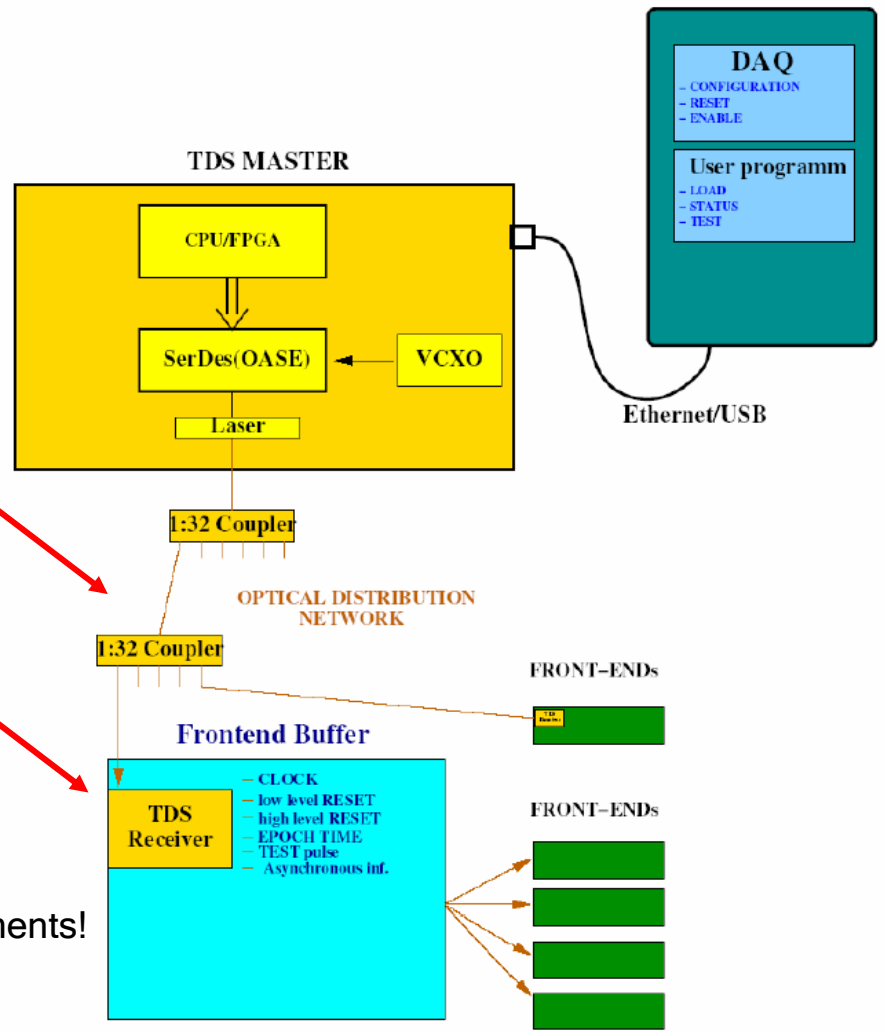
20 ps(RMS) for TOF detectors, 100 ps for all other detectors

TDS Architecture

•TDS master module
TDS encoder and laser module

• Passive optical splitter 1:32

• TDS mezzanine cards which are mounted on FE modules or DAQ modules



SERDES chip requirements:
• fixed propagation time of recovered clock
• differential CLOCK output
• long availability time

No commercial components fulfill these requirements!

OASE ASIC is the candidate for SERDES!

SerDes IC Clock Jitter

SerDes transmitter jitter parameters (HDMP-1636 and HDMP-8268)

RJ = 8 ps(σ) , DJ =15 ps (p-p) @1250 MBaud

RJ = 4 ps(σ) , DJ =15 ps (p-p) @2500 MBaud

where

RJ - random jitter caused by

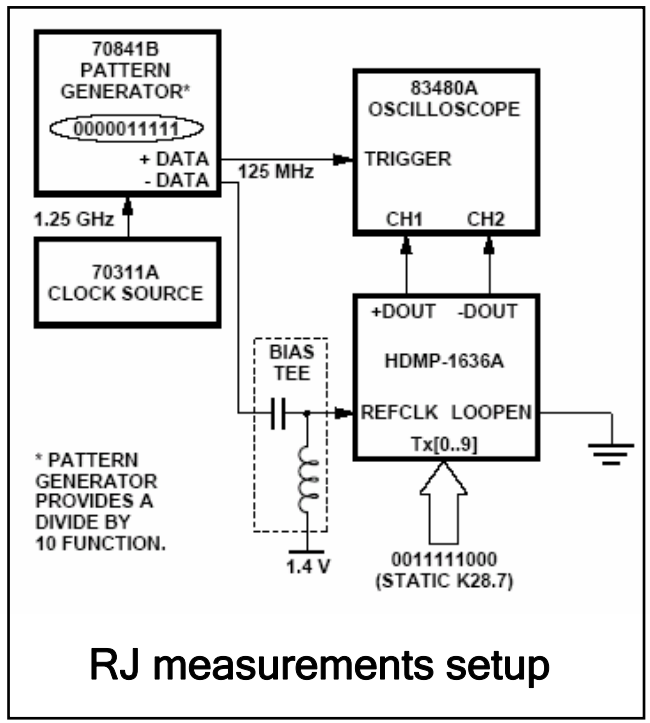
- VCO noise
- high frequency PS noise

DJ -deterministic jitter

- caused by data pattern

To be mentioned:

DJ/RJ caused by low frequency noise are not specified



RJ measurements setup

Jitter measurement of full chain is needed

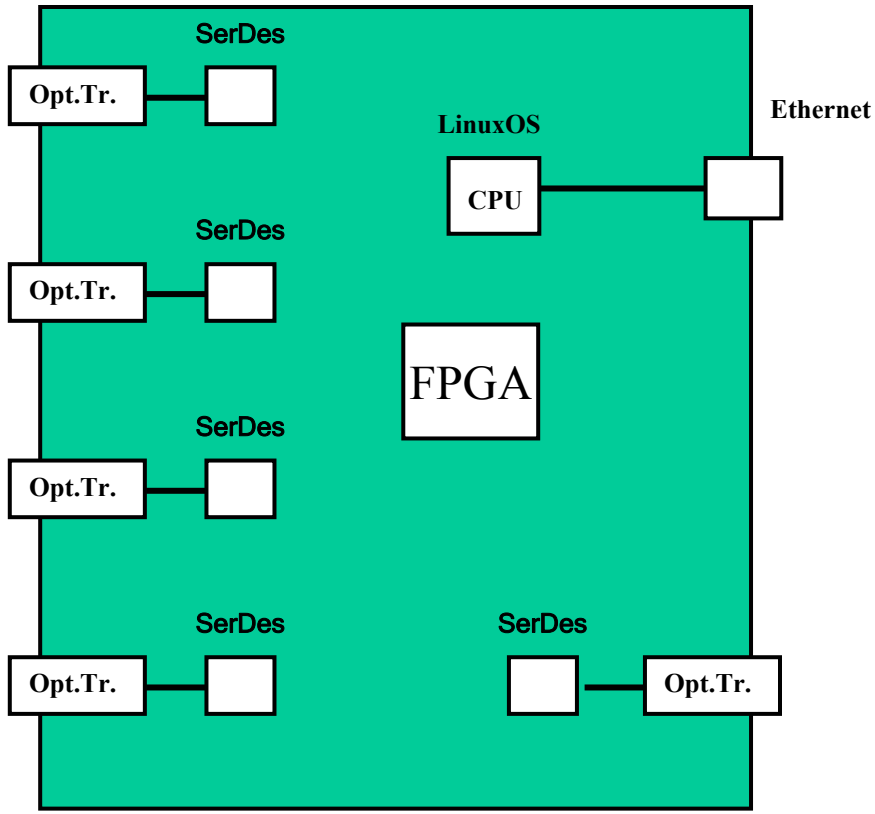
Sketch of TDS master module

Components:

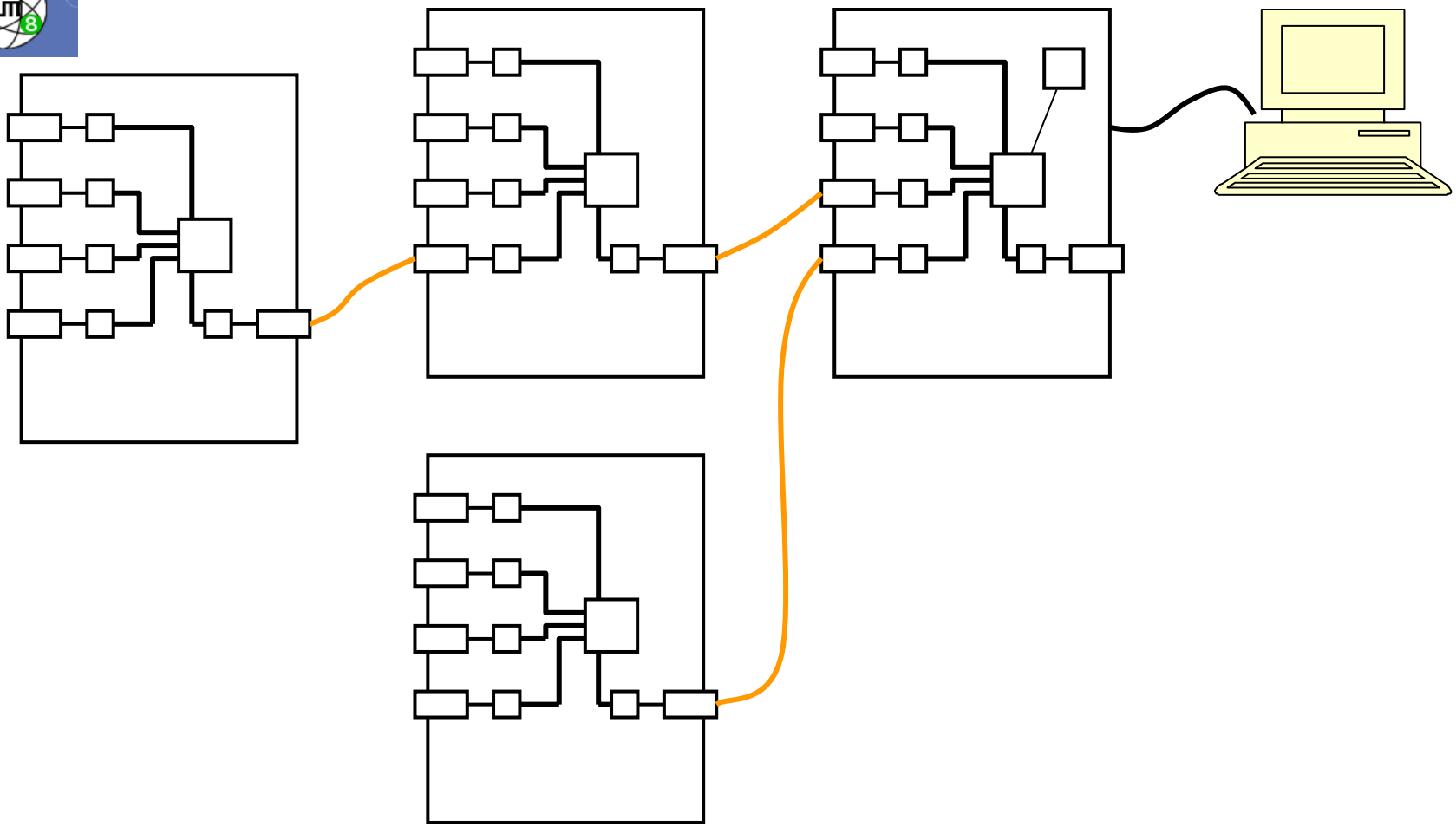
- V4 FPGA
- Embedded CPU with Linux
- SerDes
  - OASE
  - Agilent HDMP-1636

Usage:

- Time distribution system and readout module for new SADC
- Test bench for clock jitter measurements



Setup for clock jitter measurements



Outlook

- Build a mini prototype of TDS and readout system : SADCs + TDS
- Get first ideas of clock jitter behavior for different configurations

Questions for investigation and discussions :

- TDS-FEE interface
- TDS system with bidirectional optical link
- Interface with BuTiS and synchronization with accelerator

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