



CCLRC
Daresbury Laboratory

FEE for Nuclear Spectroscopy at FAIR

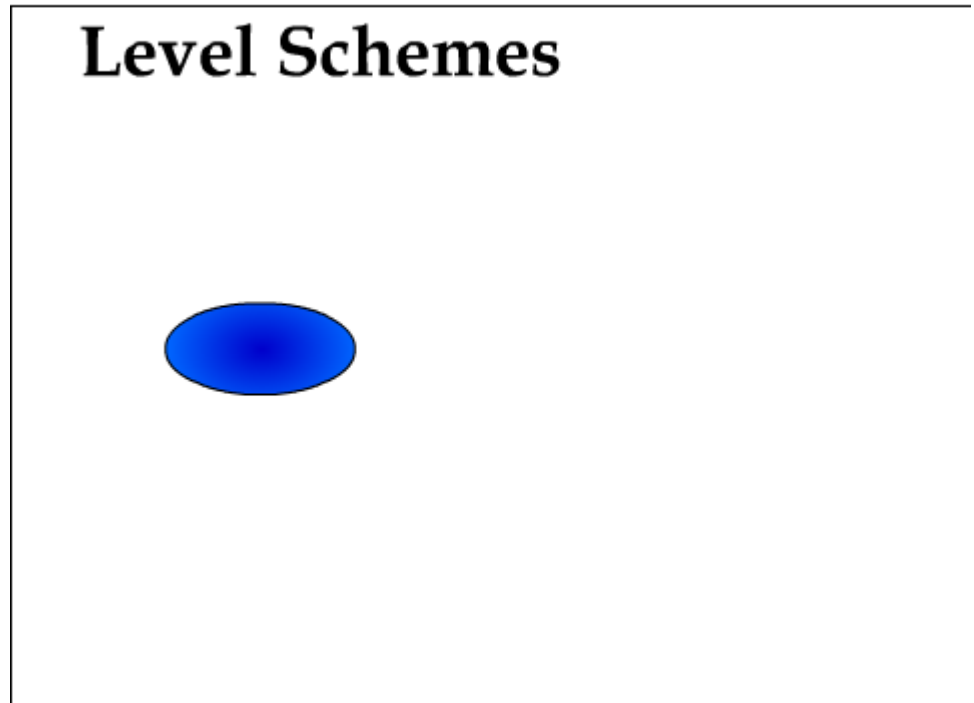
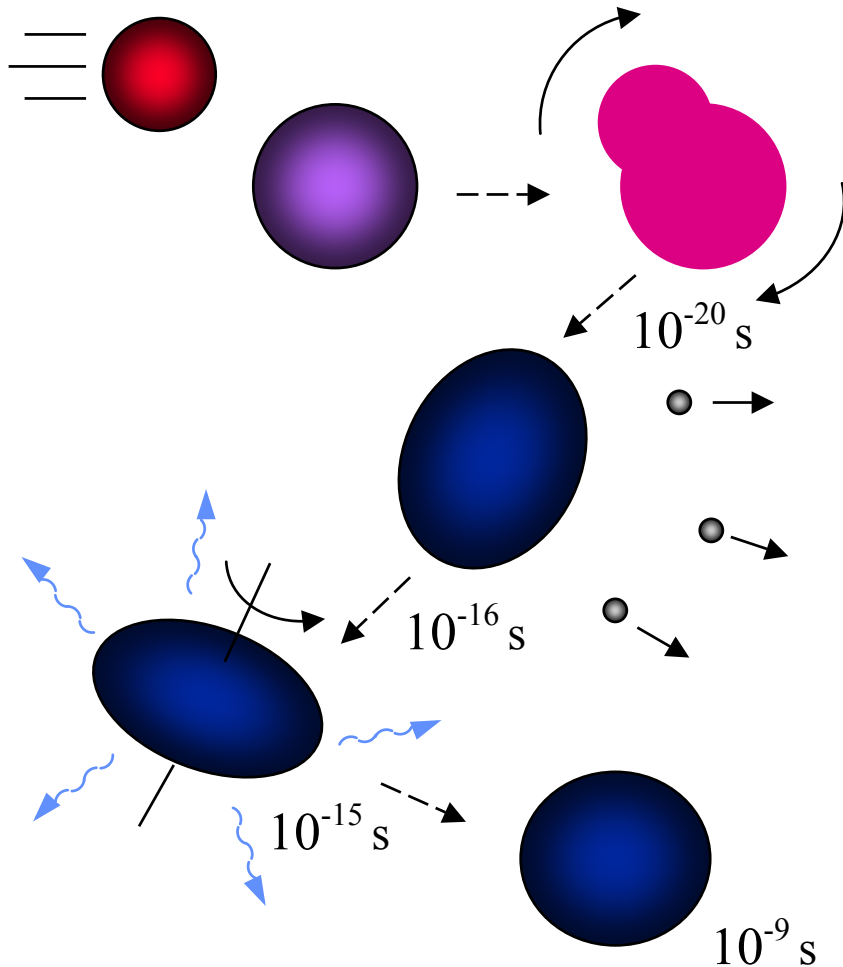
1st FAIR FEE Workshop
11th-13th Oct 2005

Ian Lazarus
NPG, CCLRC Daresbury

- Detectors and FEE for Gamma-ray spectroscopy
- Detectors and FEE for Charged Particle spectroscopy
- Detectors in some of the larger NUSTAR experiments
- Examples of FEE- DESPEC Implantation Detector
- Examples of FEE- EXL recoil detector
- FEE ASIC meeting report
- Common FEE architecture

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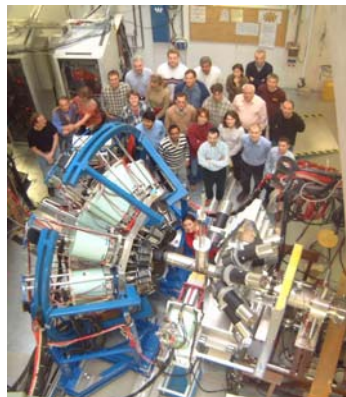
Excite a nucleus. Then watch...



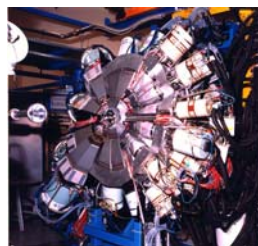
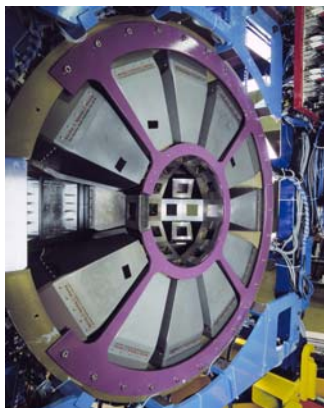
Heavy Ion Fusion Evaporation Reaction
» Nucleus at High Spins «

- **Detector Requirements:**
 - Good stopping power (density)
 - Good energy resolution (usually)
 - Good position resolution often needed too
- **Detector materials:**
 - Ge for best resolution
 - Scintillators (CsI, BGO, NaI) for price or timing
- **FEE Requirements:**
 - Energy resolving (0.1% over wide dynamic range)
 - As well as E, need T and often X,Y,Z position.
 - Low Noise
 - Good accuracy, low drift
 - High throughput rate (limited by filtering)

Nuclear Spectroscopy Instrumentation in Europe prior to FAIR



RISING, GSI



Euroball



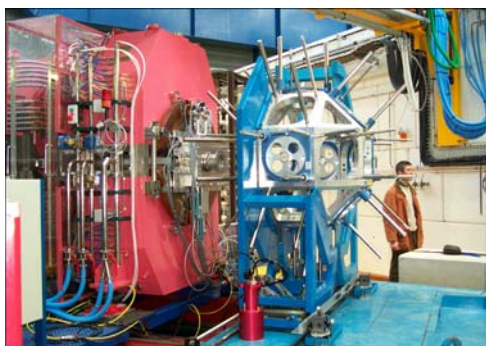
**JUROGAM,
GREAT, JYFL**



CLARA, LNL

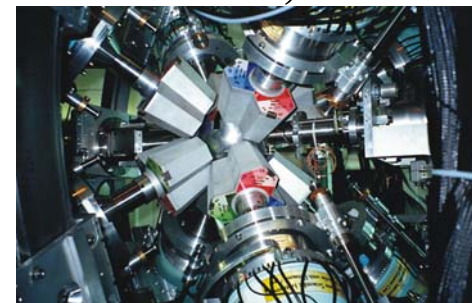
Radioactive beam spectroscopy

EXOAM, SPIRAL, Ganil

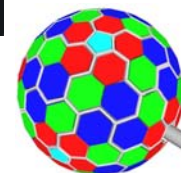


- Segmentation
- Encapsulation
- Position determination from pulse shape analysis

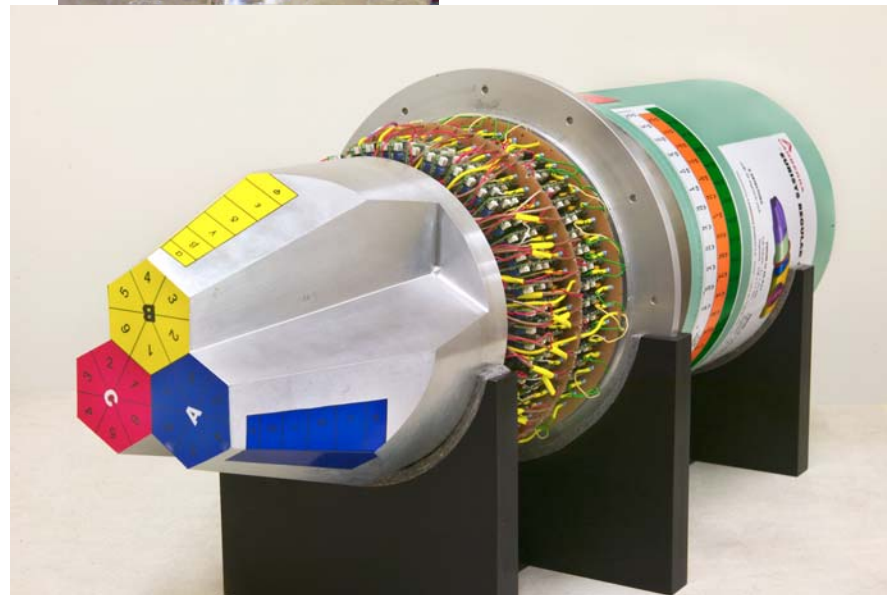
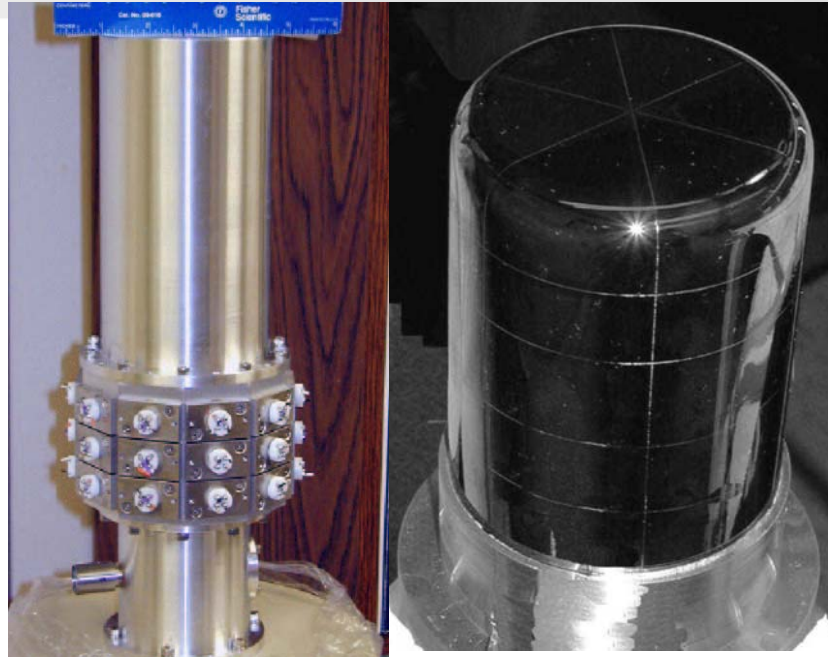
MINIBALL, RexIsolde, GSI



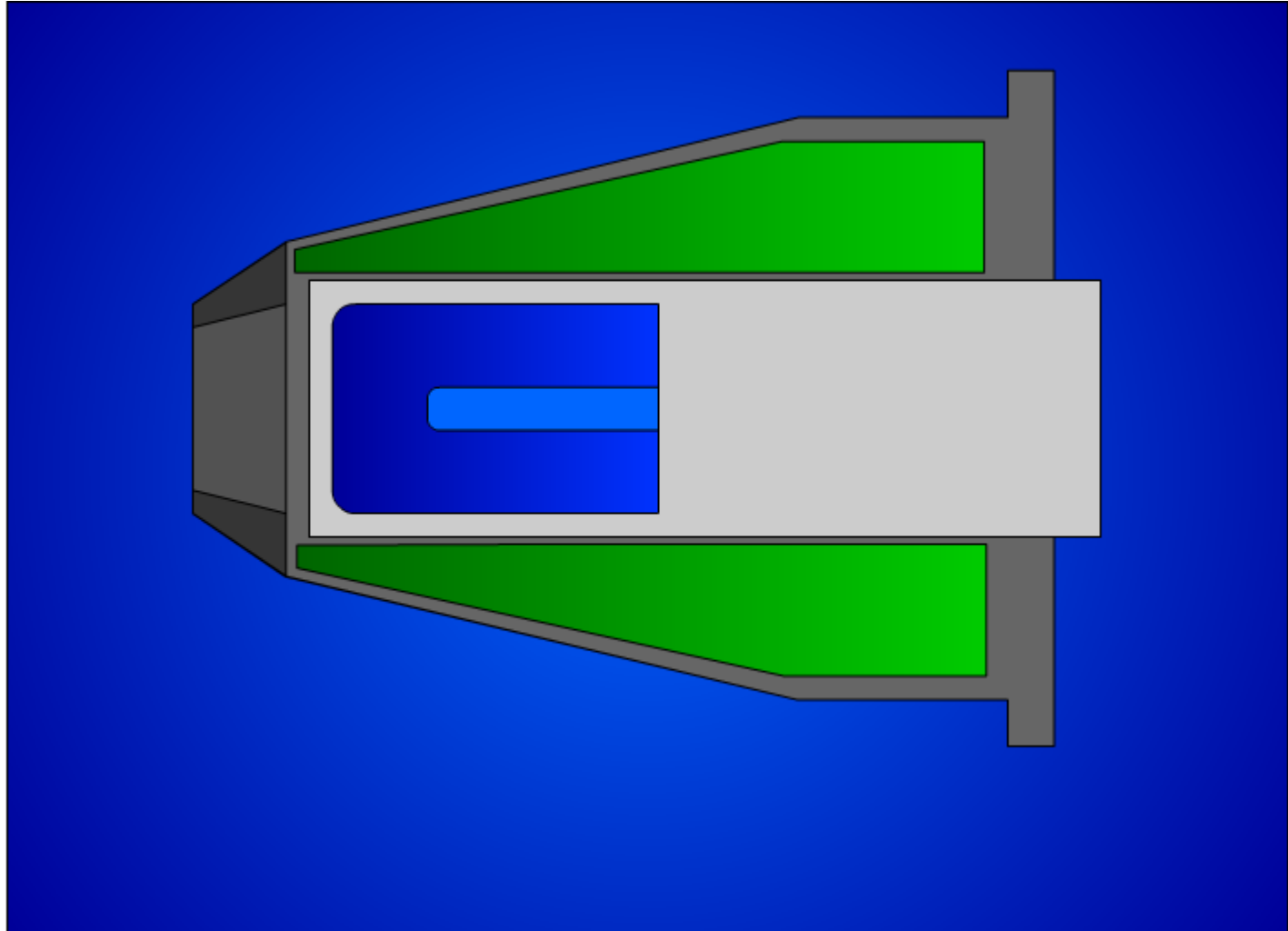
- Gamma-ray tracking
- TMR EU collaboration
- AGATA**



Typical Ge Detectors for observing gamma-rays



The scattering problem...



Compton Shielded Ge

$$\epsilon_{\text{ph}} \sim 10\%$$

$$N_{\text{det}} \sim 100$$

$$\Omega \sim 40\%$$

$$\theta \sim 8^\circ$$

large opening angle
means poor energy
resolution at high
recoil velocity.

Problems: wasting scattered gammas, solid angle

Solutions: track the scattered gammas in a Ge shell with no solid angle wasted with shields.

Ge Tracking Array

$$\epsilon_{\text{ph}} \sim 50\%$$

$$N_{\text{det}} \sim 100$$

$$\Omega \sim 80\%$$

$$\theta \sim 1^\circ$$

Combination of:

- segmented detectors
- digital electronics
- pulse processing
- tracking the γ -rays

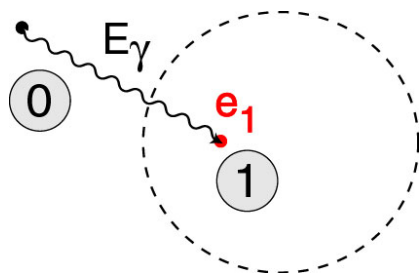
~ 100 keV

~1 MeV

~ 10 MeV

γ-ray energy

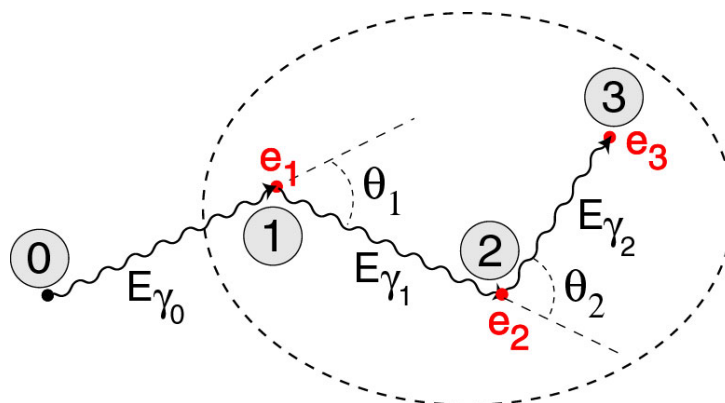
Photoelectric



Isolated hits

Probability of interaction depth

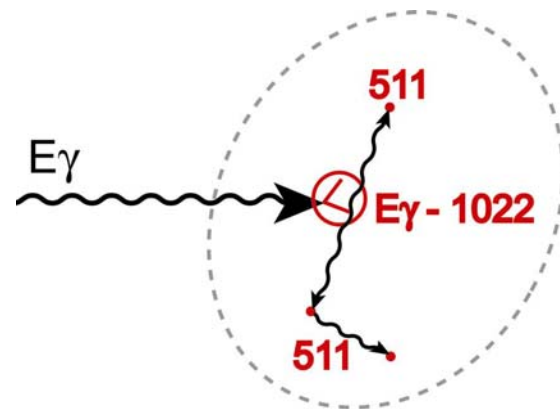
Compton Scattering



Angle/Energy

$$E_{\gamma'} = \frac{E_{\gamma}}{1 + \frac{E_{\gamma}}{m_0 c^2} (1 - \cos\theta)}$$

Pair Production

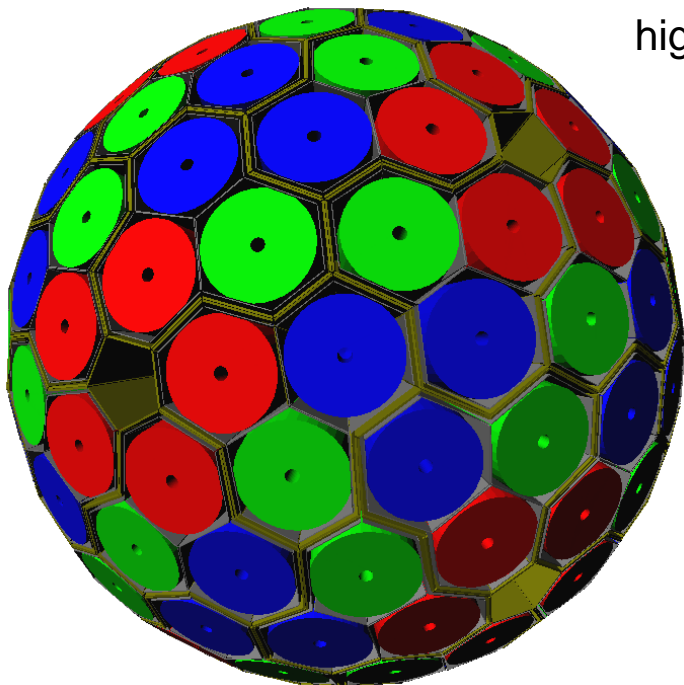


Pattern of hits

$$E_{1st} = E_{\gamma} - 2 mc^2$$

Reconstruction efficiencies are limited by :
Position resolution; Short range scattering; Compton profile.

4π γ -array for Nuclear Physics Experiments at European accelerators providing radioactive and high-intensity stable beams



Main features of AGATA

Efficiency: 40% ($M_\gamma=1$) 25% ($M_\gamma=30$)
today's arrays ~10% (gain ~4) 5% (gain ~1000)

Peak/Total: 55% ($M_\gamma=1$) 45% ($M_\gamma=30$)
today ~55% 40%

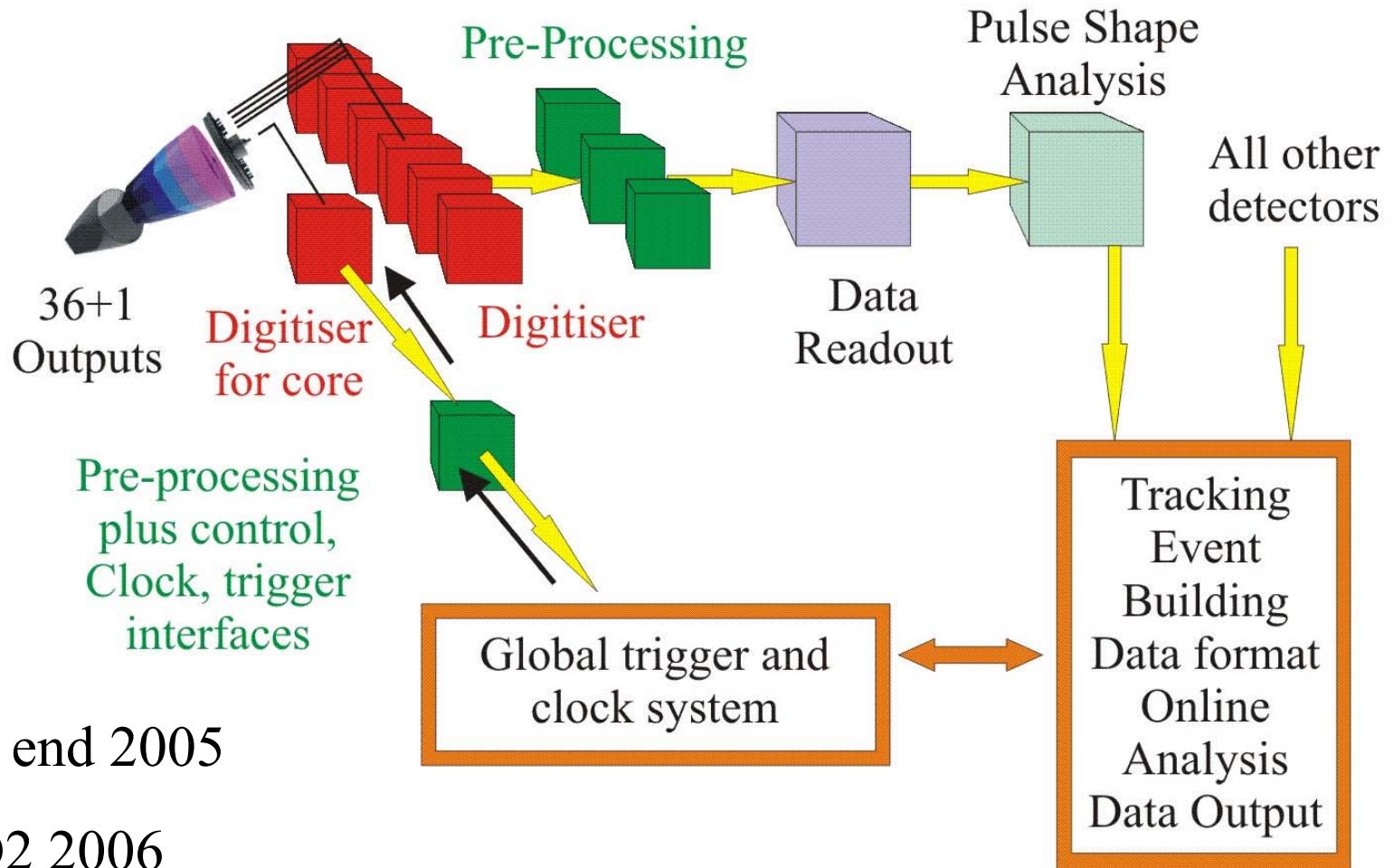
Angular Resolution: $\sim 1^\circ \rightarrow$
FWHM (1 MeV, $v/c=50\%$) ~ 6 keV !!!
today ~ 40 keV

Rates: 3 MHz ($M_\gamma=1$) 300 kHz ($M_\gamma=30$)
today 1 MHz 20 kHz

- 180 large volume 36-fold segmented Ge crystals in 60 triple-clusters
- Digital electronics and sophisticated Pulse Shape Analysis algorithms allow
- Operation of Ge detectors in position sensitive mode \rightarrow γ -ray tracking



Schematic of the Digital Electronics and Data Acquisition System for AGATA



Prototypes end 2005

Test Q1, Q2 2006

15 Ge (555 channel) demonstrator 2007

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- Examples of FEE- EXL recoil detector
- FEE ASIC meeting report
- Common FEE architecture

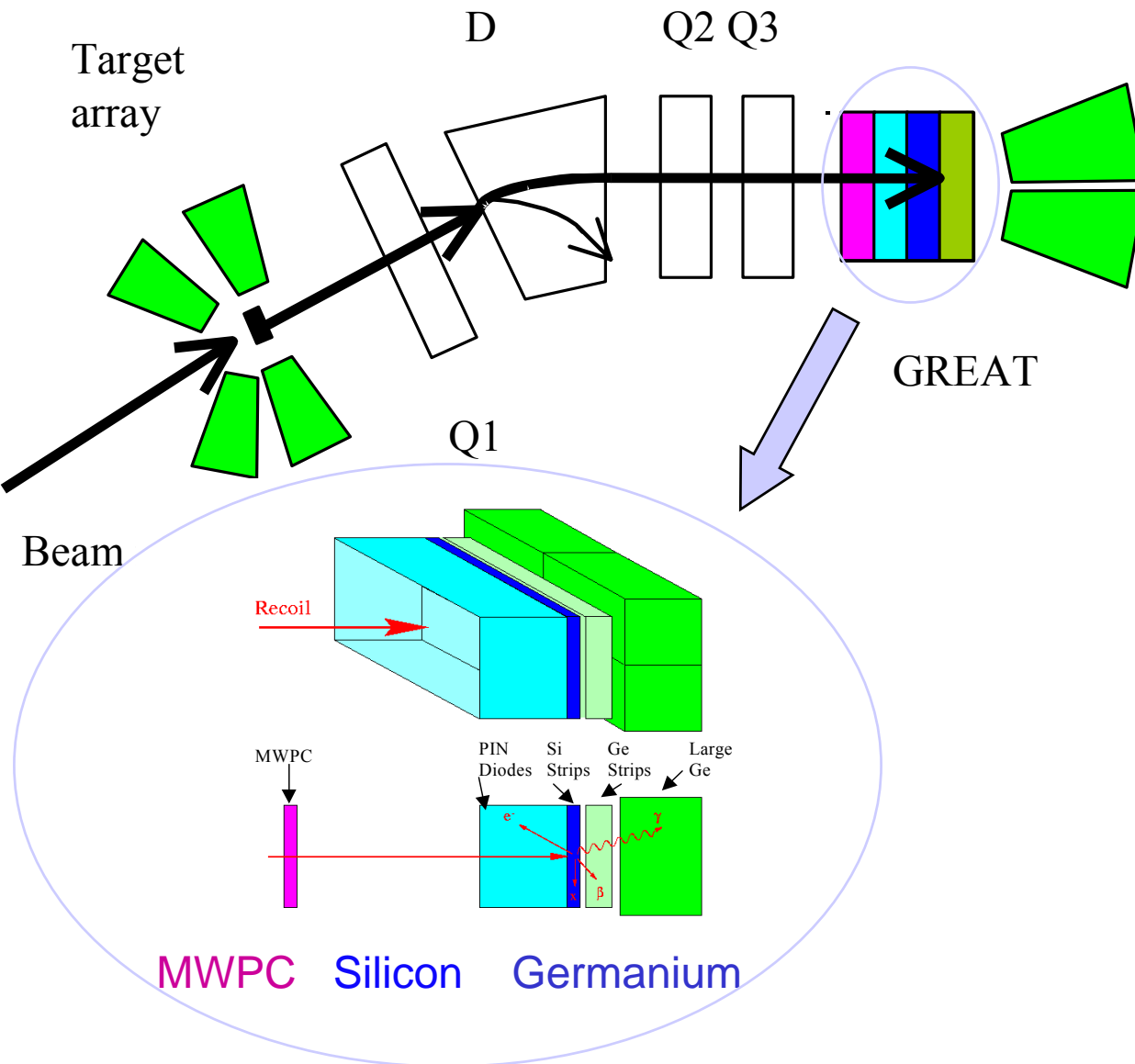
- **Detector Requirements:**
 - Energy measurement
 - Energy loss (ΔE)
 - Full energy (E)
 - Tracking
 - Beam
 - recoil fragments
 - Reaction products
 - Charge
 - Mass
 - Time of flight
- Detecting proton, alpha, LCP, or heavy ions

- **Detector Types:**
 - Si (DSSD, microstrip) SiLi
 - Scintillators (various from basic to exotic)
 - Gas
 - ionisation chambers,
 - PPAC,
 - MWPC
 - micropattern (GEM, micromegas, ...)
 - Active Target/TPC
 - magnetic spectrometers for selection

- FEE Requirements:
 - Low Noise
 - Low threshold (e.g. tiny signals from thin Si)
 - Good accuracy, low drift, good timing
 - Very large dynamic range

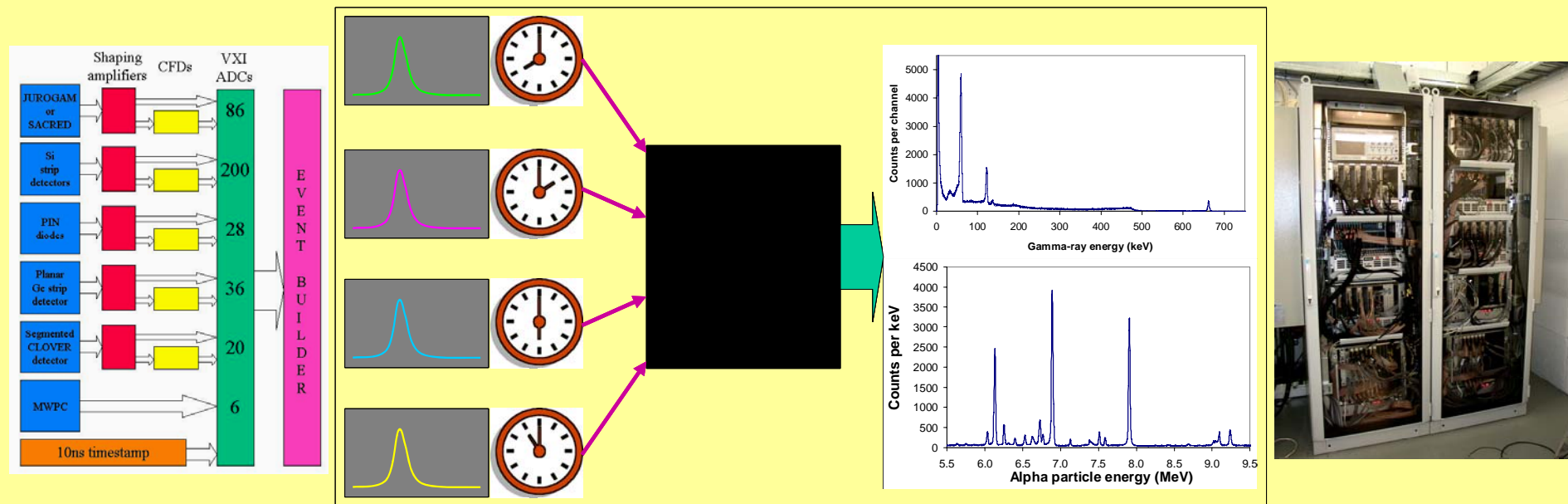
**Gamma
Recoil
Electron
Alpha
Tagging**

Spectrometer



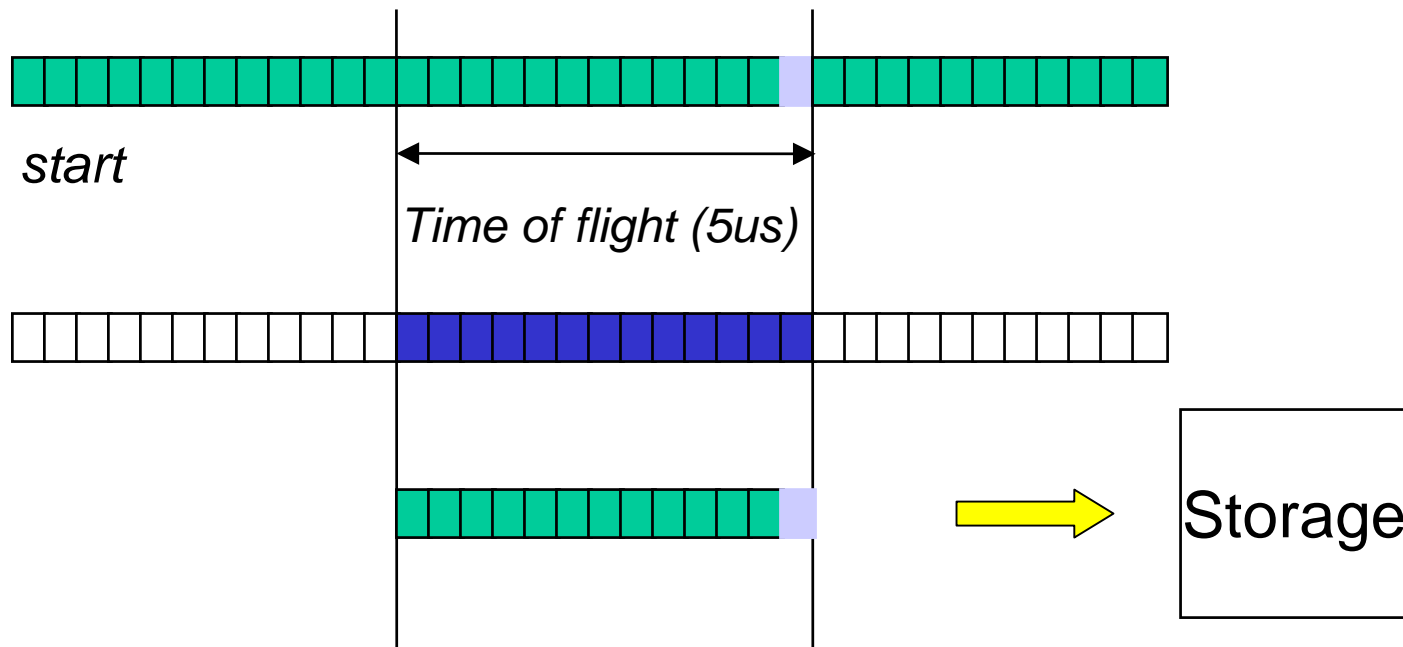
Total Data Readout

Novel triggerless data acquisition eliminates common dead time



- Recoil data from focal plane
- Ge data from target array
- Time window

Time-ordered input data stream

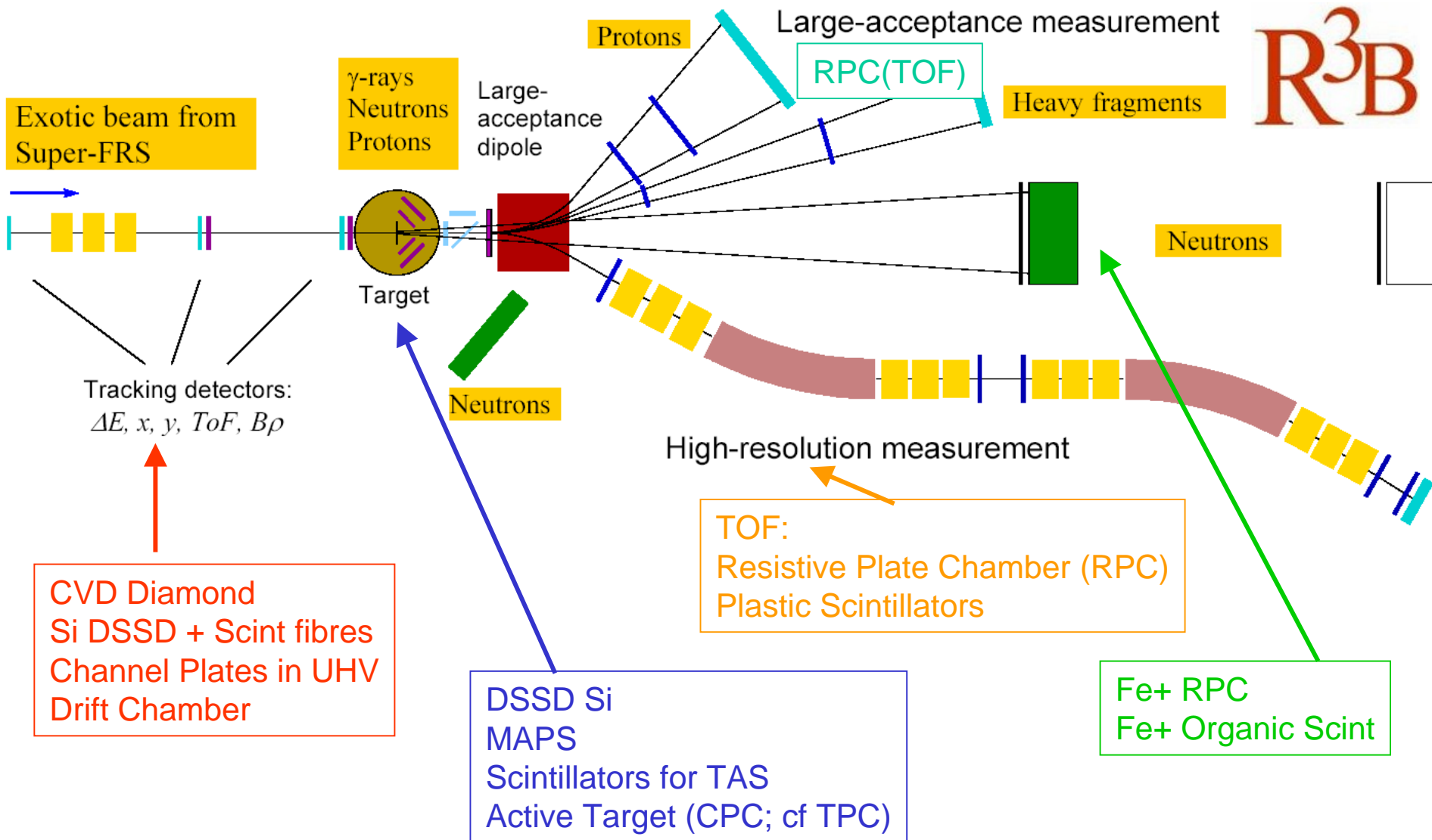


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The high-energy branch of the Super-FRS:

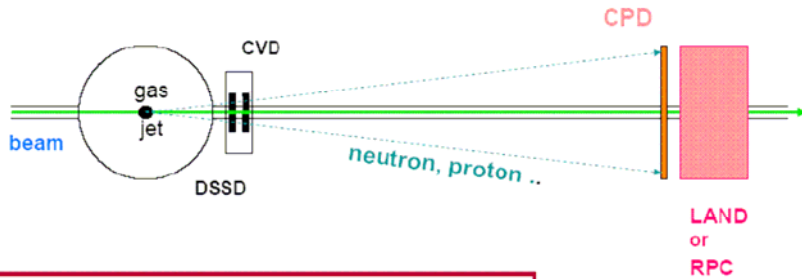
A universal setup for kinematical complete measurements of

Reactions with **R**elativistic **R**adioactive **B**eams



Kinematically complete measurements:

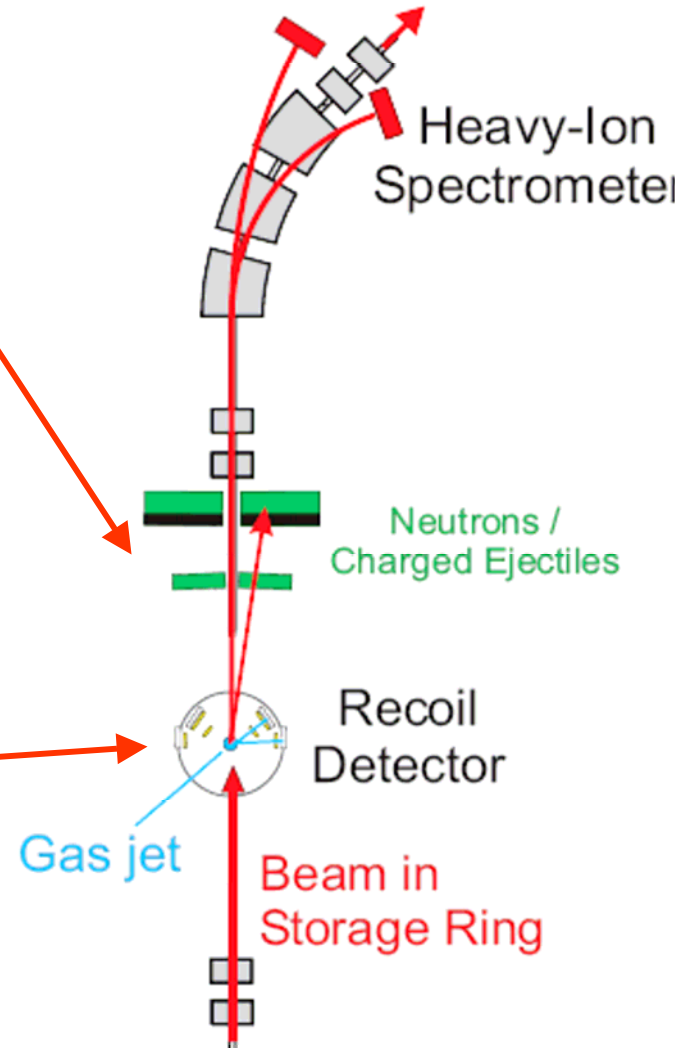
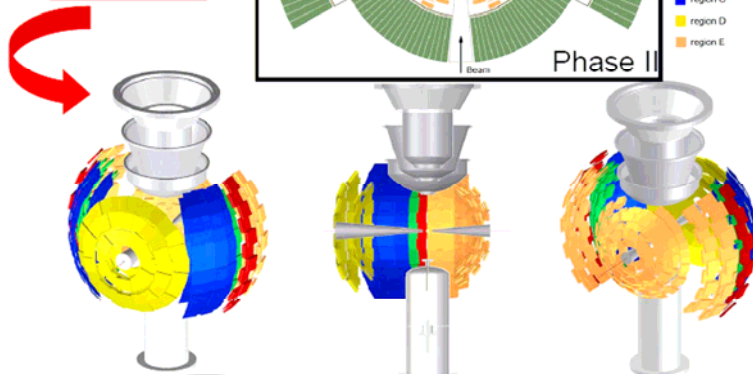
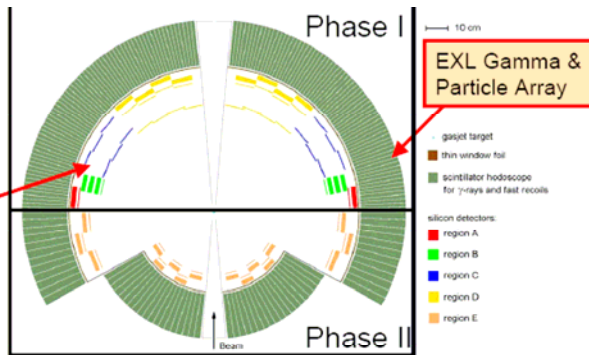
- detection of forward light particles emitted from the projectile (momenta measured)
- excitation energy of projectile residue, momentum (angular) correlations



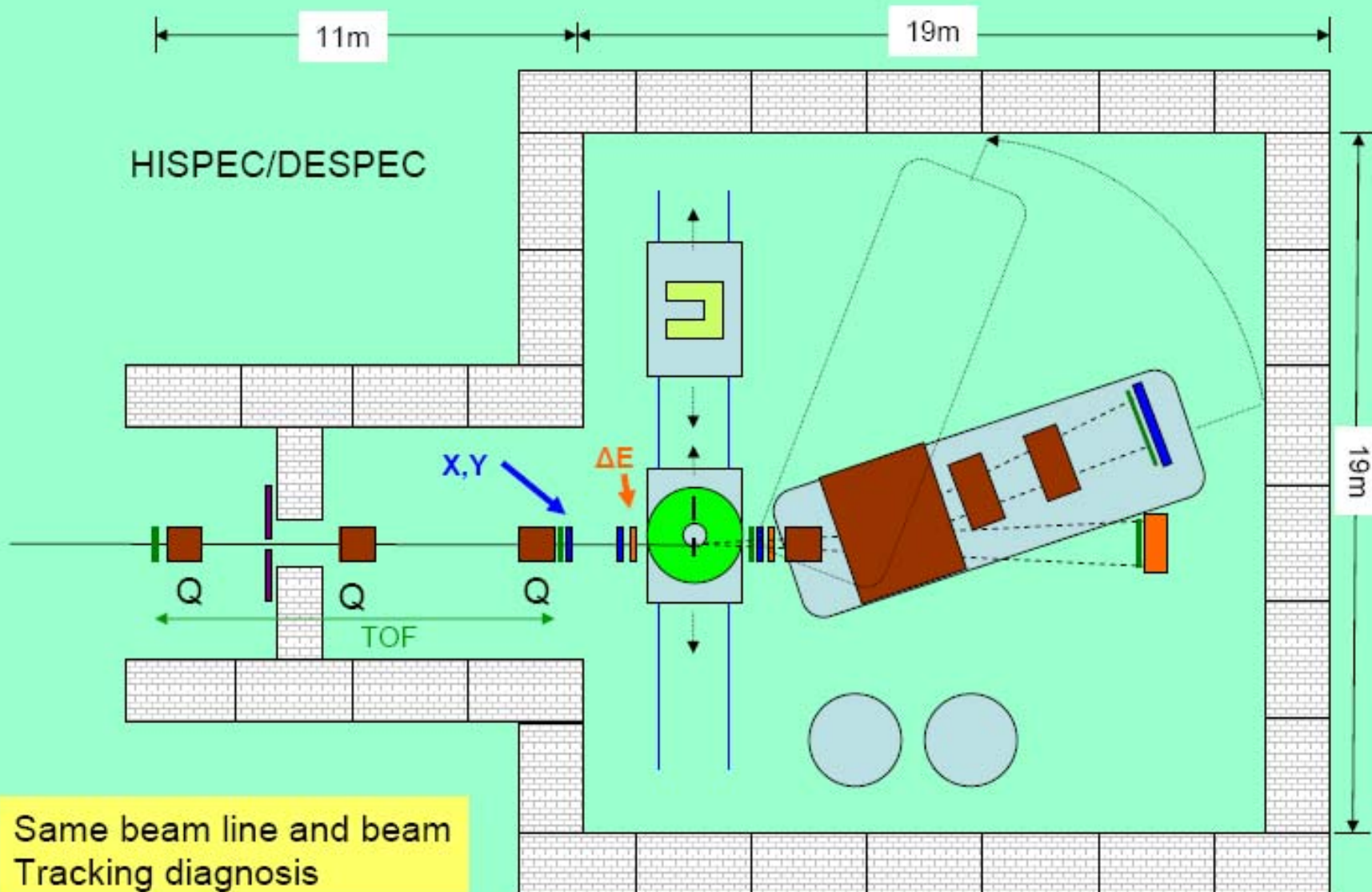
- High-resolution TOF and position measurements
- Full solid angle (forward focus)
- Phase I (LAND) and Phase II (RPC)

**EXL
Recoil & Gamma
Array**

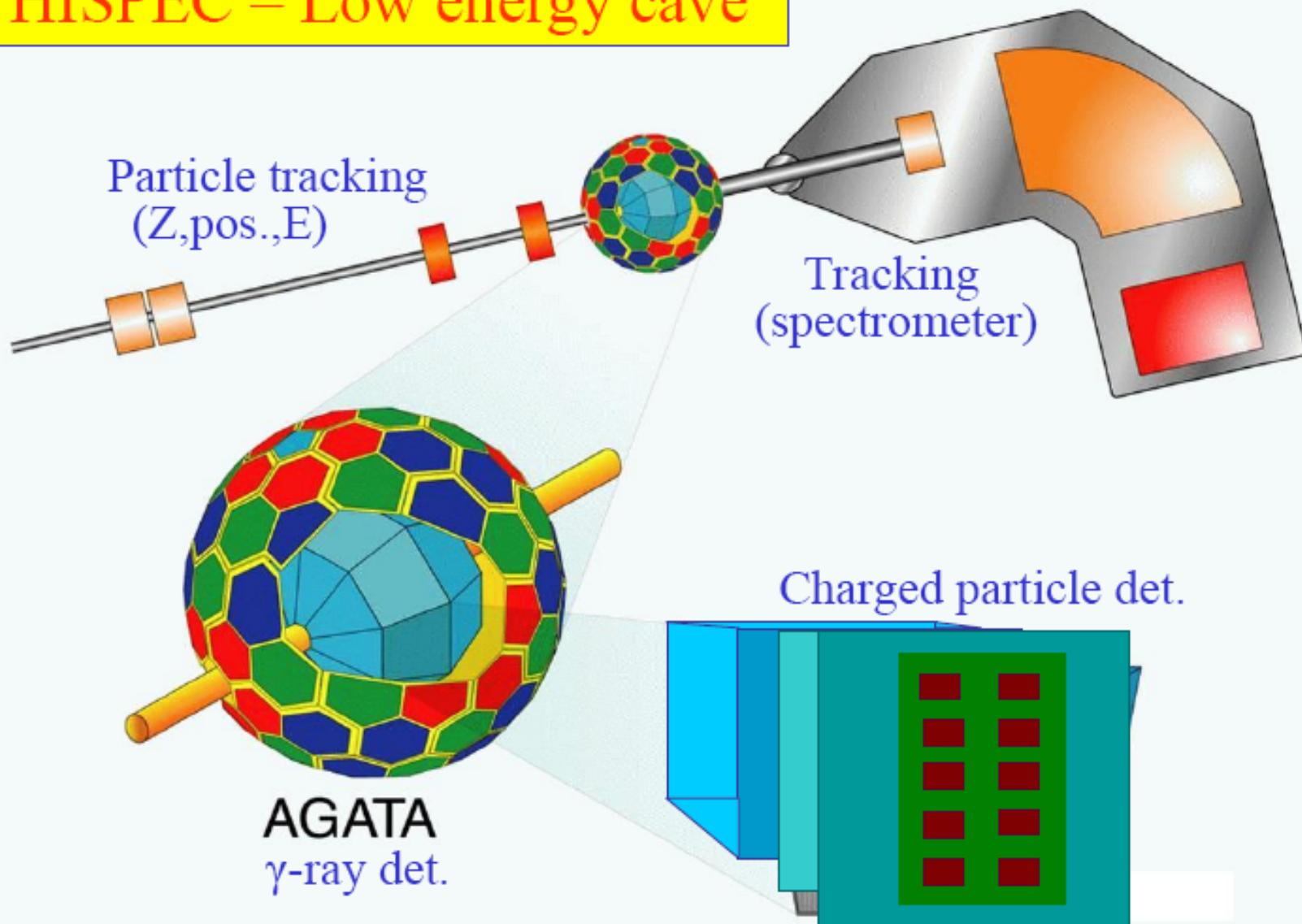
**EXL Silicon
Particle Array**



HISPEC DESPEC

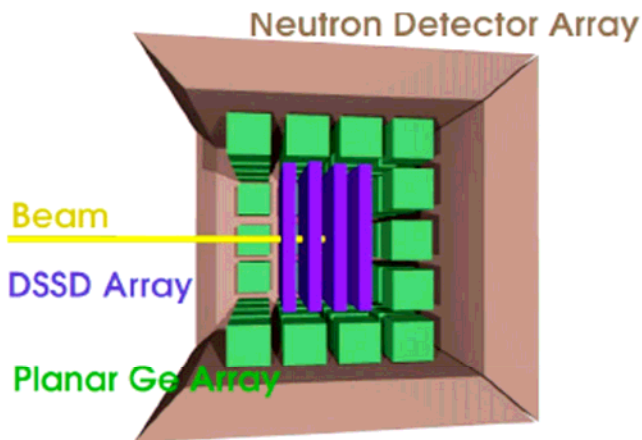


HISPEC – Low energy cave

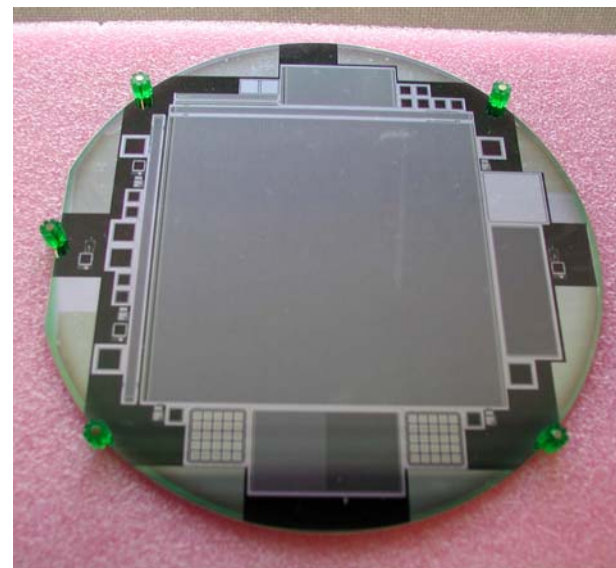


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Concept and the detector



- Super FRS Low Energy Branch (LEB)
- Exotic nuclei – energies $\sim 50\text{-}150\text{MeV}/u$
- Implanted into multi-plane DSSD array
- **Implant - decay correlations**
- **Multi-GeV DSSD implantation events**
- Observe subsequent p , $2p$, α , β , γ , βp , βn ... decays
- Measure half lives, branching ratios, decay energies ...



- 6" wafer-10cm x 10cm area
- 1mm wafer thickness
- Integrated components
 - a.c. coupling
 - polysilicon bias resistors
 - ... important for ASICs
- Series strip bonding (3 together)

DSSD Segmentation

We need to implant at high rates *and* to observe implant – decay correlations for decays with long half lives.

DSSD segmentation ensures average time between implants for given x,y quasi-pixel \gg decay half life to be observed.

- Implantation profile

$$\sigma_x \sim \sigma_y \sim 2\text{cm}$$

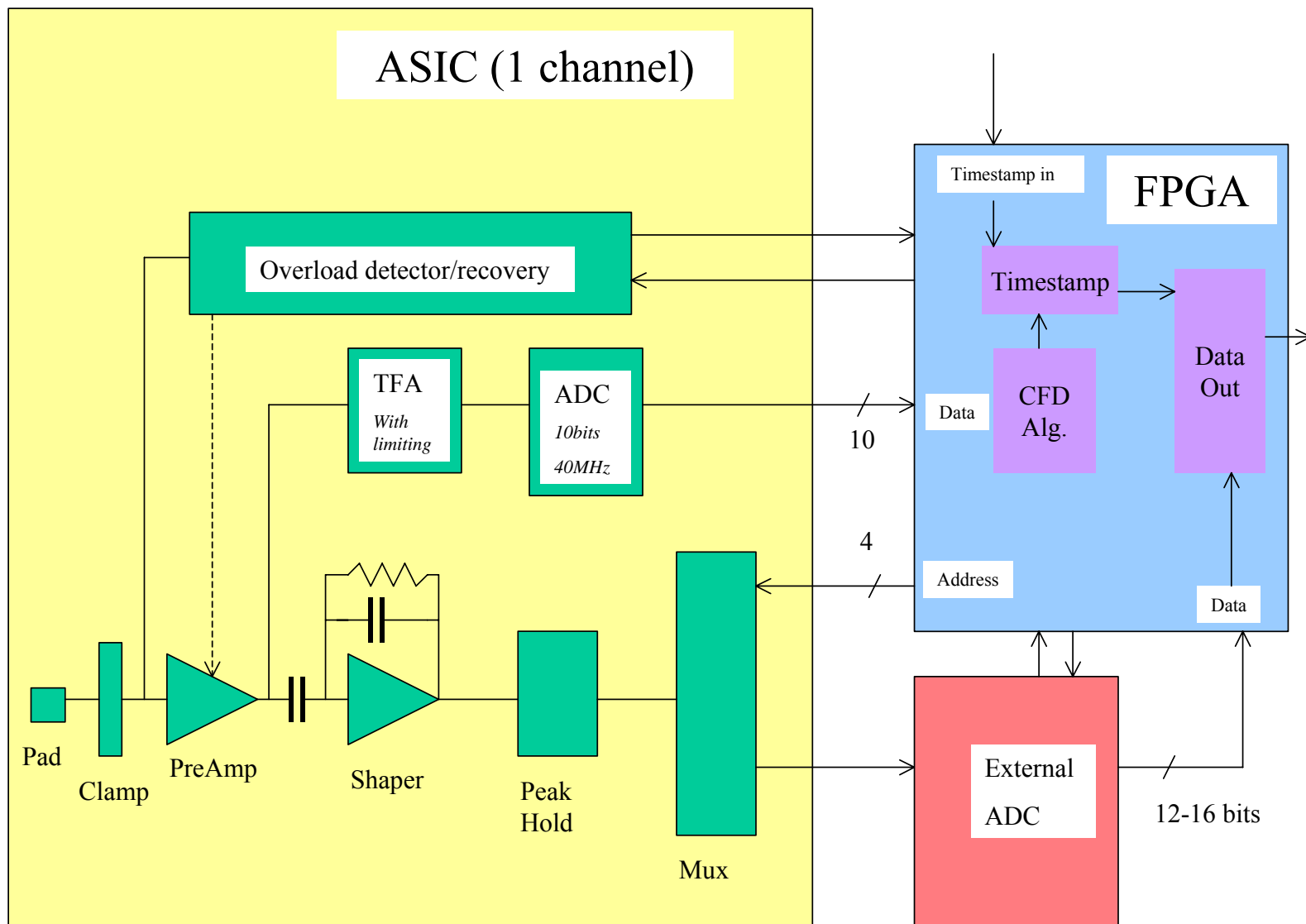
$$\sigma_z \sim 1\text{mm}$$

- Implantation rate (8cm x 24cm) \sim 10kHz, \sim kHz per isotope (say)
- Longest half life to be observed \sim seconds

Implies quasi-pixel dimensions \sim 0.5mm x 0.5mm

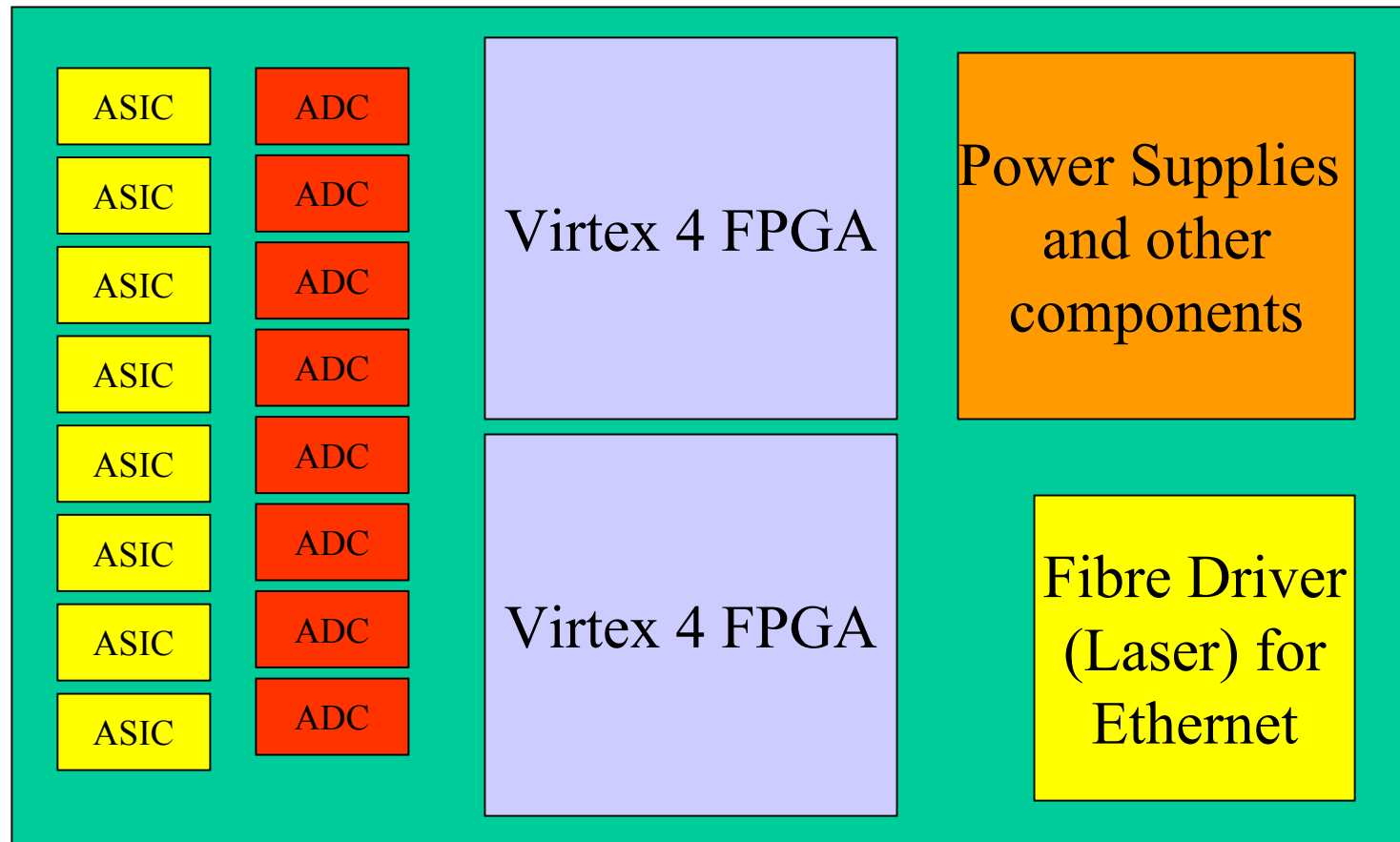
Segmentation also has instrumentation performance benefits

1 of the 16 channels in the DESPEC Implantation Detector ASIC (shown with external FPGA and ADC)



16 ch ASIC 16 bit ADC

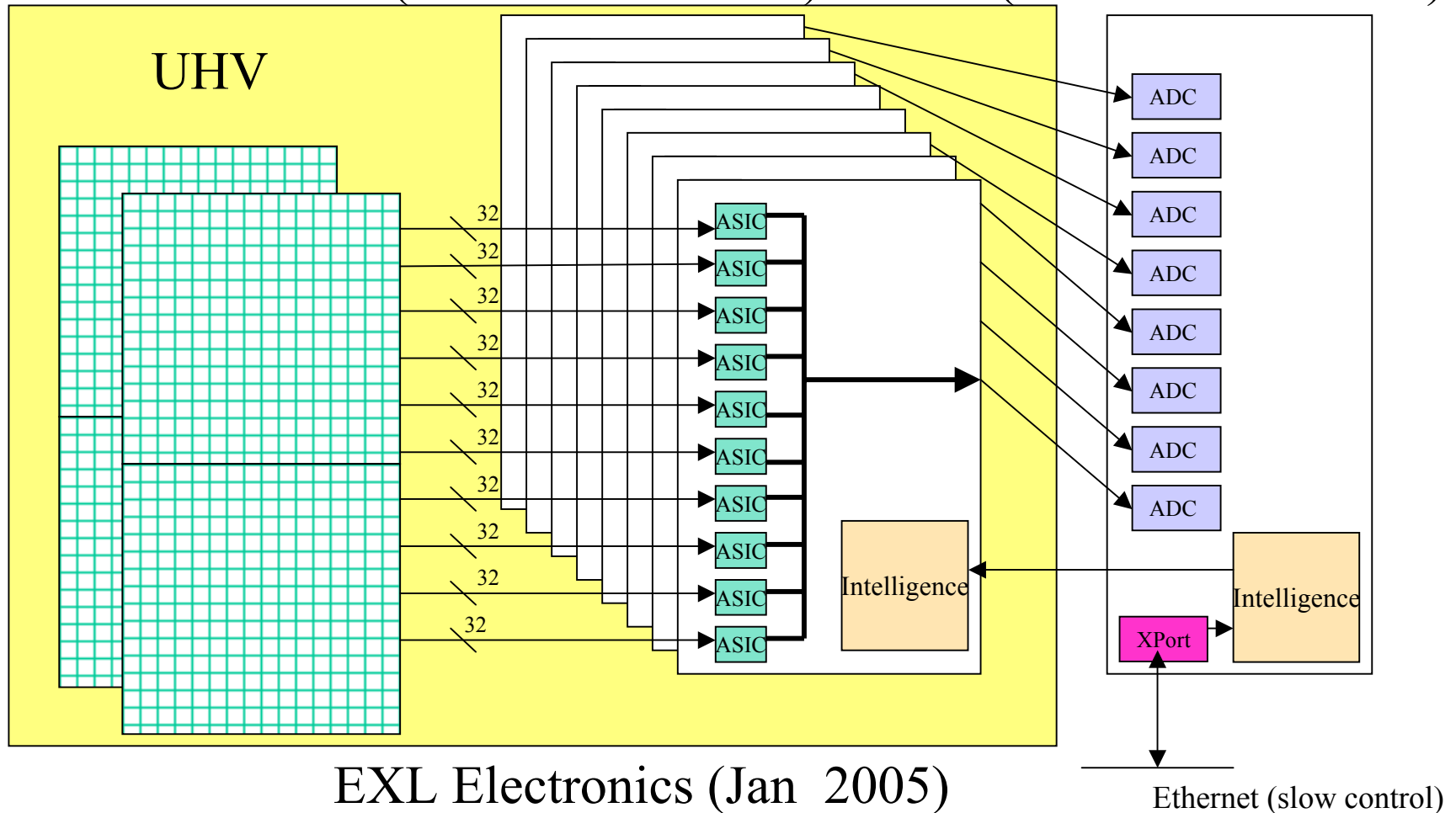
128 detector signals in; 1 data fibre out



Estimated size: 80x220mm,
Estimated power 25W per 128ch (800W total)

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Detectors-	ASIC cards- approx	ADC cards- 1750
560000 channels	17500 ASICs on 1750 cards	ADCs on 219 cards
DSSD and SiLi	(32 channels/ASIC)	(320 channels/ADC)



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Small group (CCLRC & CEA Saclay) discussed EXL, R3B DESPEC, HISPEC and SPIRAL 2.

Found 3 FEE ASICs needed (so far) for NUSTAR:

1. Fast recovery after implantation of ion in DSSD Si to measure decay in the same pixel. (DESPEC)
2. EXL CsI calorimeters covering energy range 300keV to 500MeV. 13k channels needed.
3. EXL/R3B Si strip and SiLi detector ASIC. Normal Si processing chain of preamp, shaper, mux or ADC, timing. Add PSD too. Maybe 2 ASIC solution?

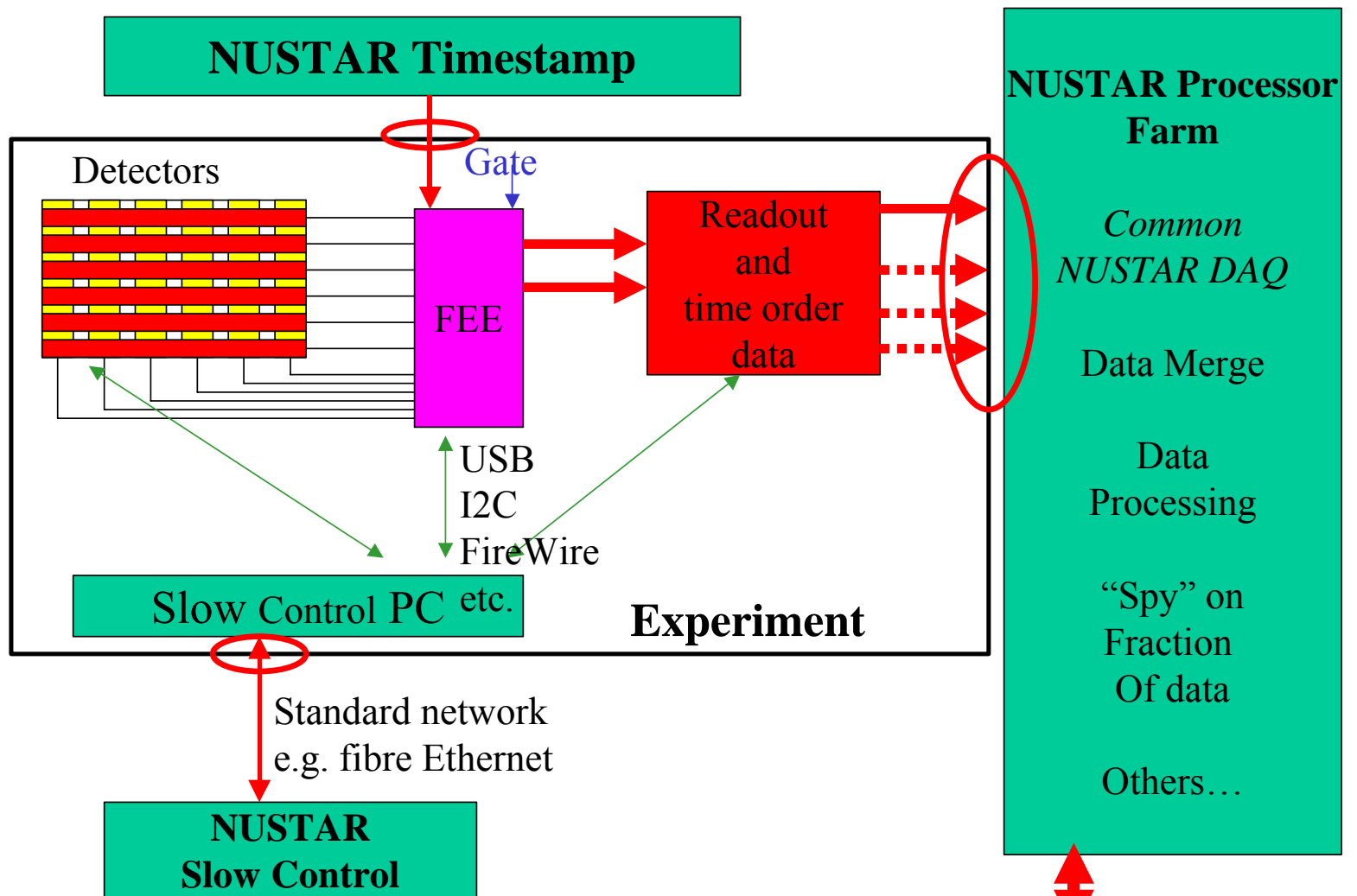
Why collaborate on ASICs and FEE?

- Limited ASIC manpower- don't waste it.
- Limited FEE and DAQ manpower too.
- Avoid duplication of design effort where 2 experiments need a similar ASIC
- Common software for slow control and DAQ (reduced software effort for experiments)
- Compatibility between experiments
- Independent design reviews (increase the probability of a working ASIC).

Actions/decisions:

1. Up to Jun 2006: Make physicists aware of these discussions about ASICs and collect the outline specs as they emerge from draft TDRs to look for synergy.
2. Find NUSTAR ASIC designers and talk to them!
3. ASIC Technology lifetimes- the NP (& HEP) market is so tiny as to have no influence on the lifetime of ASIC processes. Just use best guess. (CCLRC & CEA both use AMS 0.35um CMOS process for analogue.)
4. ASIC design cycle (3 iterations) takes 3-4 years. Start soon with 12 months of consultation and specification.
5. **Design a system, not just an ASIC (or FEE card).**

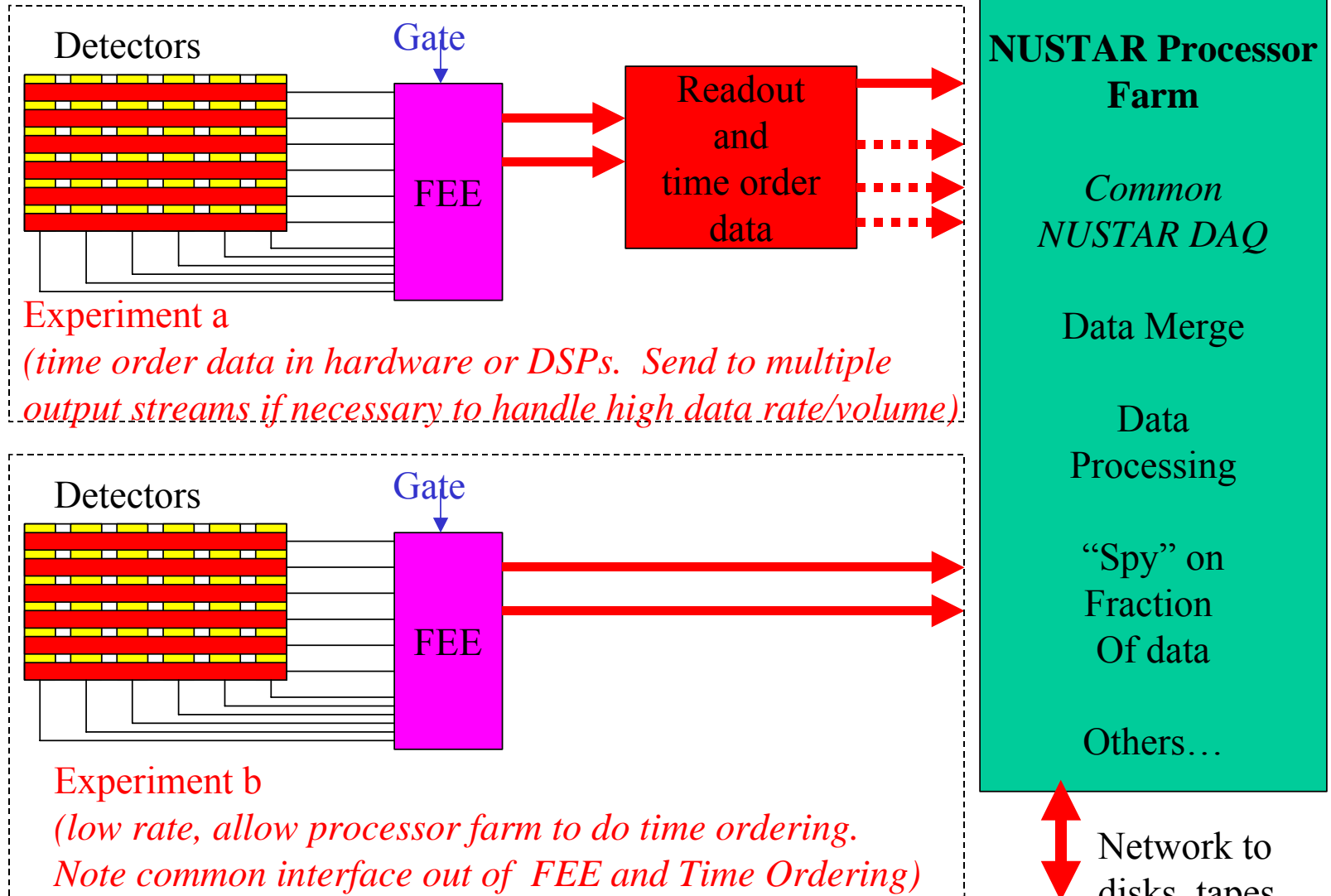
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One experiment showing 3 standard interfaces to the NUSTAR Slow Control, Timestamp and DAQ

Network to disks, tapes, Grid etc.

Flexibility from standard interfaces

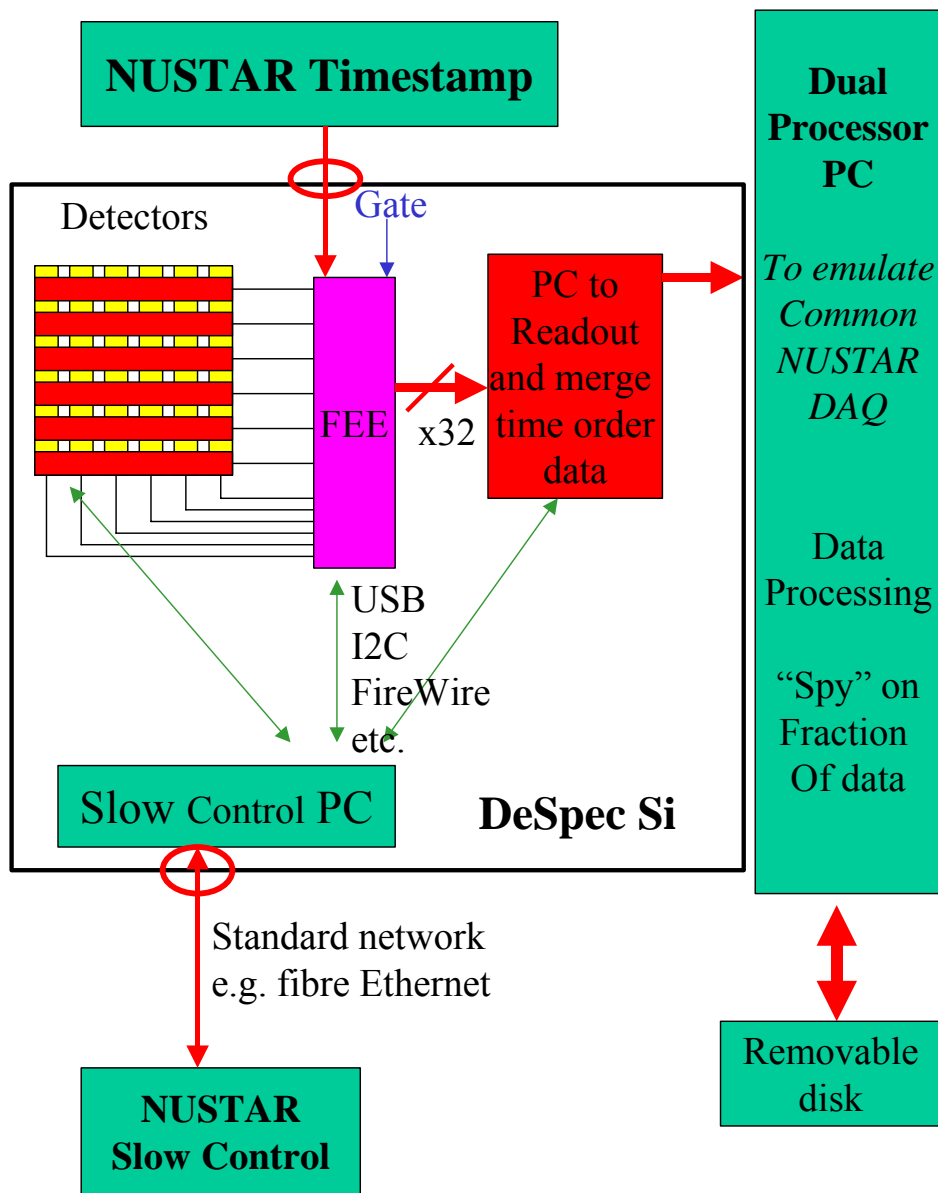


Experiment a
(time order data in hardware or DSPs. Send to multiple output streams if necessary to handle high data rate/volume)

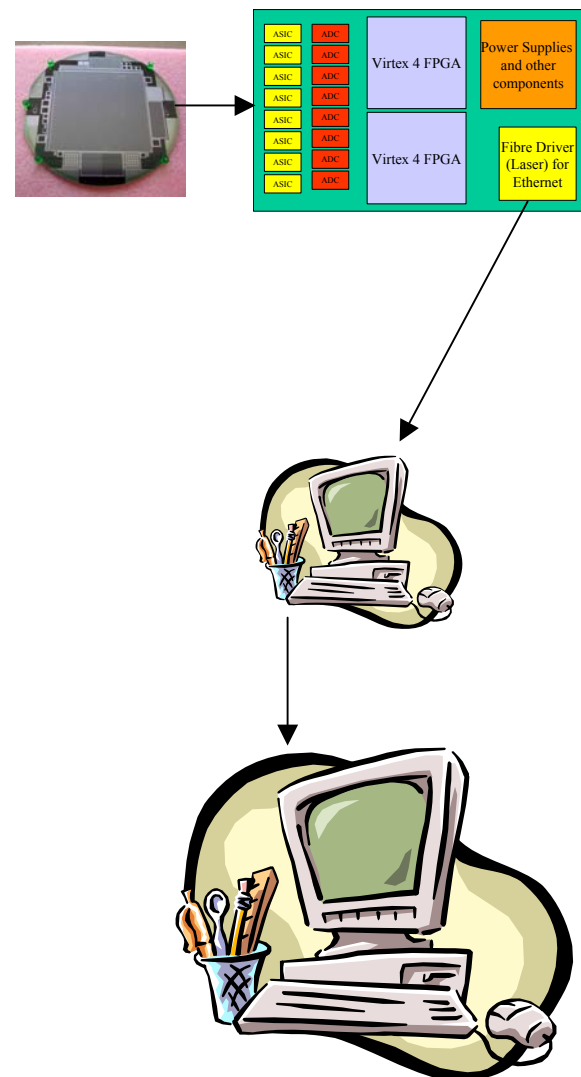
Experiment b
(low rate, allow processor farm to do time ordering. Note common interface out of FEE and Time Ordering)

*Optional bypassing of time ordering stage for low rate experiments.
The advantage of a common interface standard (e.g. (10)Gbit Fibre)*

- Common clock distribution and timestamp control method (synchronisation, heartbeats and resets)
- Data output format- 1st generation use fibre 10G Ethernet?
- Slow control- common interface (Ethernet/Soap???)
- On board processing- too early for device, maybe can now choose Type= FPGA and family=Xilinx?
- Power: 48V with local conversion
- Board size and format- doesn't matter (match to detector?)



DESPEC example



- Wide variety of requirements in NUSTAR.
 - Some (e.g. LASPEC) need just a crate of NIM or CAMAC and PC, no need for common FEE or DAQ.
 - Large systems e.g. EXL plans over 0.5M channels- should consider common DAQ and FEE.
- Large systems- forced to use ASICs by space constraints and cost (e.g. DESPEC, EXL).
- Limited resources so look for common ground in
 - FEE
 - ASICs
 - DAQ
- Design a **system**; don't work in isolation and hope!

Presentation includes pictures from other people.

Thanks to:

- John Simpson (CCLRC),
- Tom Davinson (University of Edinburgh)
- Robert Page (University of Liverpool)
- Roy Lemmon (CCLRC)
- Marielle Chartier (University of Liverpool)

NUSTAR FEE diagrams result from discussions with

- Haik Simon (GSI)
- Lolly Pollacco (CEA Saclay)
- Roy Lemmon (CCLRC)