Building Blocks for FEE
(as supported by TU KL)

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Outline

- Building blocks for FEE available as IP-cells of TU KL

- Proposed flexible PreAmp-Filter-ADC chip;
some considerations

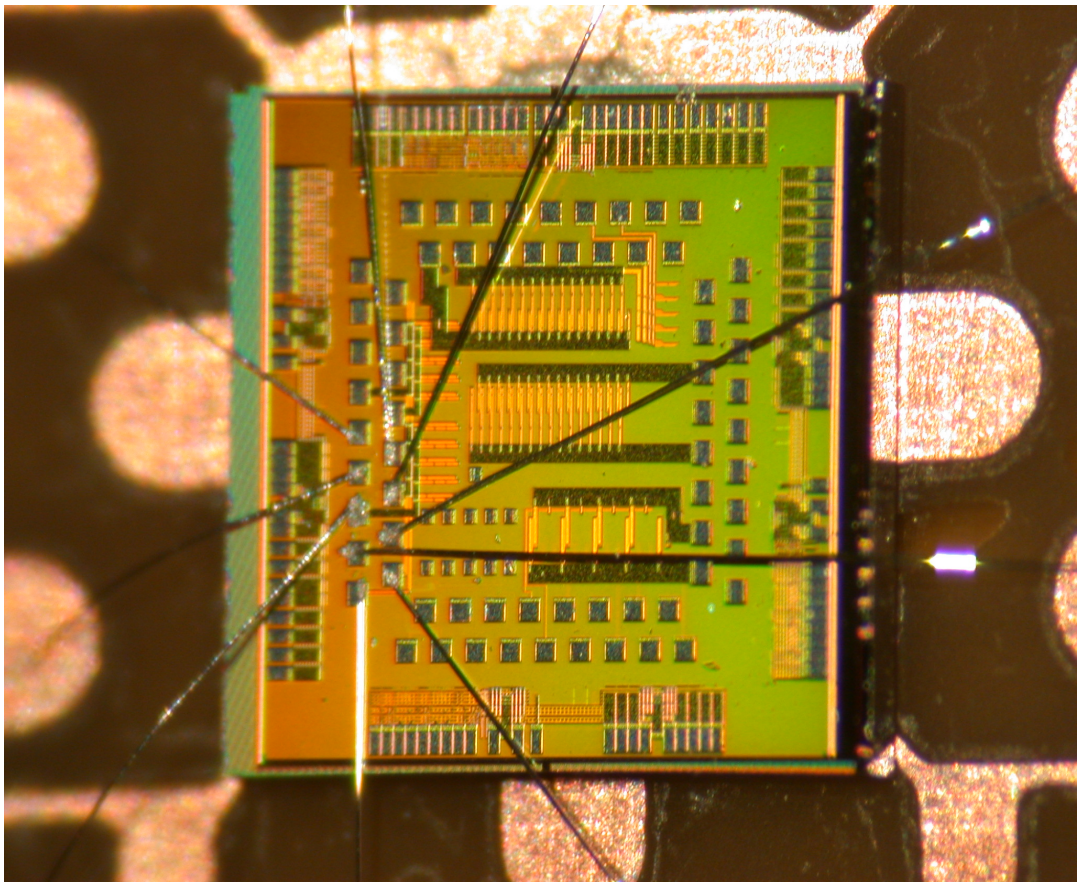
- Motivation for a scaleable Low Power ADC up to 100MS/s
(continued by the presentation of D. Muthers)

- Motivation for low jitter Clock and data recovery units
(continued by the presentation of S. Tontisirin)

- Summary

Low Power LVDS Tx/Rx Testchip 0.12µm CMOS

(including different 4/8/16 Bit I/O- banks)



- **Vdd_Core: 1.5V**
- **Vdd_I/O: 3.3V**

- **Transmitter**
  Vdd: 1.5V
  Idd: 3.4 mA
  Vcom: 1.2V
  Vout,diff: 320mV
  Nom. Data rate: 625 Mb/s

- **Receiver**
  Vdd: 3.3V/1.5V
  Idd: 35µA/12µA
  Nom. Data rate: 625 Mb/s

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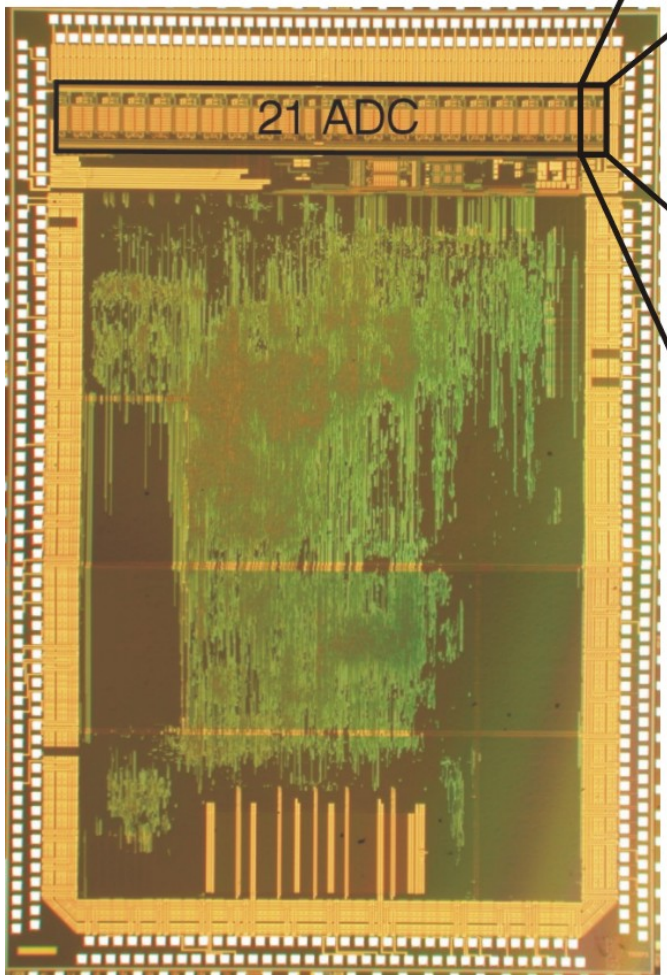
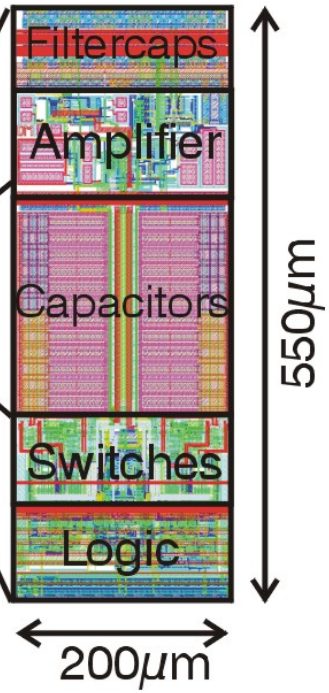
Multichannel ADC-Implementation





Cyclic ADC

10bit, 10MS/s

Power: 9.5mW

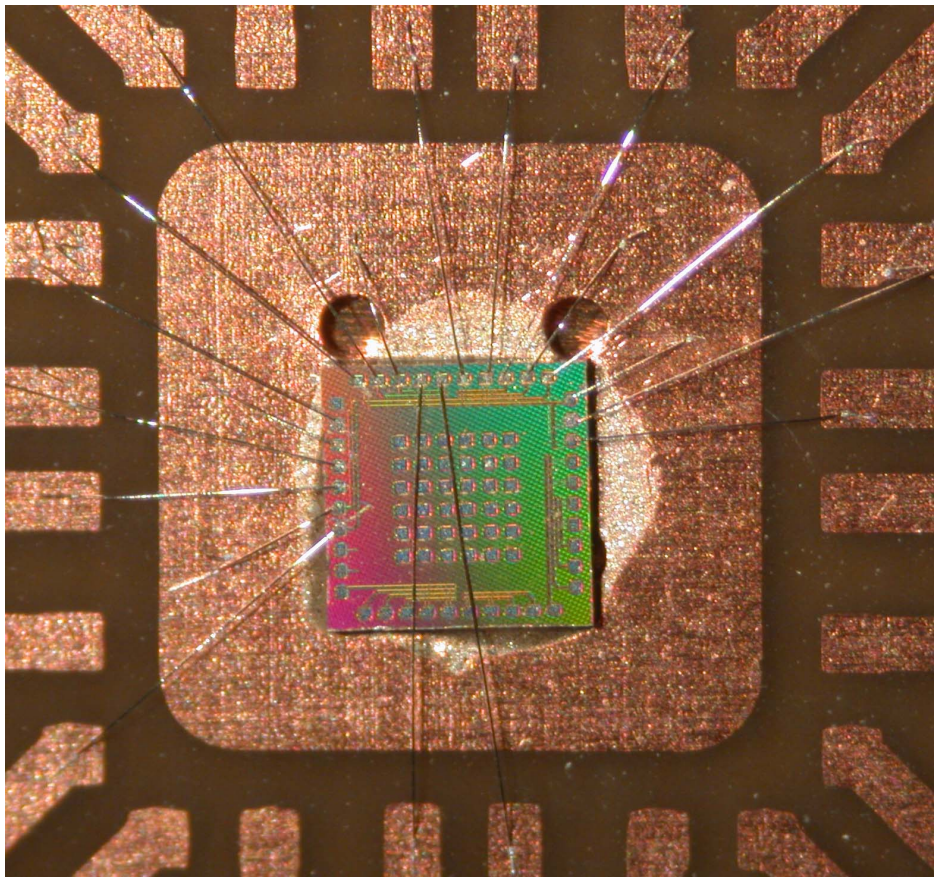
Area: 0.11mm²

0.18µm CMOS

SNR 59.2dB (1MHz signal)
ENOB 9.5bit "
SFDR 73.0dB "
THD -69.5dB "
DNL -0.4/+0.6LSB
INL -0.8 / +0.7LSB

High Speed CML/LVDS Transceiver 0.12µm CMOS

(including Pre-Emphasis Feature)



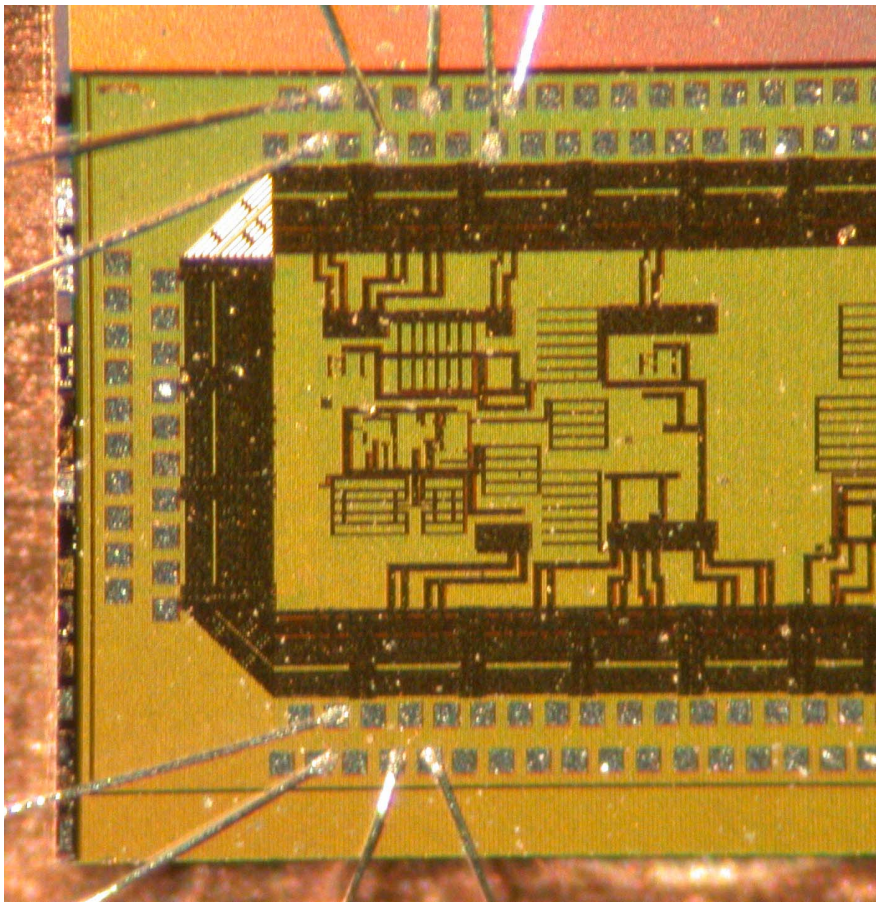
- Vdd_core: 1.2V
- Vdd_I/O: 2.5V

- CML Tx
  Vdd: 1.2V
  Idd: 18 mA
  Vout,diff: 400mV
  Data rate: 2.5 Gbps

- CML Rx
  Vdd: 1.2V
  Idd: 3 mA
  Data rate: 2.5 Gbps

2.5 Gbit/s Transceiver Testchip 0.18µm CMOS

(east side shown, including LVDS I/O, 8b/10b Encoder, Frequency Synthesizer, Serializer, CML Transceiver, and Laser Driver)



- Vdd_core: 1.8
- Vdd_I/O: 3.3V

- Frequency Synthesizer
  (PLL based, F-ref x 5)
  Vdd: 1.2V
  Idd: 20 mA
  Fout-max. : 1.33 GHz.
  Fout-min. : 310 MHz.

- Serializer 10:1
  (half-rate clock)
  Vdd: 1.2V
  Idd: 15 mA
  Data rate: 2.5 Gbit/s

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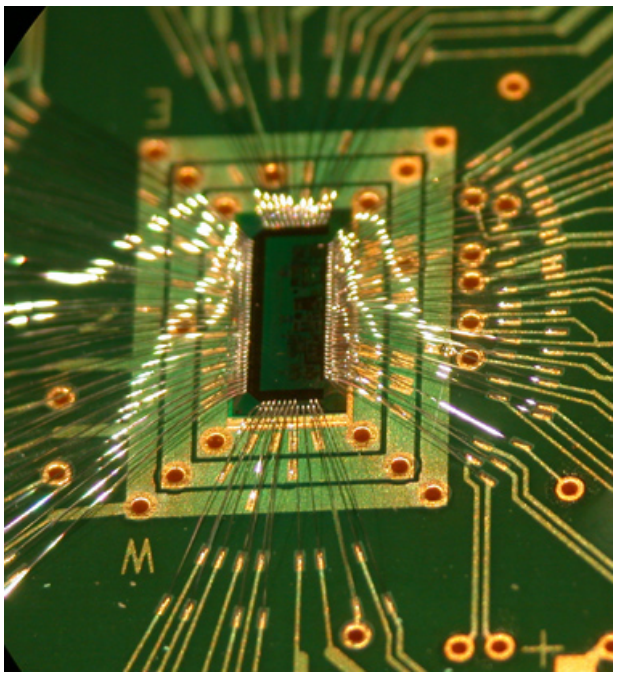
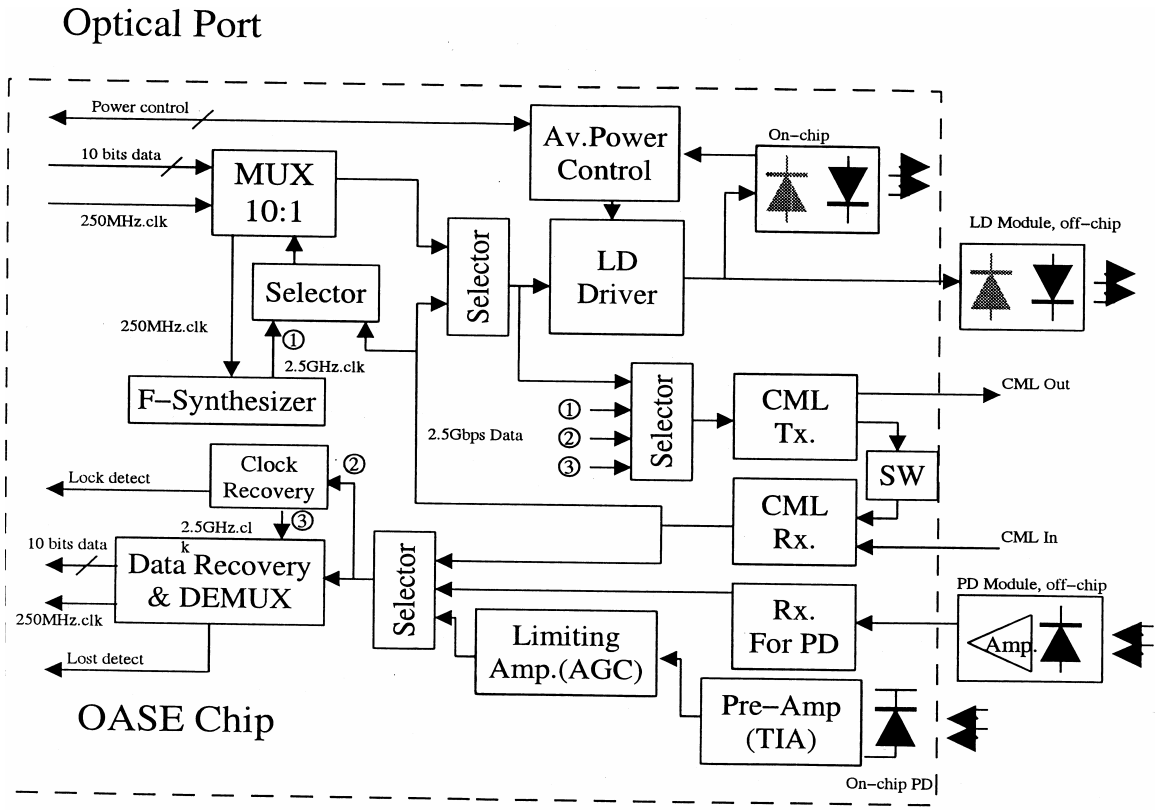
SerDes&Optical Transceiver (2.5 Gbit/s)
Analog/ HighSpeed Electronics of „OASE“ Chip





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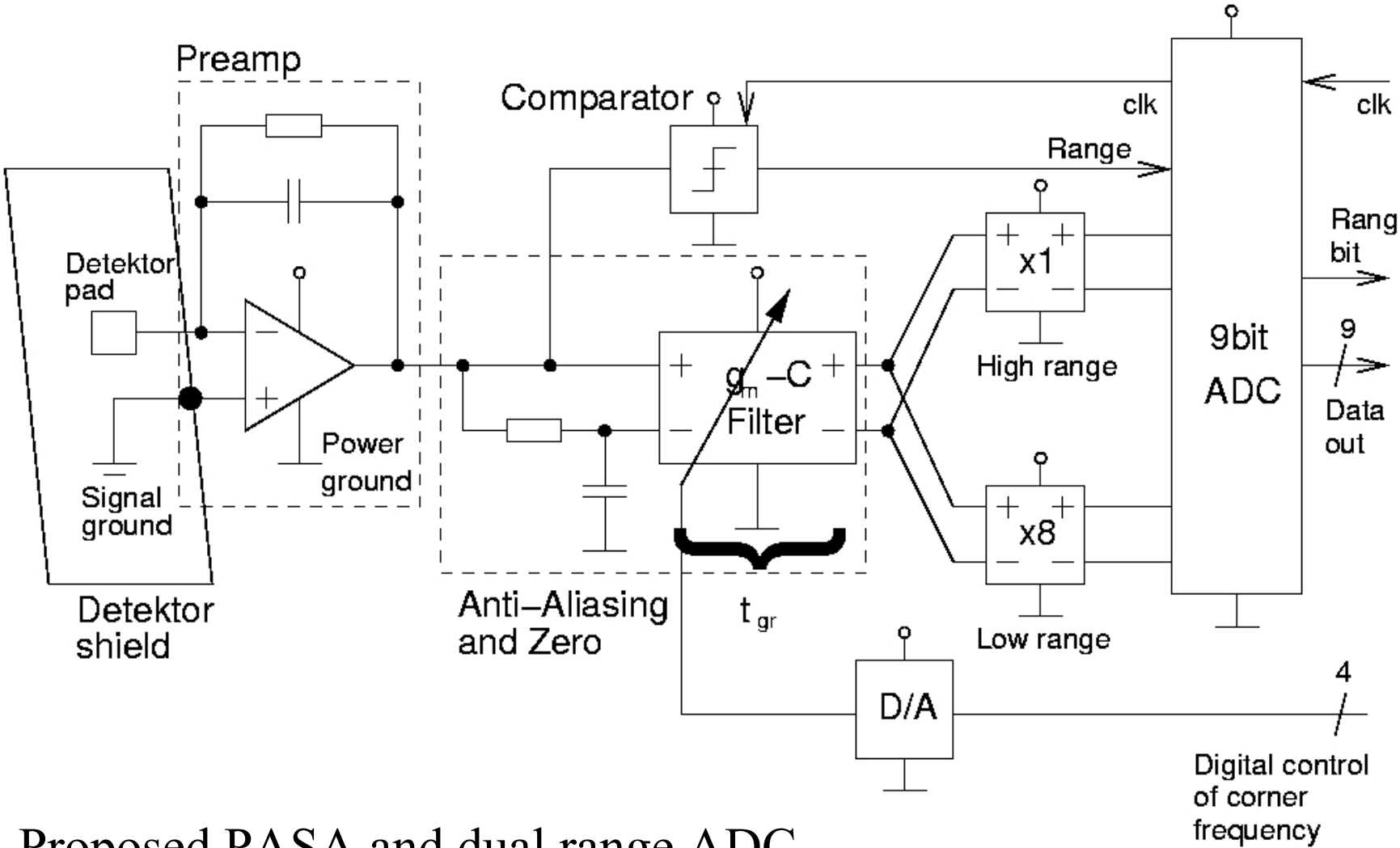


Proposed PASA and dual range ADC

Some Signal Checks with the ALICE drift chamber measured directly at an unloaded Readout Pad using a Wideband Probe and cosmic ray events

Goal is to estimate the PASA requirements and to demonstrate the advantage of differential probing

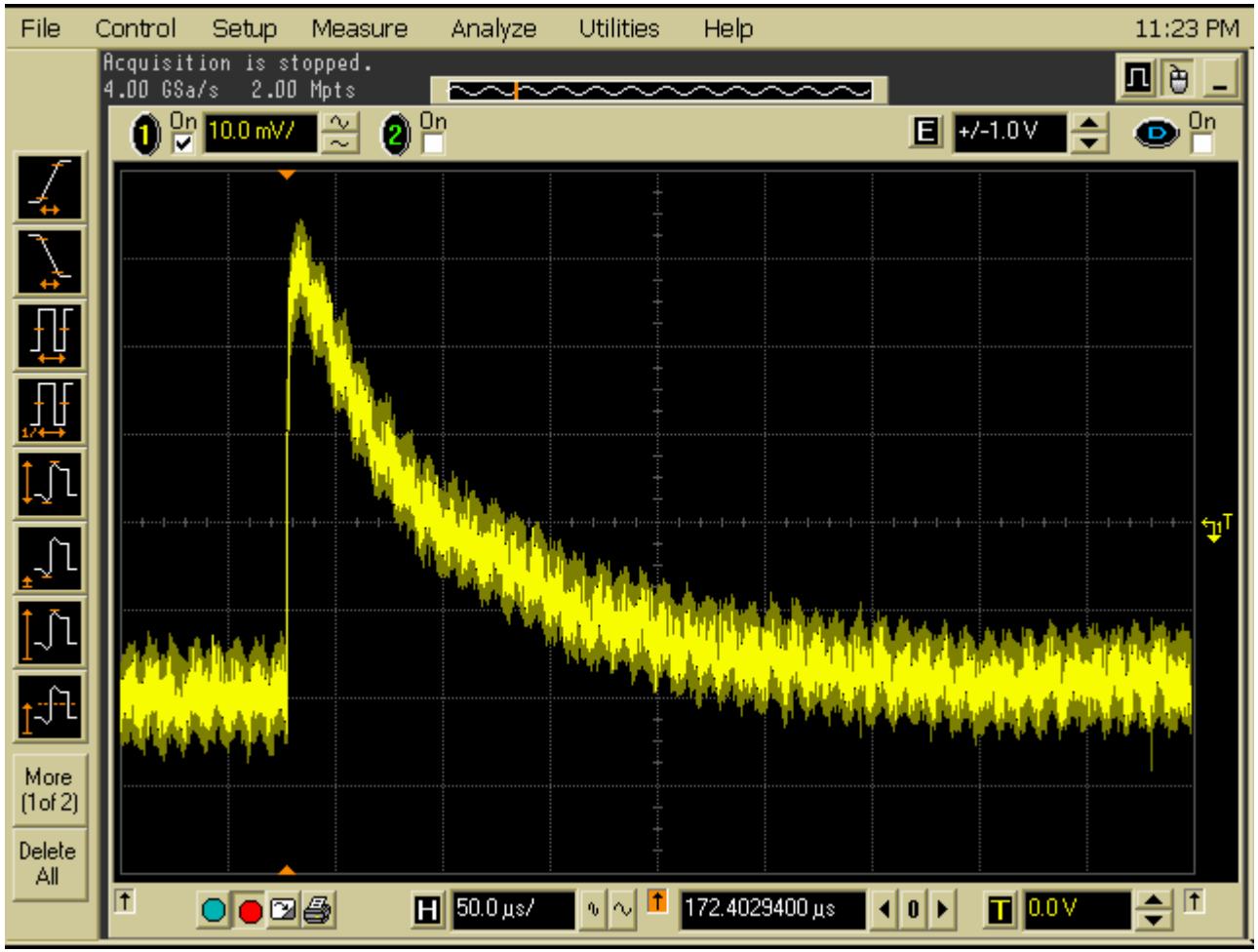
Pad capacitance 15 to 20 pF

Unity Probe gain

Shunt impedance 3 MOhm/ 2pF

3 dB Bandwidth of probe is 900 MHz; 4G samples/s Scope

Unfiltered Signal at Readout Pad (900 MHz bandwidth)



Hor.: 50 µs/div ver.: 10mV/div

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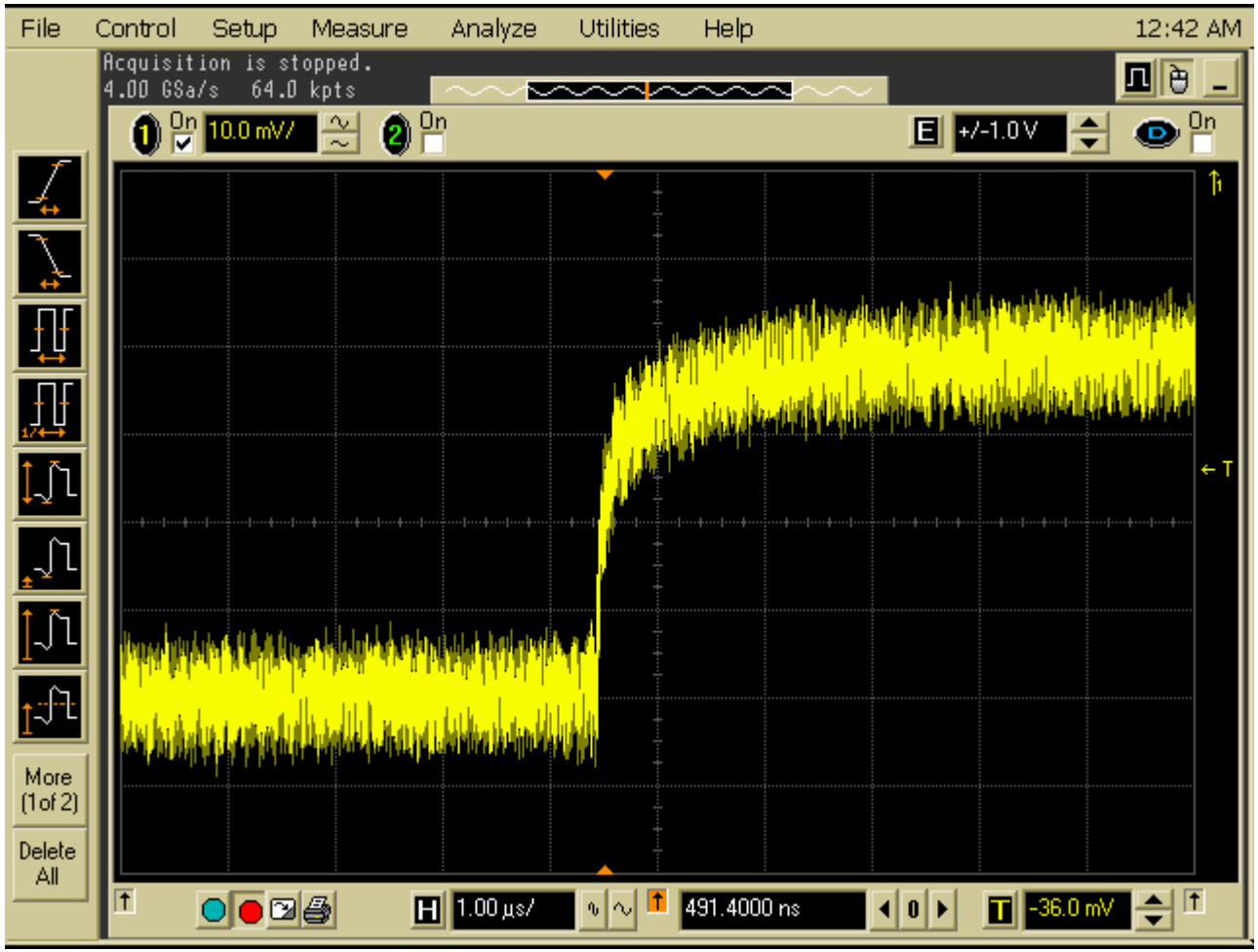
Unfiltered Signal at Readout Pad (900 MHz bandwidth)



Hor.: 1 µs/div ver.: 10mV/div

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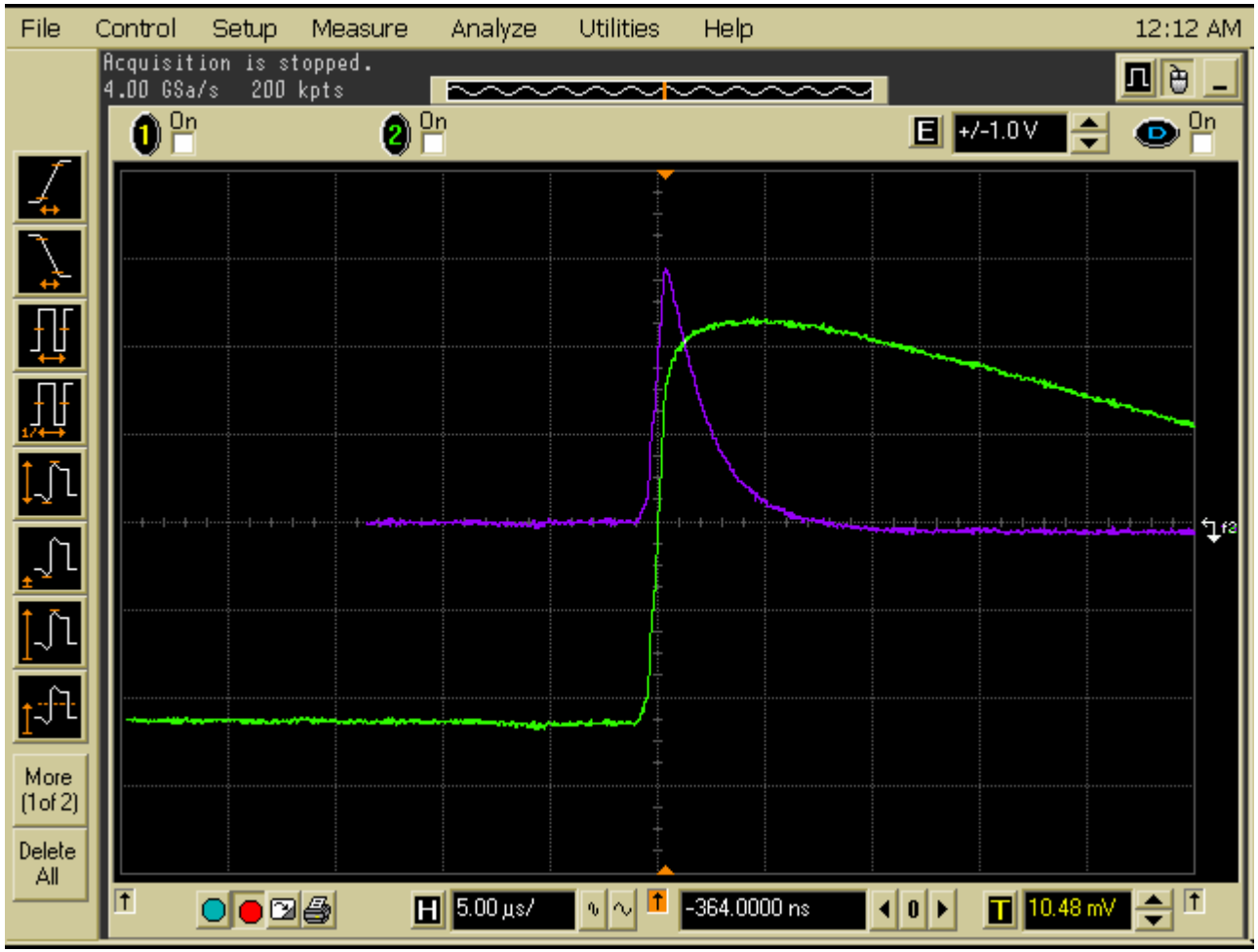
Filtered Signal at Readout Pad (green lowpass; magenta highpass)



Hor.: 5 µs/div ver.: 10mV/div

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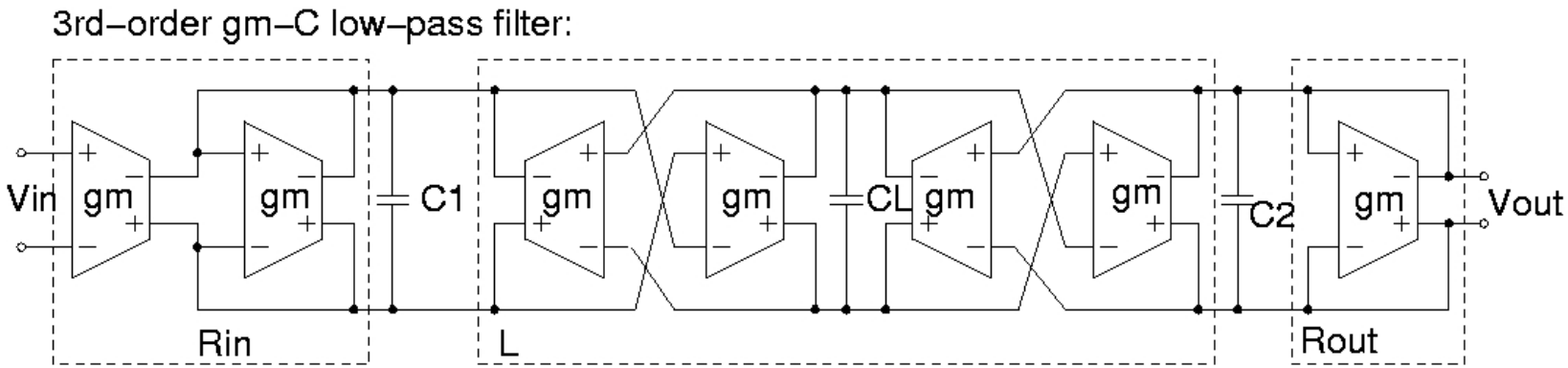

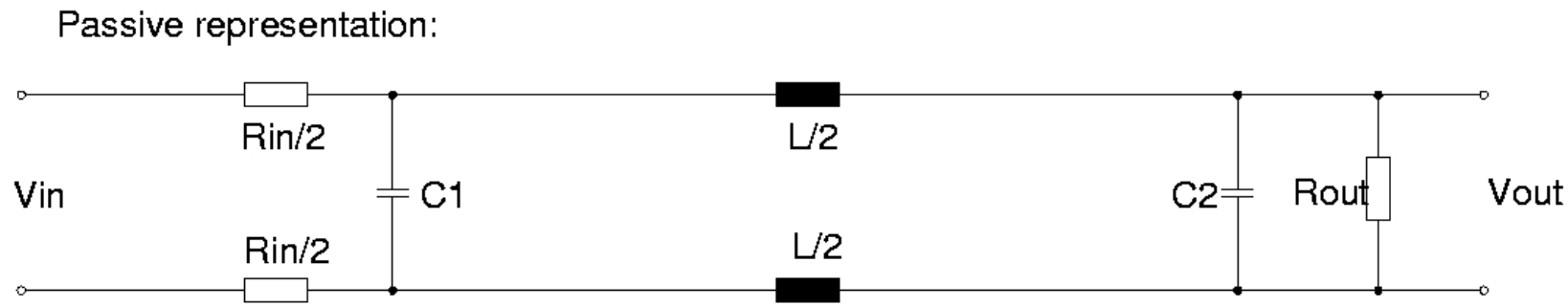

Active Anti-aliasing Filter

Summary

- Several Building Blocks have been verified in Silicon ready for Re-Use in Fair FEE Systems: Low Power LVDS/CML I/O-cells; Gigabit SerDes; Optical line driver/receiver cells; Low Power 10 bit/10MS/s ADC-cells

- A field programmable Preamplifier-Filter-ADC Chip is proposed, featuring flexibility of filter parameters, ADC resolution and sampling rate.

- Differential inputs of the PreAmp are foreseen to reduce pick up noise of large detector arrangements. This could be a dominant contribution compared to thermal noise.

- High order lowpass Gm/C- filter can provide a wide range of parameter settings according to the reqired sigmal bandwidth of the detector.

- Dual Range ADC is an option; programmable resolution and sampling rate is a goal in accordance with power scaling.

- First Silicon of a flexible 12bit 70 MS/s Low Power ADC has been verified on the latest 0.18 µm test chip (presented by D. Muthers)

- Novel Clock and Darta Recovery Units suited for clock distribution of FEE boards have been demonstrated on the latest 0.18 µm test chip (presented by S. Tontisirin)