General Purpose Charge Readout Chip

FAIR FEE Workshop, GSI, 12 October 2005

Outline

- Motivations and specifications
- Architecture & building blocks
- Programmable Charge Amplifier ⇒ Gerd Trampitsch
- Time-interleaved Multi-Channel A/D Converter
- Digital filtering and Signal Feature Extraction
- Project Milestones

Motivations & Specifications 1/2

- Requirements to the front-end and readout electronics set by the present generation of High Energy Physics Experiments:

  low power, high speed, high density, radiation tolerance

- These requirements can only be met by highly integrated systems implemented with very deep submicron CMOS technologies.

- The volumes of ICs required for a typical HEP detector remain low <1Mch

- Non Recursive Engineering (NRE) costs are more and more dominant for high energy physics and, in the absence of standardization, will become prohibitive for many sub-detectors in the future.

- Development of *standard* chips capable of handling a wide range of high energy physics applications, in order to obtain a reasonable volume to warrant the NRE expenditure.

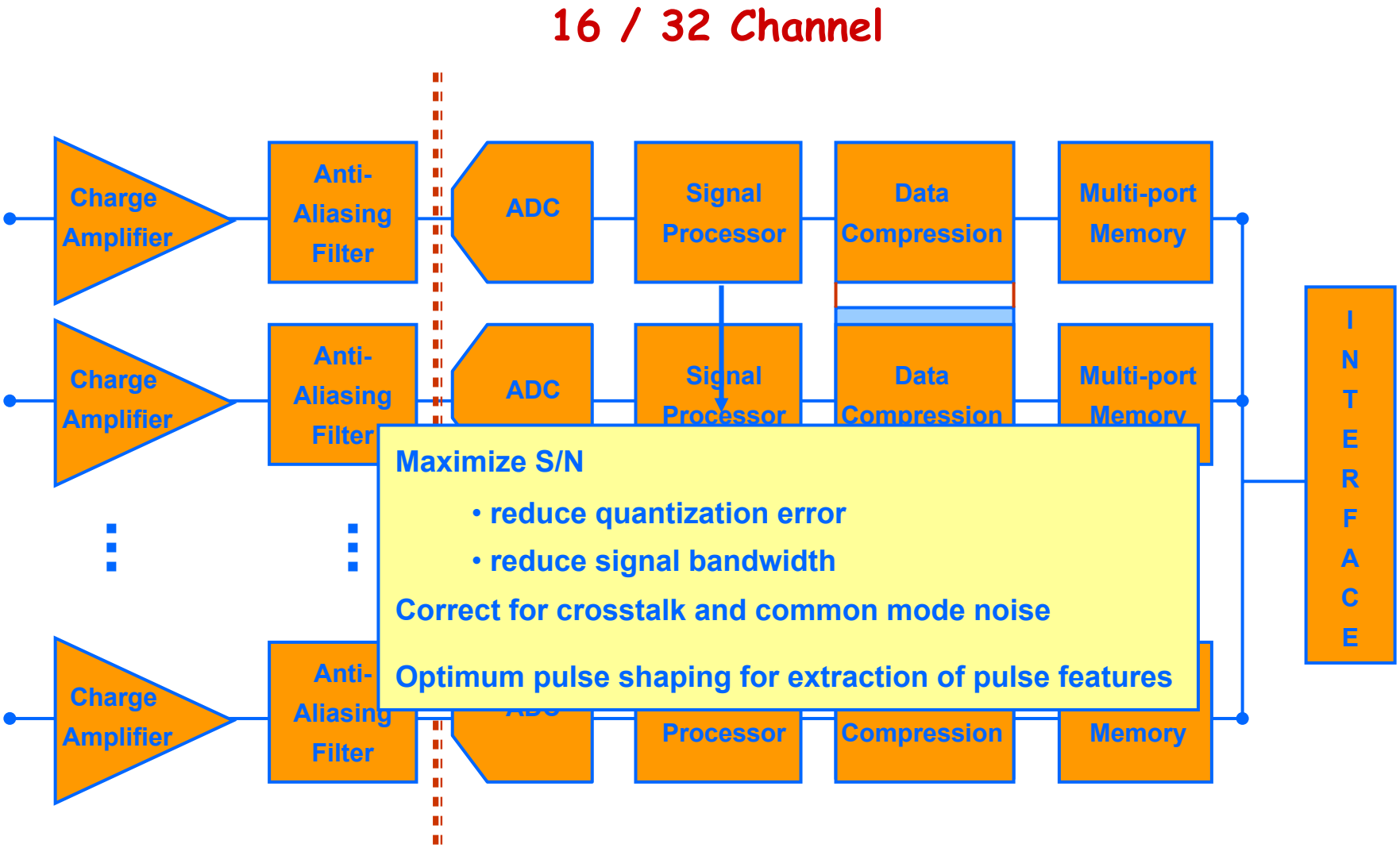
- Likely this polyvalence of the circuits will be obtained through an increased level of programmability.

Motivations & Specifications 2/2

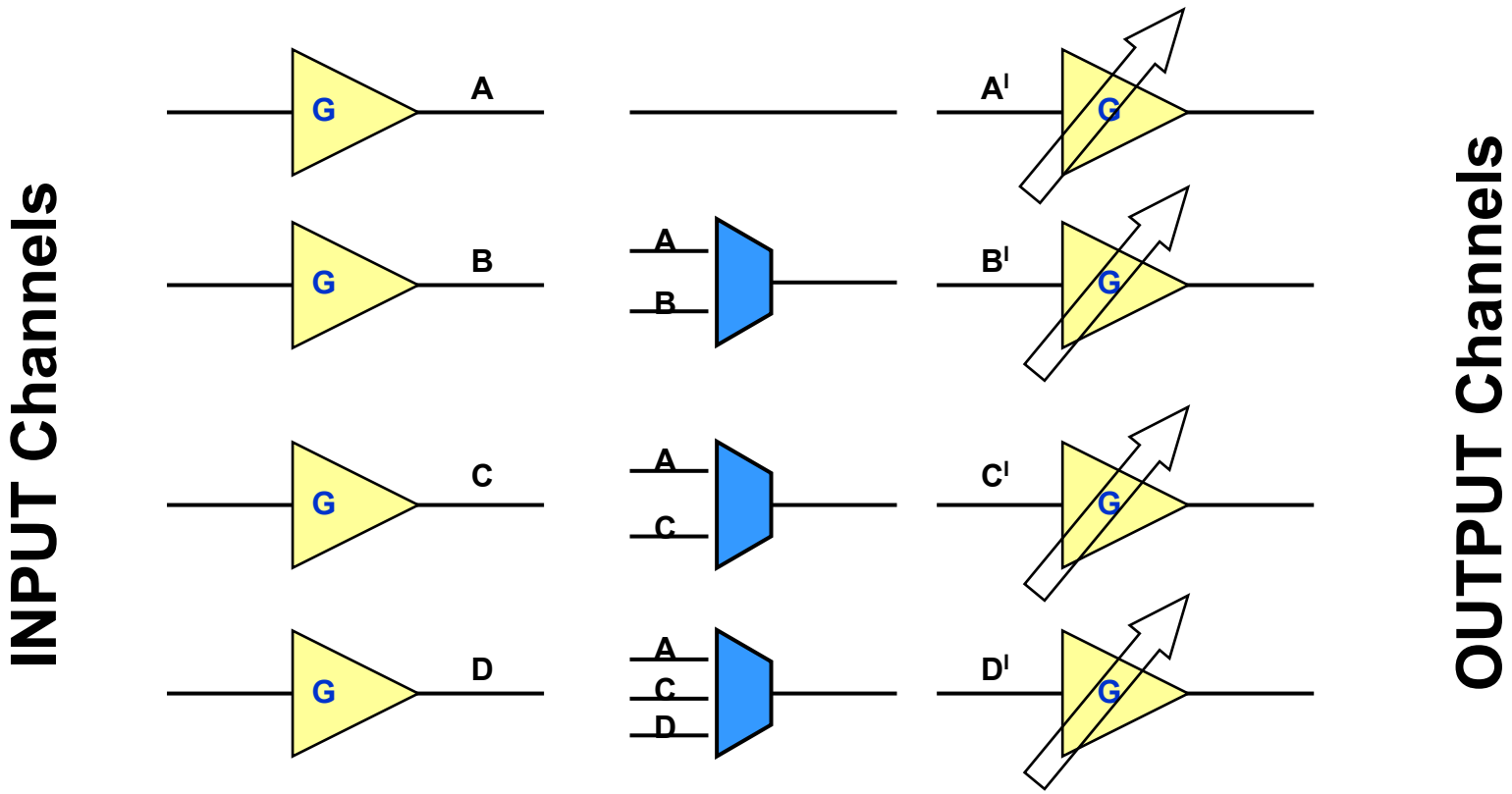
A general purpose charge readout chip

- number of readout channels: 16 or 32
- programmable charge amplifier:
  - sensitive to a charge in the range: ~10^2 - ~10^7 electrons
  - Input capacitance: 0.1pF to 100pF
- high-speed high-resolution A/D converter:
  - sampling rate in the range 40MHz - 160MHz;
- programmable digital filter for noise reduction and signal interpolation;
- a signal processor for the extraction and compression of the signal information (charge and time of occurrence).

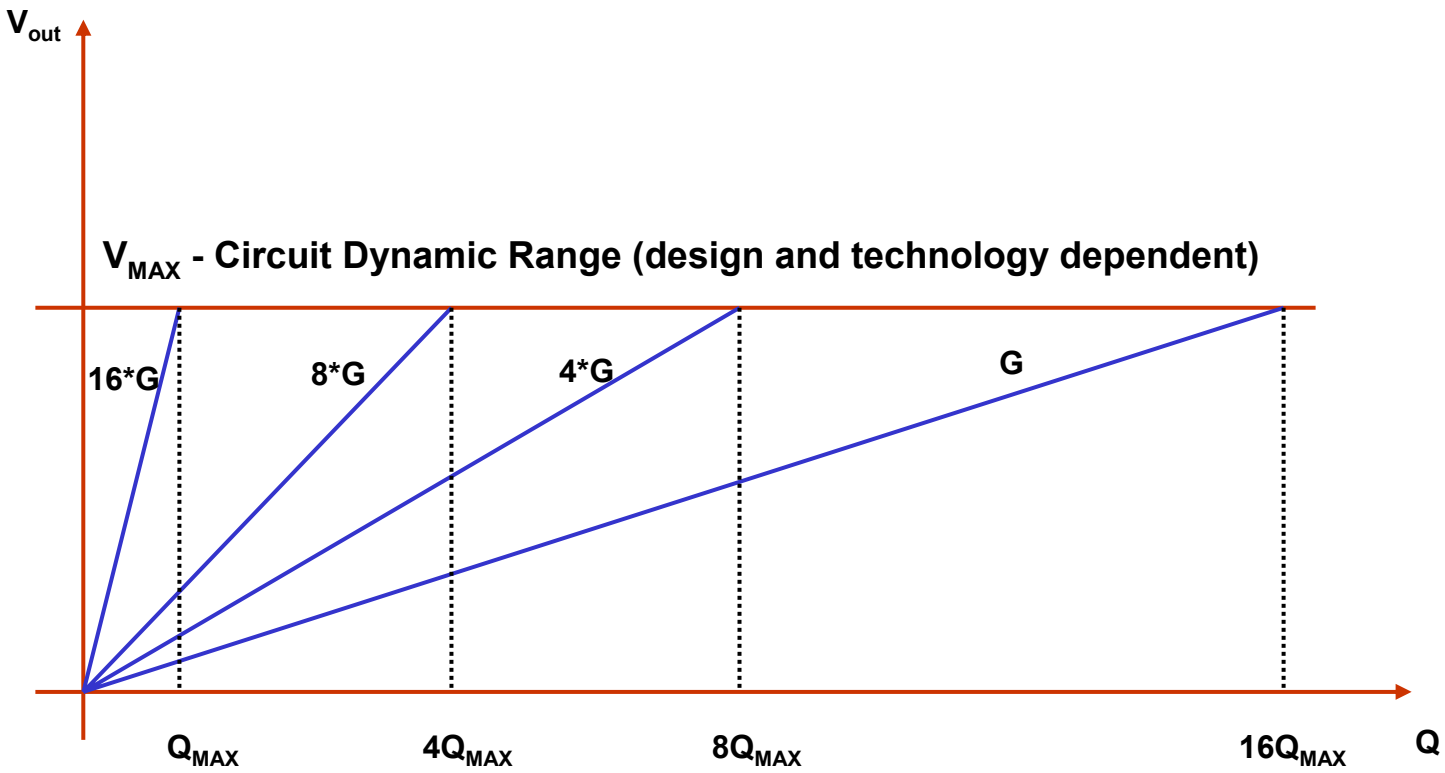
Charge Readout Chip Block Diagram



Programmable Piece-wise Linear Amplifier



Charge Sampling Amplifier 2/10



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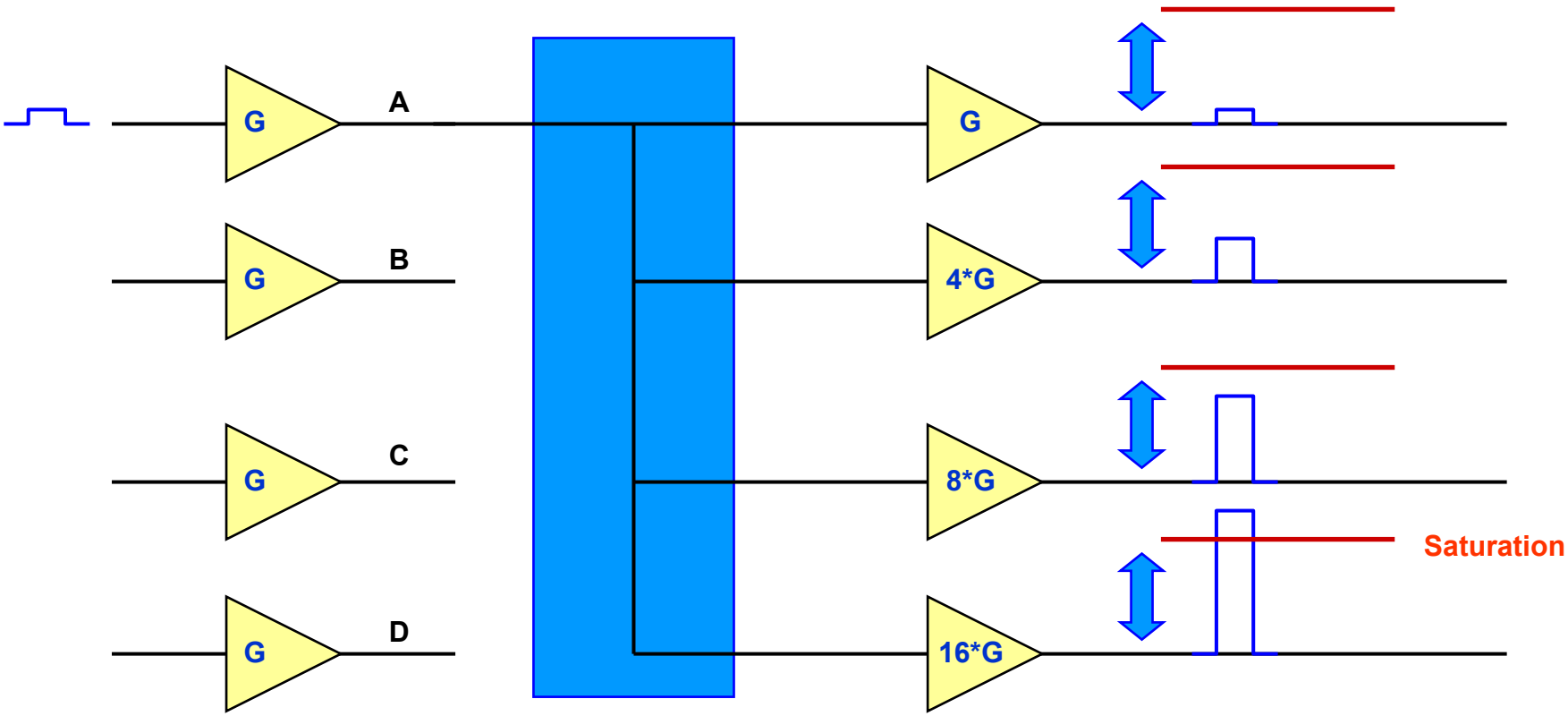
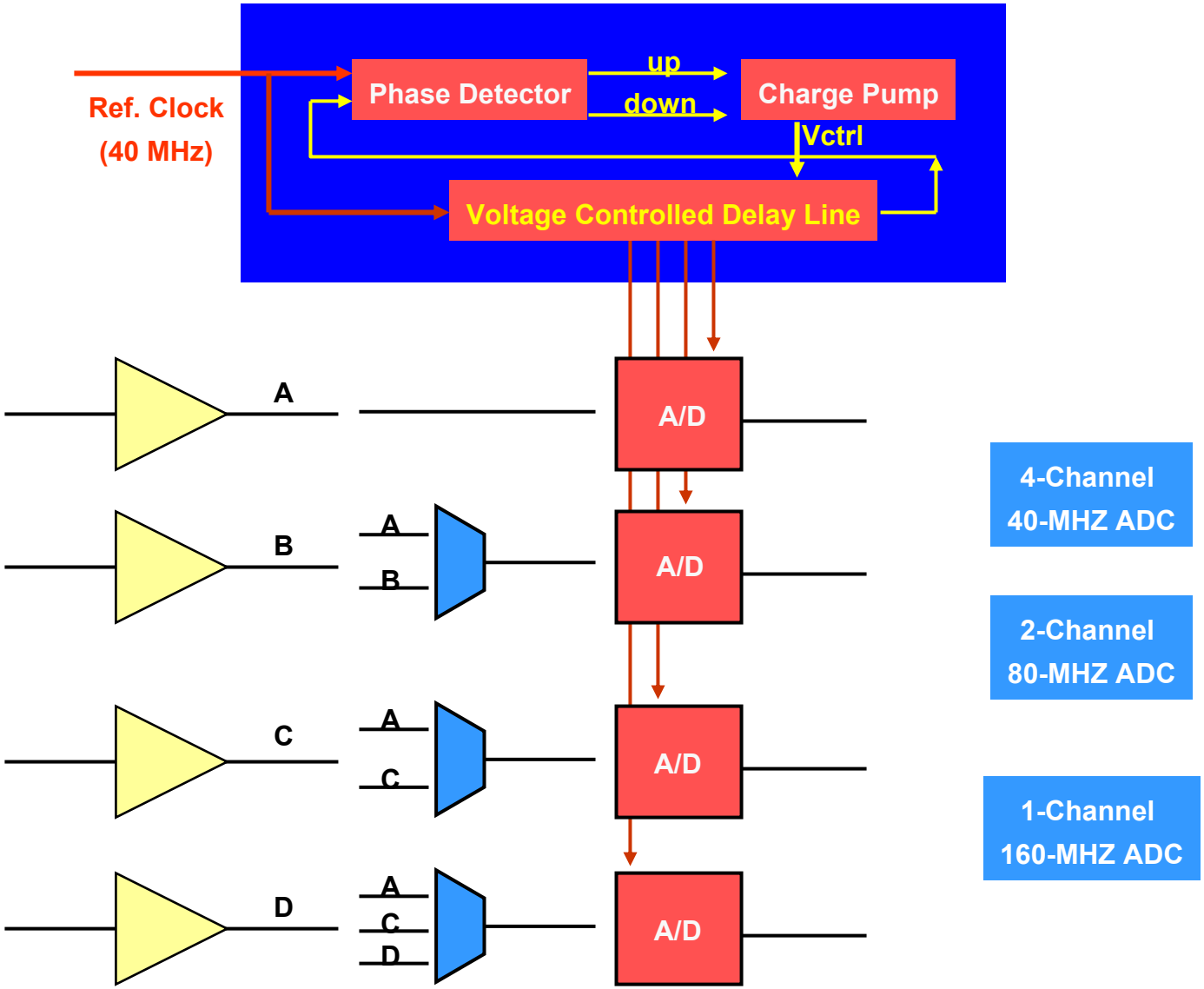
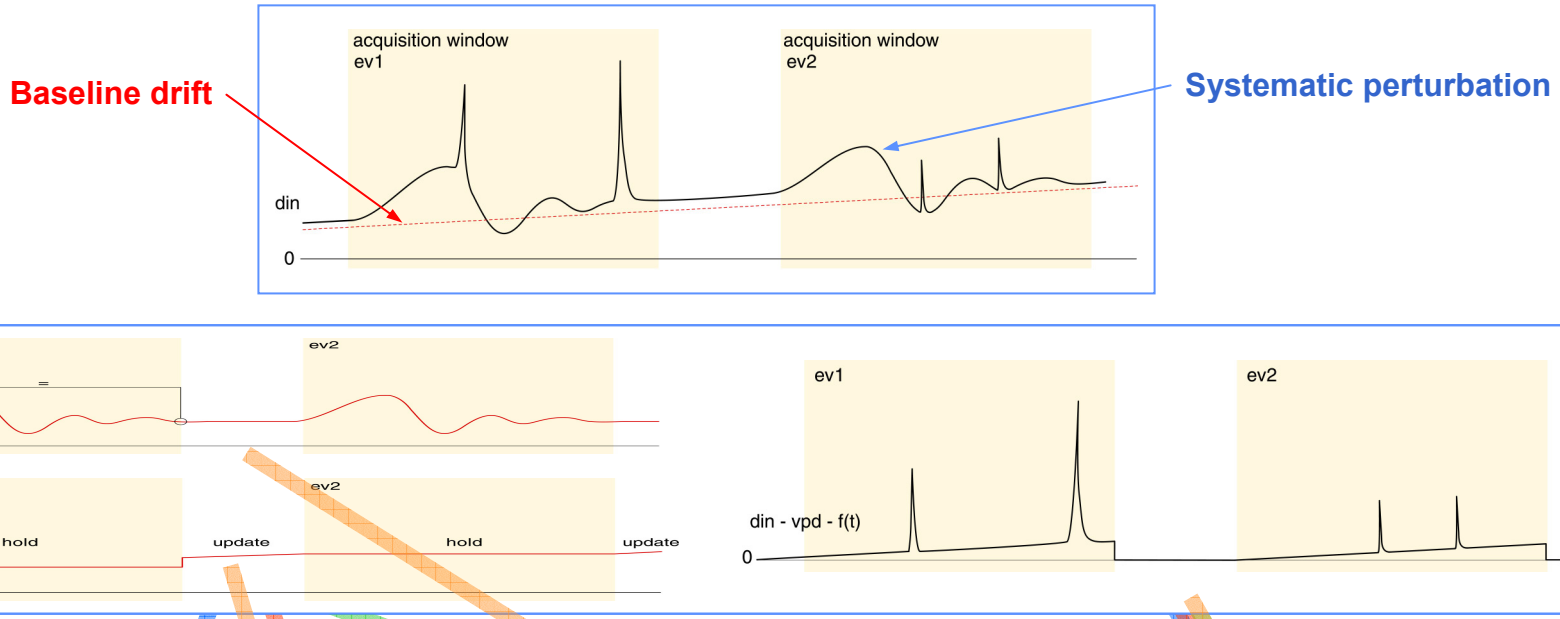


Multi-Channel Time-Interleaved A/D Converter

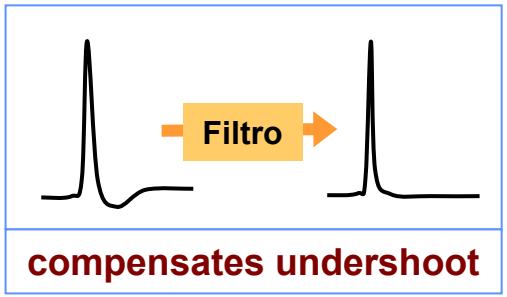


Baseline Correction I

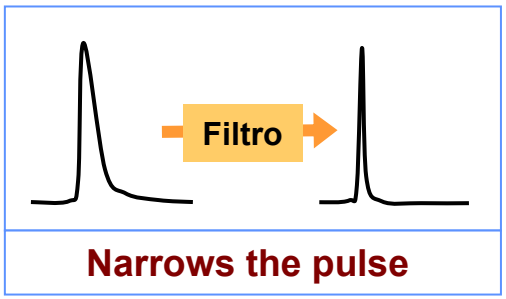


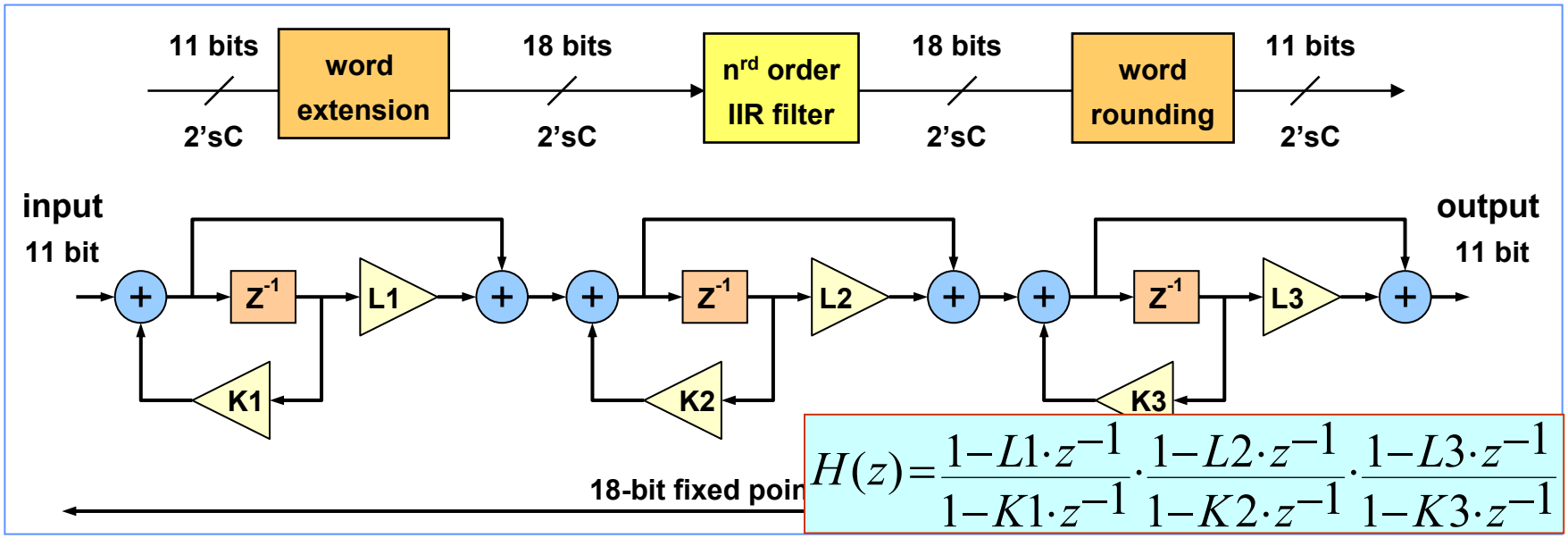
Pulse Shaping Filter

- **Functions**
  - signal shaping
  - pulse narrowing ⇒ improves cluster separation
  - gain equalization



- **Architecture**
  - n[rd] order IIR filter
  - 18-bit fixed point 2'sC arithmetic
  - single channel configuration ⇒ 6 coefficients / channel

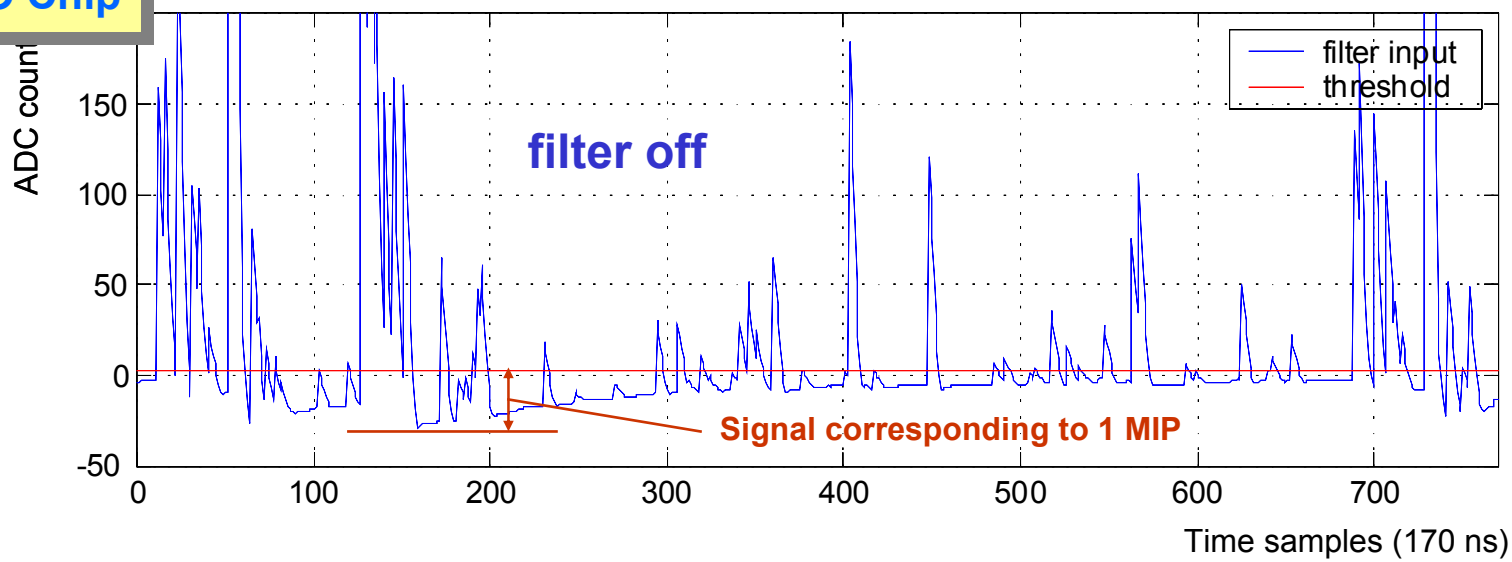




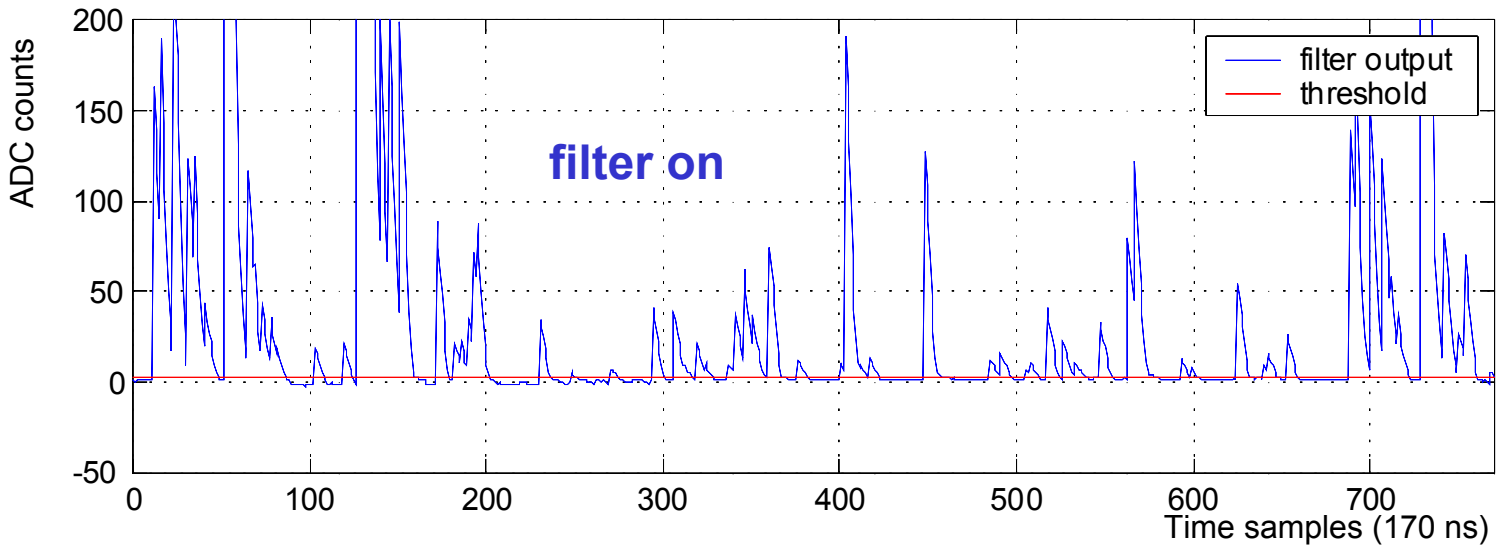
Test of the Pulse Shaping Filter

ALTRO Chip

DIGITAL TAIL CANCELLATION PERFORMANCE



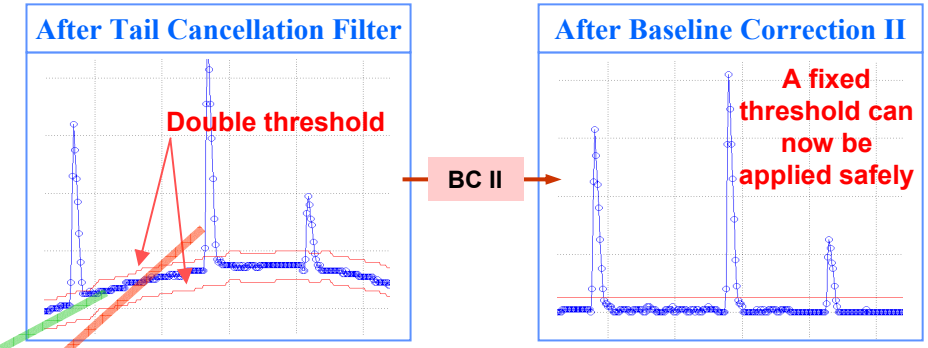
Filtered data and fixed threshold



Baseline Correction 2

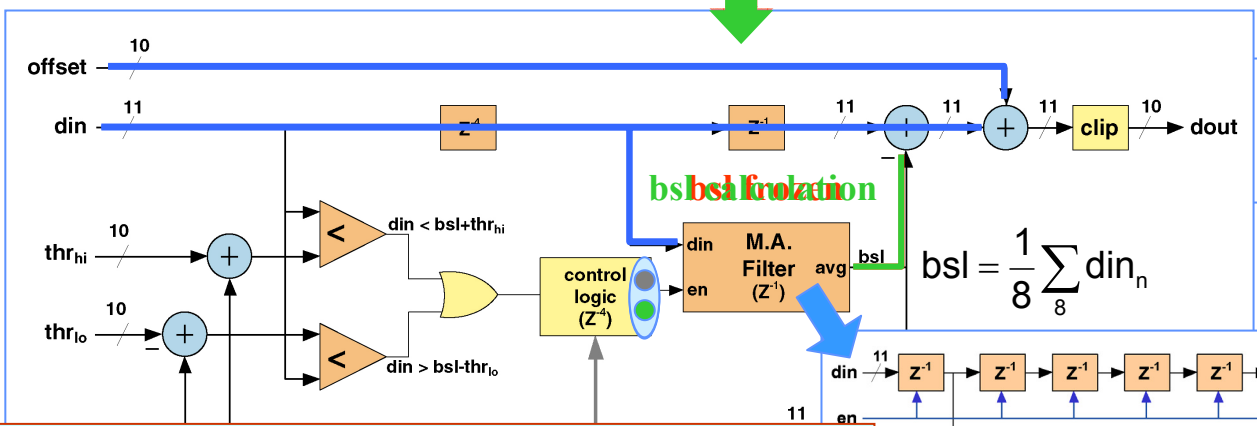
Characteristics:

- Corrects non-systematic perturbations during the processing time
- Moving Average Filter (MAF)
- Double threshold scheme (acceptance window)



Operation

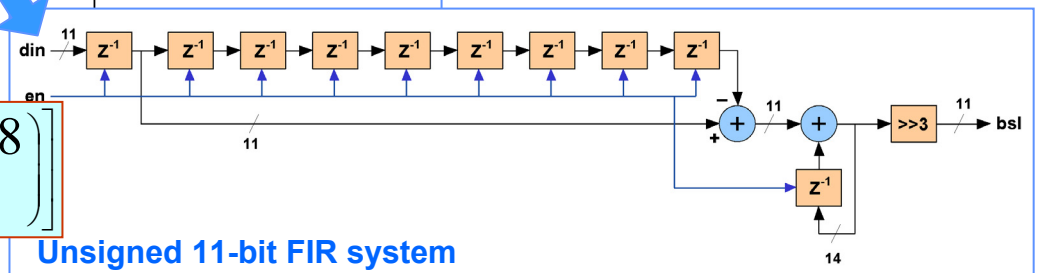
1. Slow variations of the signal ⇒ Baseline updated
2. Fast variations of the signal ⇒ Baseline value frozen



$$bsl = \frac{1}{8}\sum_{8} din_n$$

$$\begin{cases} din - bsl + offset & , 0 \le dout \le 1023 \\ 0 & , dout < 0 \\ din - bsl + offset - 1024 & , dout > 1023 \end{cases}$$

$$H(z) = z^{-1}\left[1 - \frac{1}{8}\cdot\left(1 + z^{-1} + z^{-2} + \ldots + z^{-8}\right)\right]$$

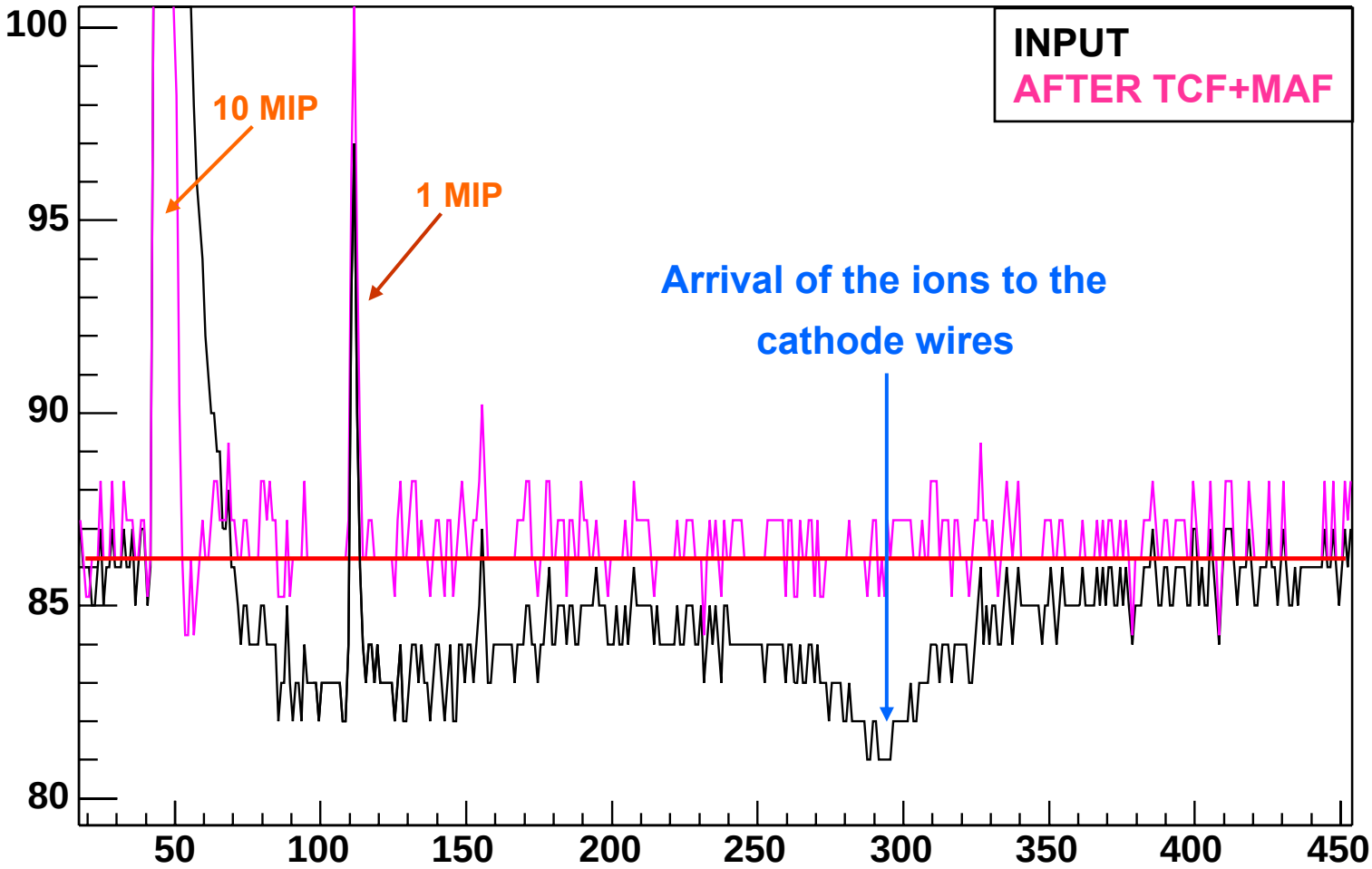


Unsigned 11-bit FIR system

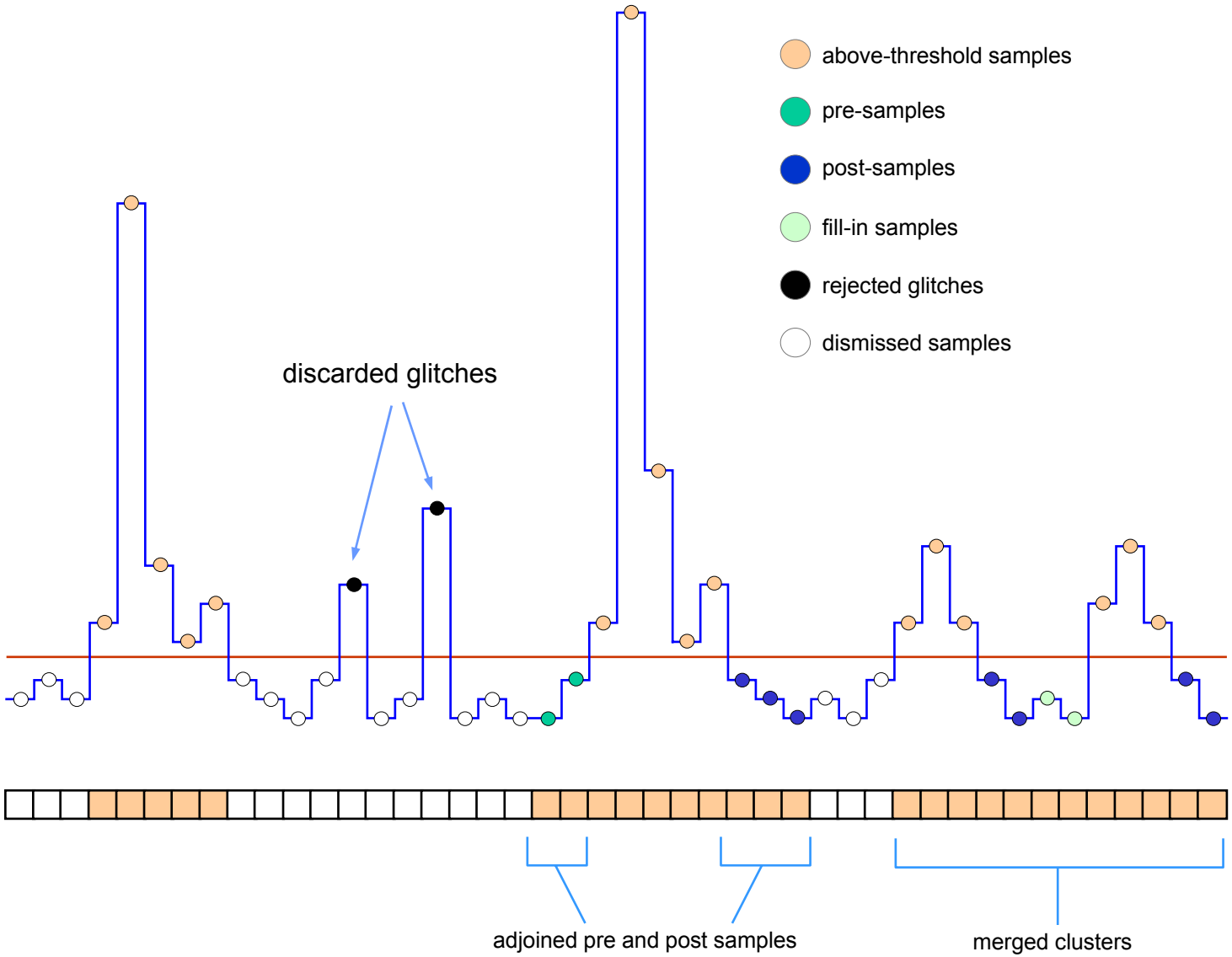
Test of the Adaptive Baseline Correction

ALTRO Chip

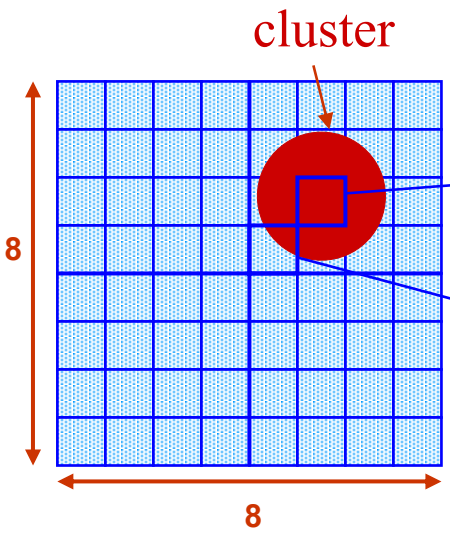
IONIZATION WITH COSMIC RAYS

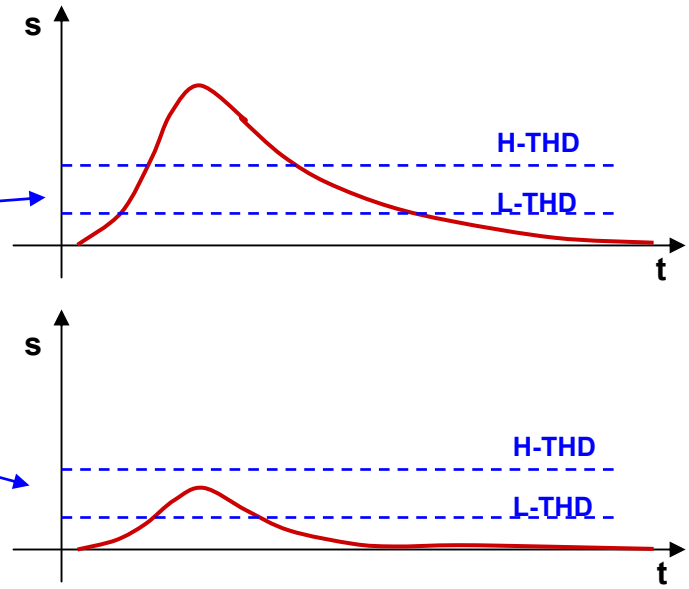


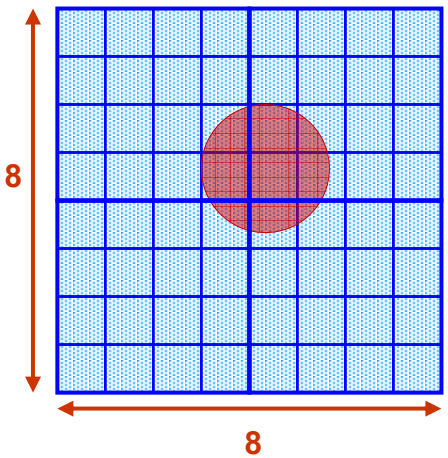
1-D Zero Suppression

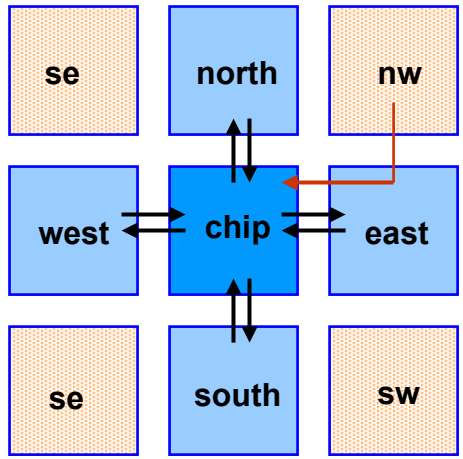


2-D Zero Suppression







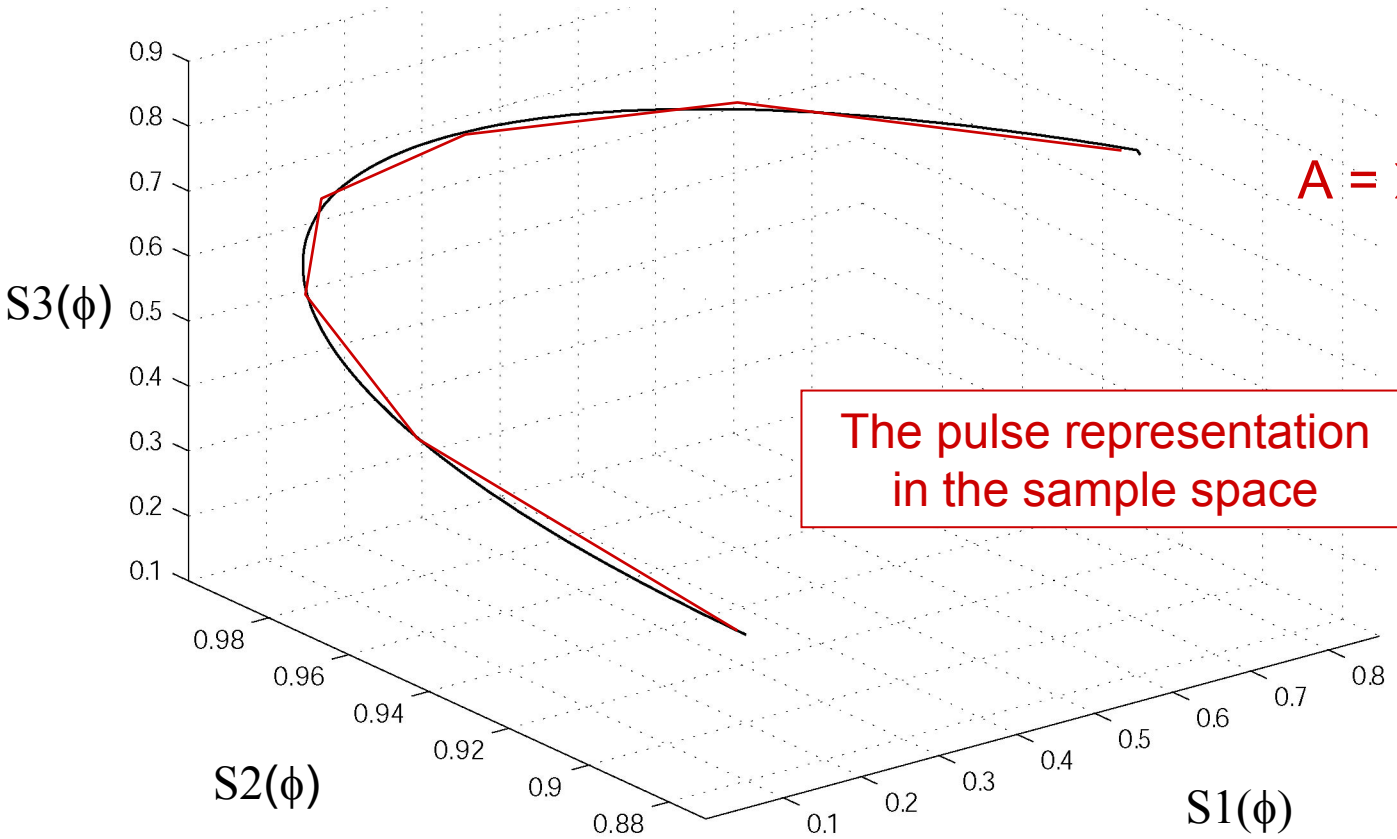


Recovery of signal parameters 2/2

Extraction of the pulse features (amplitude and time)

V. Buzuloiu et al.

Find the pulse features, Amp = F(S1,S2,…) and time = T(S1,S2,..), as quasi-invariants in the sample space



$A = \Sigma\, a_i(\phi_j)\, S_i$

The pulse representation in the sample space

Project Milestones

- Milestone I (Q4 2006) ⇒ Programmable Charge Amplifier (prototype)
  - 16 channel charge amplifier + anti-aliasing filter.
- Milestone II (Q2 2007) ⇒ 10-bit multi-rate ADC (prototype)
  - 4-channel 10-bit 40-MHz ADC. The circuit can be operated as a 4-channel 40-MHz ADC or single-channel 160-MHz ADC.
- Milestone III (Q2 2008) ⇒ Charge Readout Chip (prototype)
  - This circuit incorporates 16 (or 32) channels.
- Milestone IV (Q2 2009) ⇒ Charge Readout Chip (final version)