Studies on Programmable Charge Amplifier

GSI, FAIR FEE Workshop

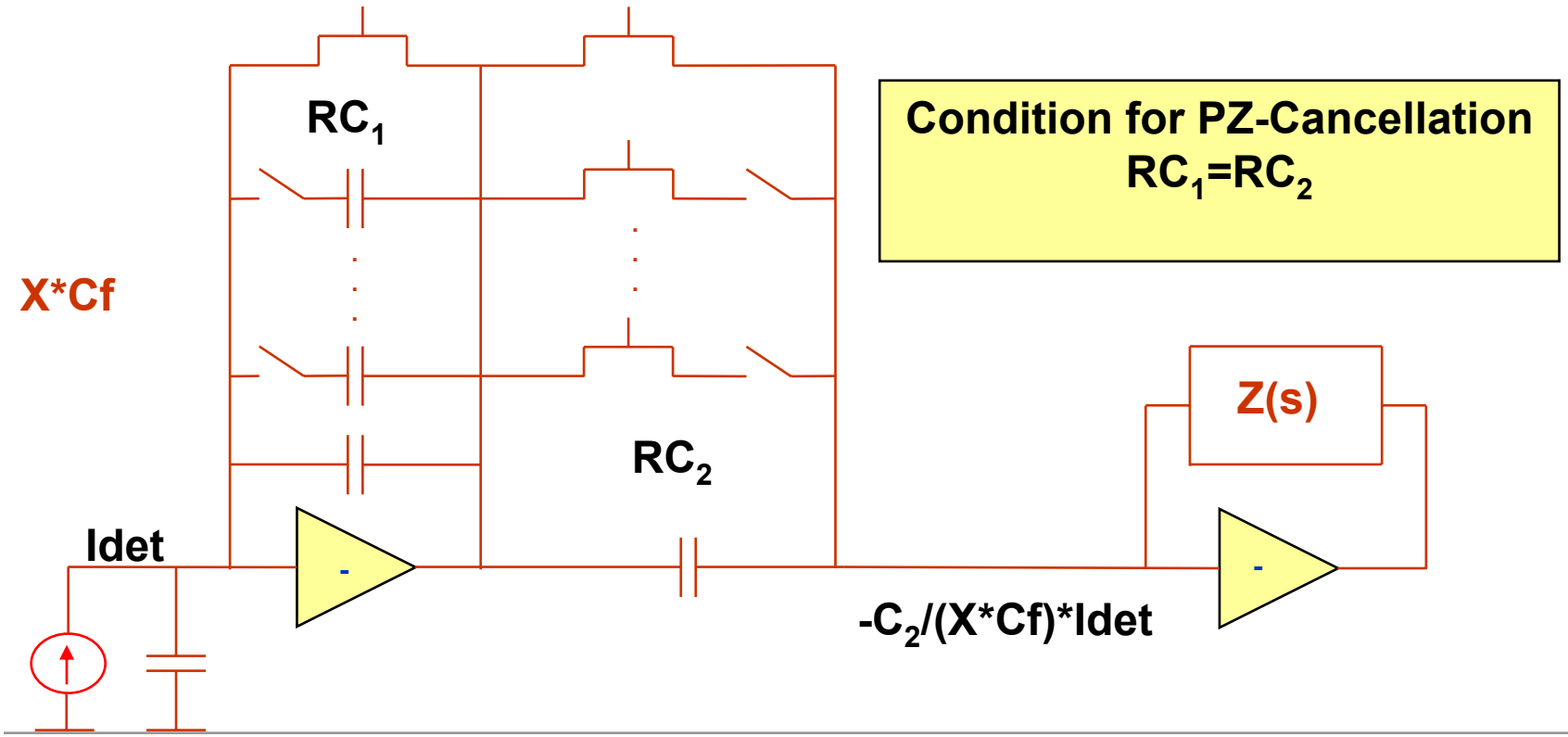
Trampitsch Gerd CERN - PH/ED

Overview

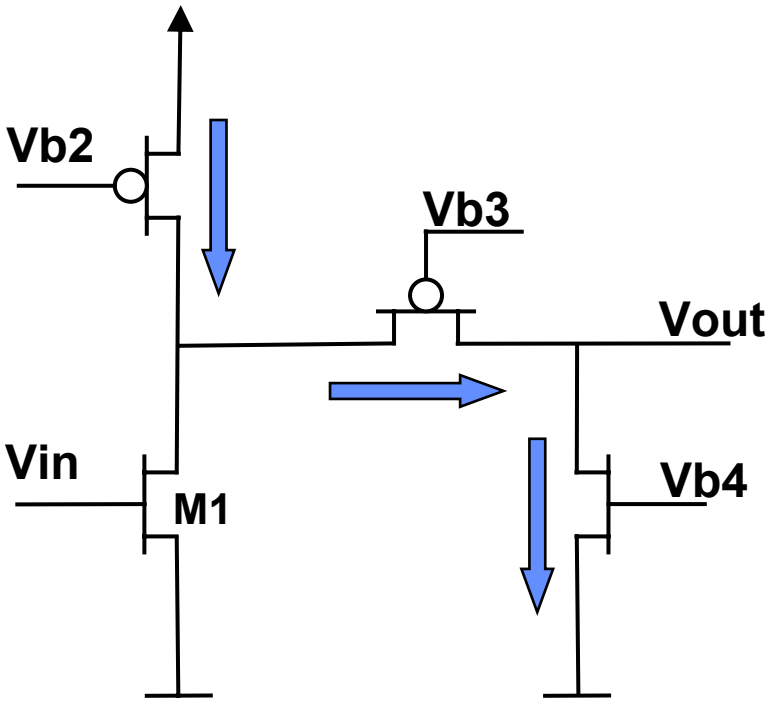
- **Ways towards a programmable Analog Front End**
  - Programmable Analog Parameters
    - Input Charge Range
    - Gain
    - Feedback Resistance of the CSA
    - Peaking Time
    - Sensitivity to signals with positive and negative polarities
- **Design of a Charge Sensitive Amplifier and Shaper in the IBM 0.13um CMOS process**
  - Architecture
  - Schematic and Layout of the CSA
  - Characteristics of the Circuit

Changing the Conversion Gain

- **Adopt Input Stage to different Charge Ranges**
  - Different Detectors
  - Calibration of Conversion Gain
  - Calibration of imperfect Pole Zero Cancellation
  - Input of an inverting Amplifier is held at constant Voltage ➔ Constant On-Resistance of Switches



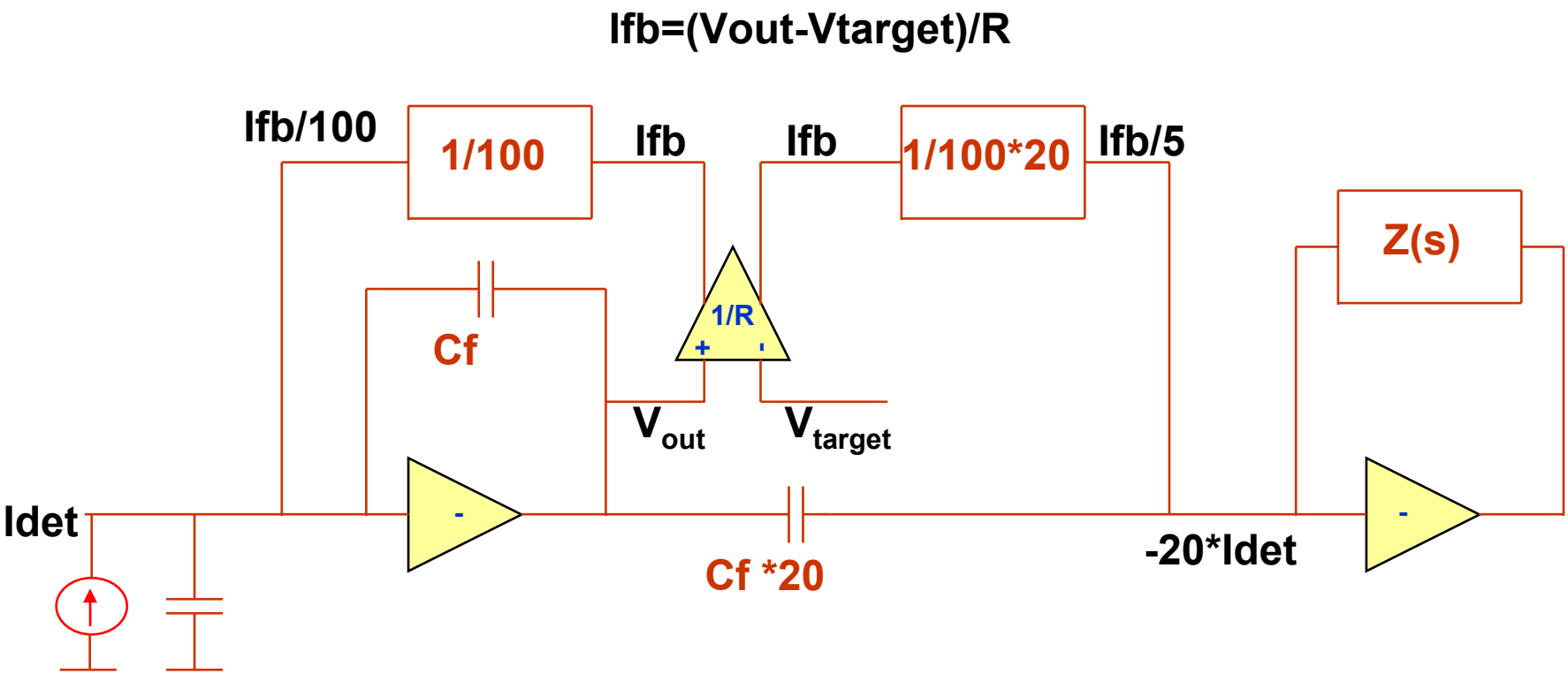
Sensitivity to positive and negative signals



- **Limited Output Swing**
  - Voutmax=Vb3+Vth
  - Voutmin=Vsat4
  - Max Output swing
    - Vdd-3Vdsat
  - Gets less when designing for low Noise
  - At 1.5V supply, only some hundreds of mV

- **Solution**
  - Design Rail to Rail Preamp ➔ Allows more Gain in the first Stage ➔ Less Feedback Capacitance
  - Change DC Level of the Amplifier's Output according to the expected Input Signal (Ions or Electrons)

Sensitivity to positive and negative signals

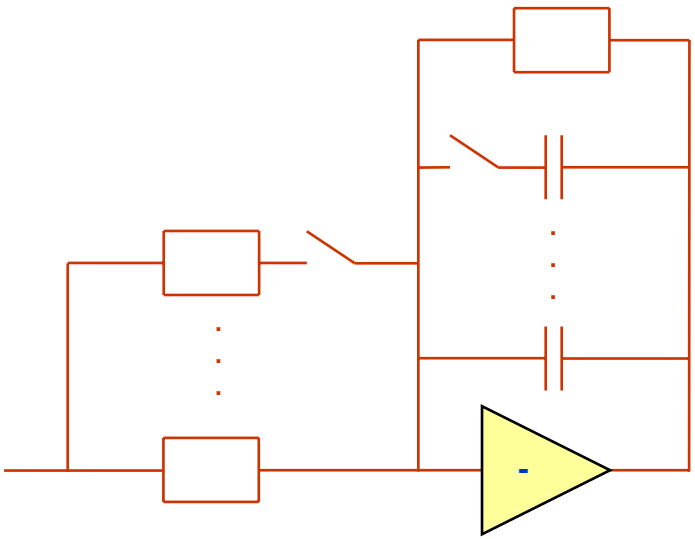


- **Transconductor sets the output dc level to the desired voltage(V_{target}) independently to the input dc Level**
  - This architecture can handle both, positive and negative going signals
  - Effective Feedback Resistance is 100R
  - Ifb gets divided by current mirrors with different aspect ratios

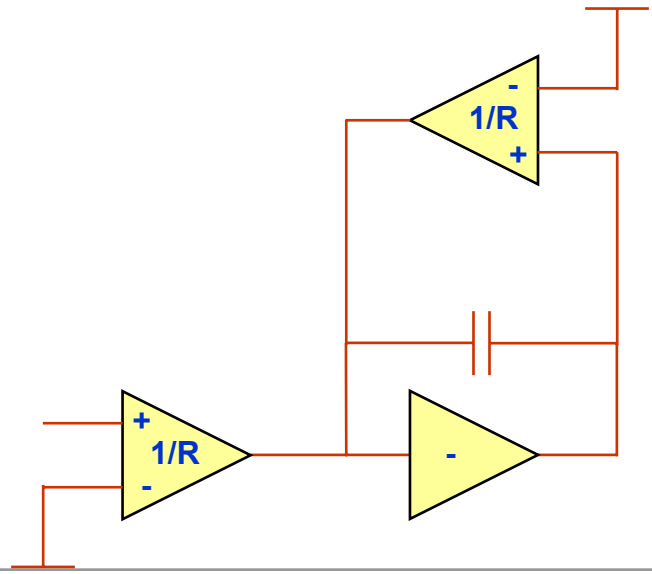
Changing or Adjustment of the Peaking Time

- **Basic 1st Order Filter Cells allow to tune Gain and Time Constants Independently**
- **Build Higher Order filters by cascading of 1st Order Cells or Biquads**

- **RC Filter**
  - **Better Linearity**



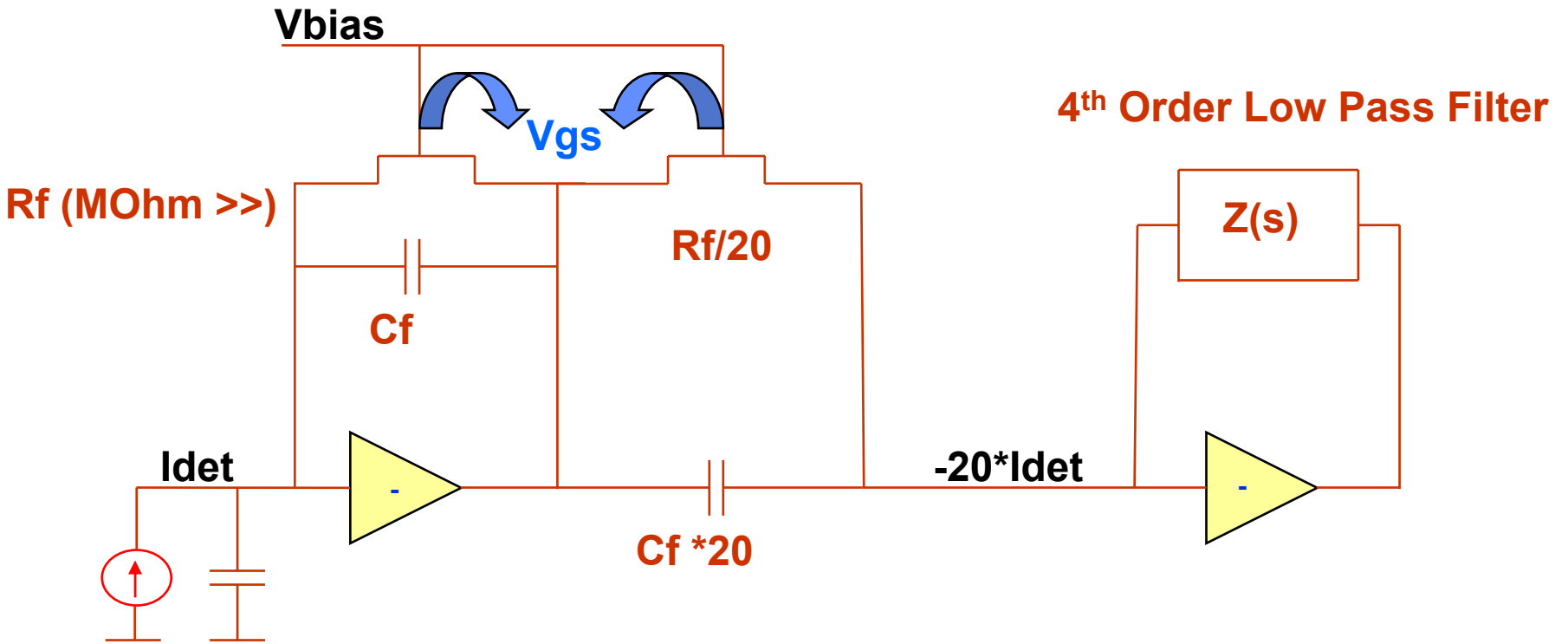
- **Gm-C Filter**
  - **Wider Tuning Range of Time Constants**



Design for low noise in CMOS 0.13um

- **Increased gm**
  - + Better ENC (Equivalent Noise Charge)
    Should ideally improve by ca. 20% per CMOS Generation
- **Low Supply Voltage limits SNR**
  - - Dynamic Range
  - Rail to Rail Design
  - Invest Power to improve SNR
    - Big Capacitors
    - Design Shaping Circuit for Low Noise
- **Reduced Gate Oxide Thickness**
  - - Gate Tunneling Current
  - + Radiation Tolerance
- **Short Channel Effects**
  - Hot Carrier Stress – Reliability, Noise
  - Velocity Saturation

Architecture – CSA & Semi Gaussian Shaper



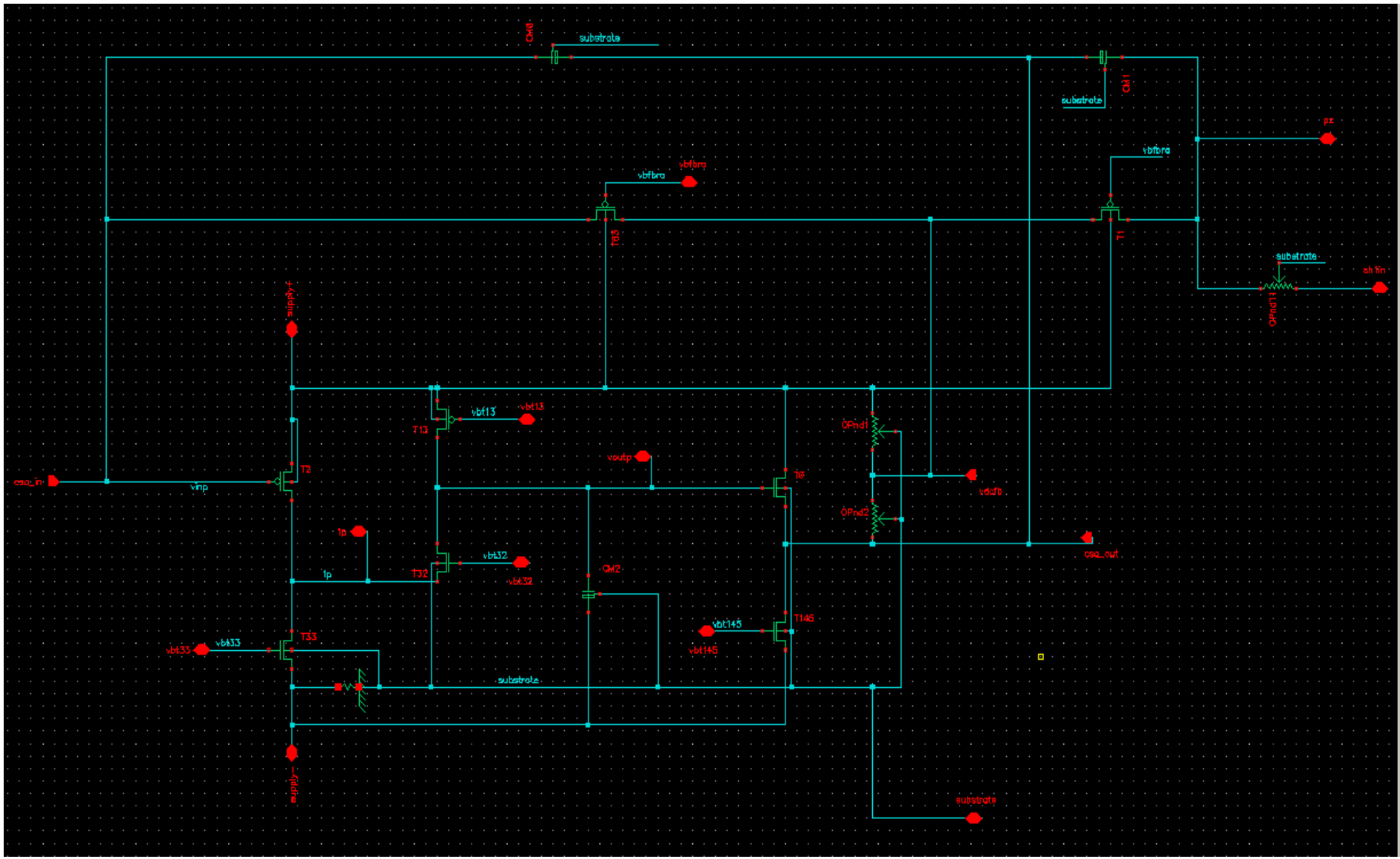
- The Resistance of the Feedback Element is a function of its Gate to source Voltage
  - Vgs is the same for both Transistors
  - Neglecting mismatches between the two transistors the according resistance should track
  - The CSA's input dc level is equal to its output dc level
  - The Current Gain is -20

CSA and Shaper

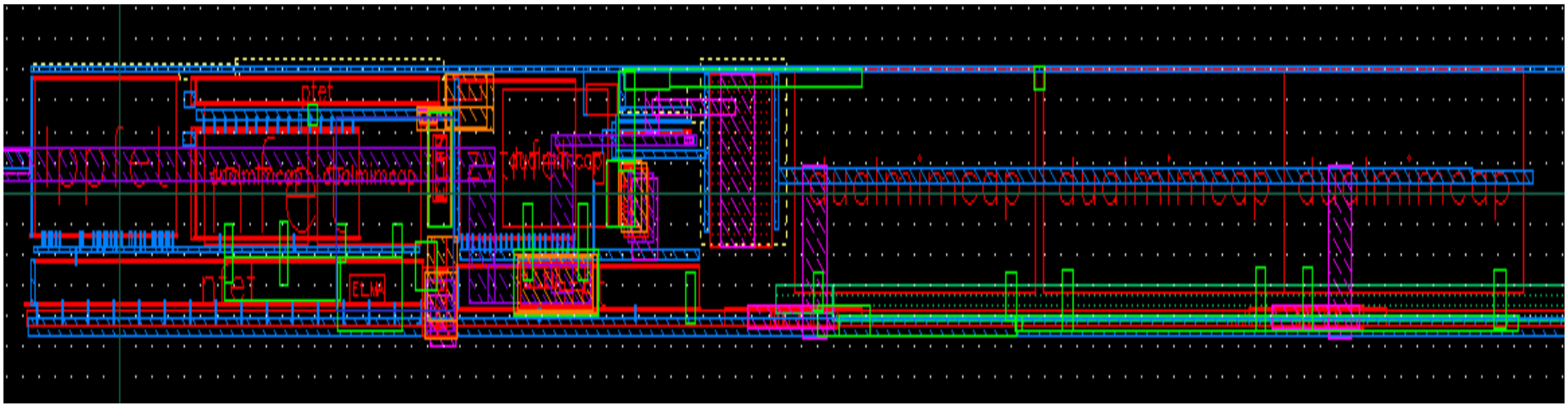
Characteristics of current Design

- ENC ca. 300 electrons$_{rms}$ (@12pF Cin)
- Peaking Time 100ns
- 4th Order Semi Gaussian Shaper
- 9mW Power Consumption
- Charge Range 0 - 160fC input signal with negative polarity
- 30pF Driving Capability of the Output Stage
- Differential Output
- Feedback Resistance of CSA ca. 10 MOhm
- Designed in a modern Process(0.13um)
  - Gives the possibility to integrate the Digital and Analog Signal Processing on the same Chip

Charge Sensitive Amplifier (Folded Cascode)



Charge Sensitive Amplifier (Layout)



- **The area is dominated by the size of the Capacitors**
  - **IBM CMOS 8RF, 0.13 um**
  - **CSA Area = 50um X 500um = 0.025mm^2**
  - **Total Area per Channel = 0.075mm^2**
  - **16 Channel Chip ➔ 2.50mm^2**