# The HADES RPC Frontend Readout System

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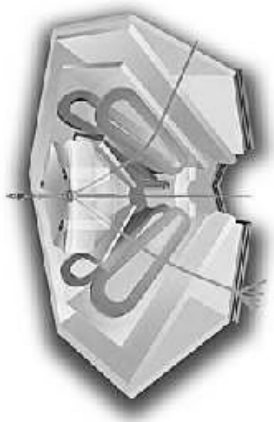
J. S. Lange [3], J. Marin [1], N. Montes [4], P. Skott [3],
M. Traxler [3], W. Koenig [3]



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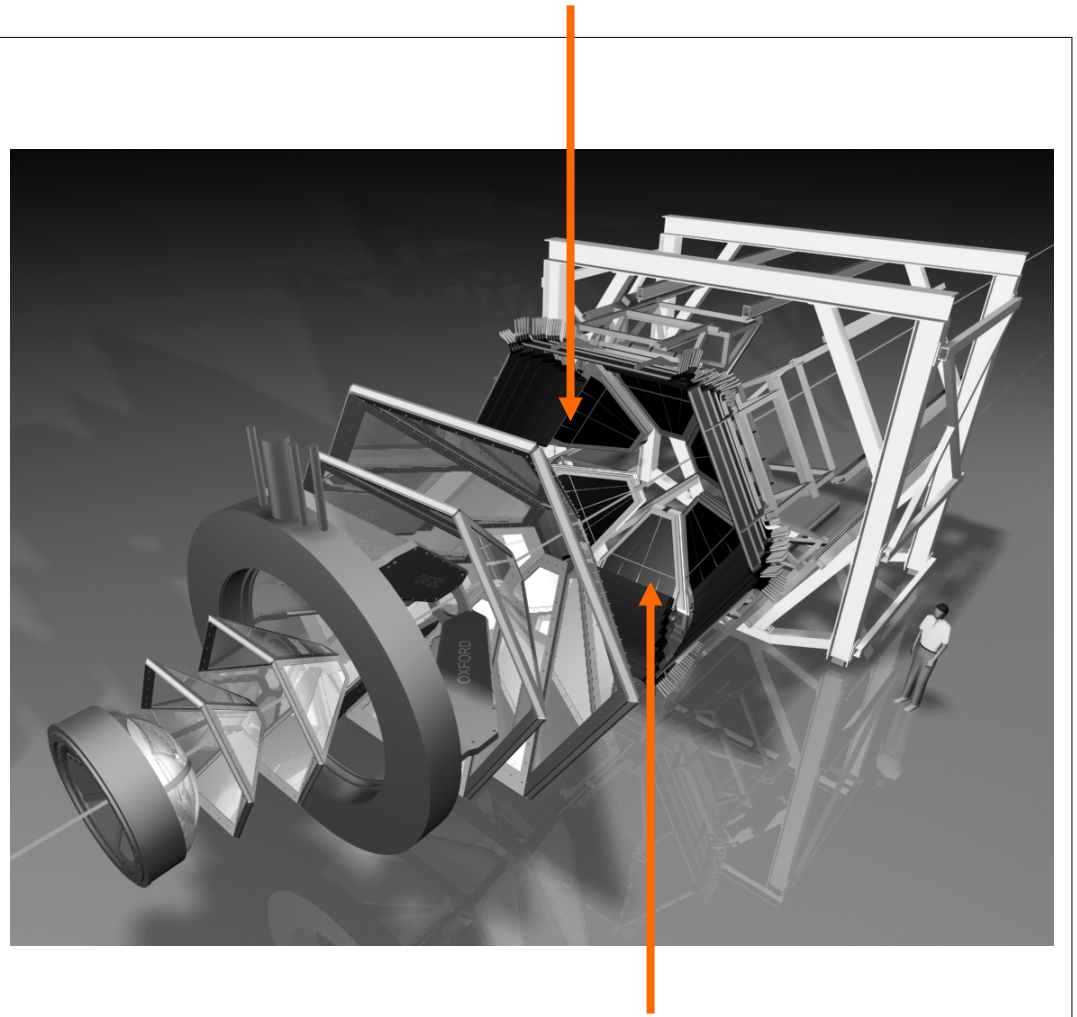
1st FAIR-FEE Workshop, GSI Darmstadt, 11-13.10.2005

# Content

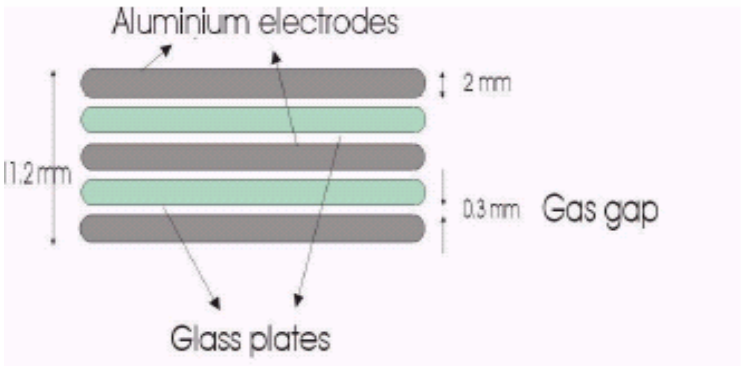
- The Daughterboard (DB)
  - 2nd iteration (STEP2)
  - 3rd iteration (STEP3)
  - 4th iteration (STEP4) – pre-final
- The Motherboard (MB)
- The Power Supply Board (RPS)
- Test results from 2 Santiago tests and 2 LIP/Coimbra tests
- Note: this talk covers everything in front of the TDC board (see talks by K. Korcyl, M. Palka)

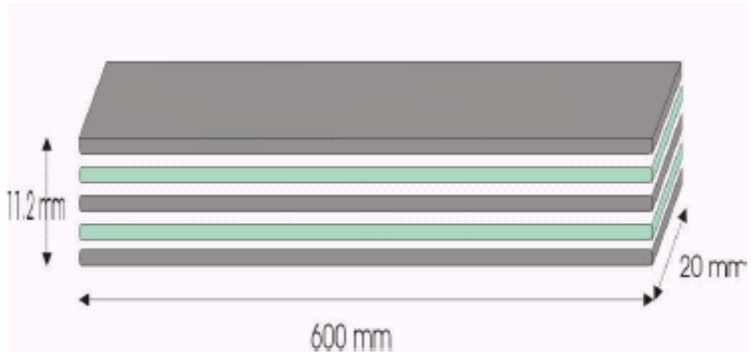
# The HADES Resistive Plate Chamber (RPC) Detector.

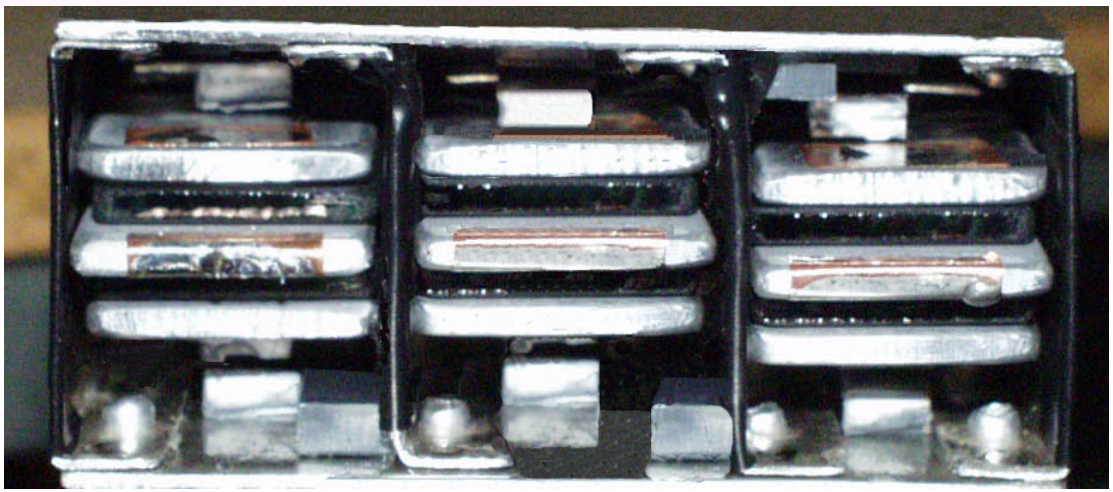
- Area 8 $m^{2,}$ 6 sectors
- construction 2005-2008
- 1024 detectors
- 2-sided
- **TOF**
  (time-of-flight)
  **TOT**
  (time-over-threshold)
  into same TDC channel
  (multi-hit TDC)
- TDC bin width
  $\Delta t$=100 ps
  sufficient for 3$\sigma$
  lepton/$\pi$ separation
  (flight path factor ~2
  larger than FOPI)



# The HADES RPC Detector

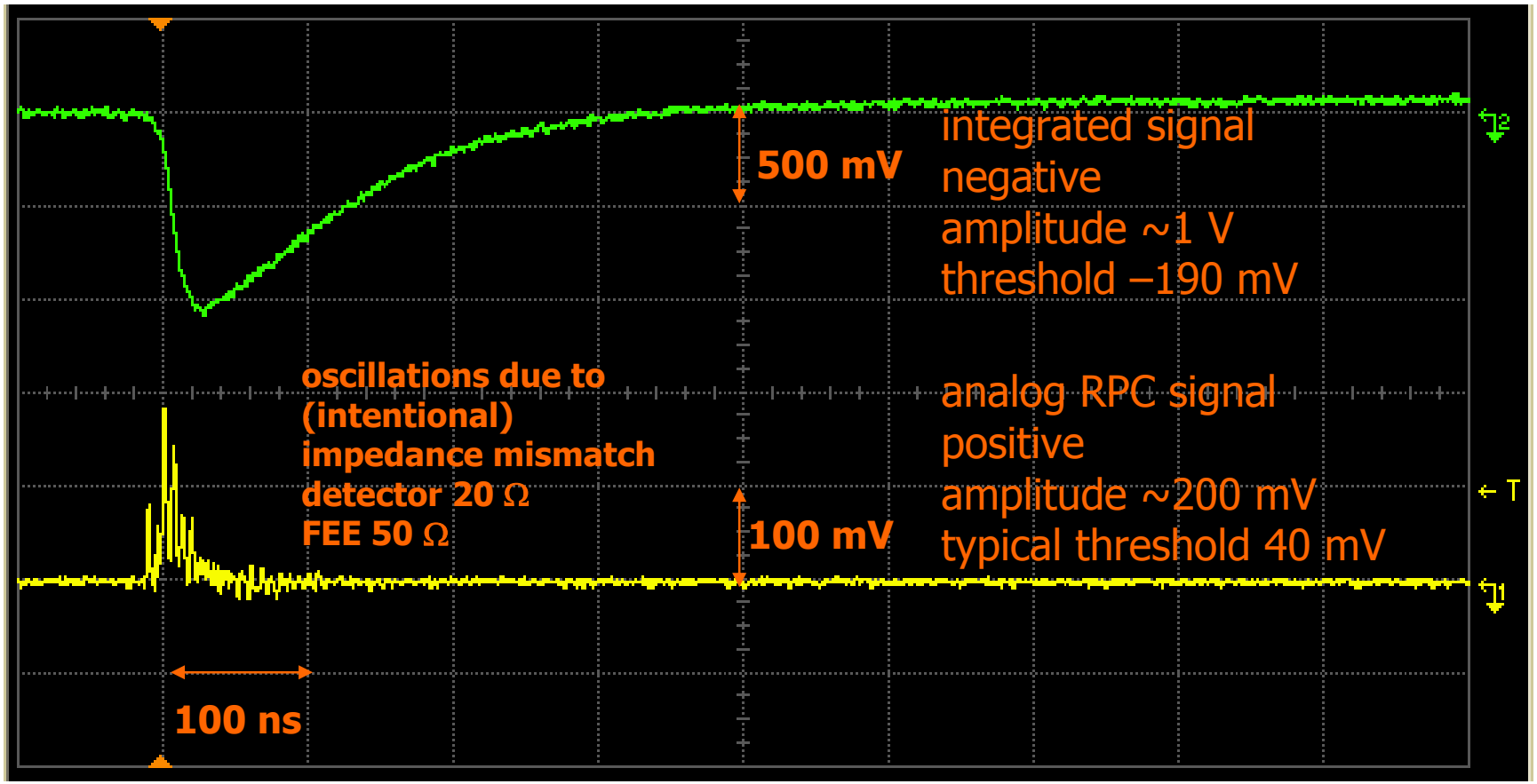


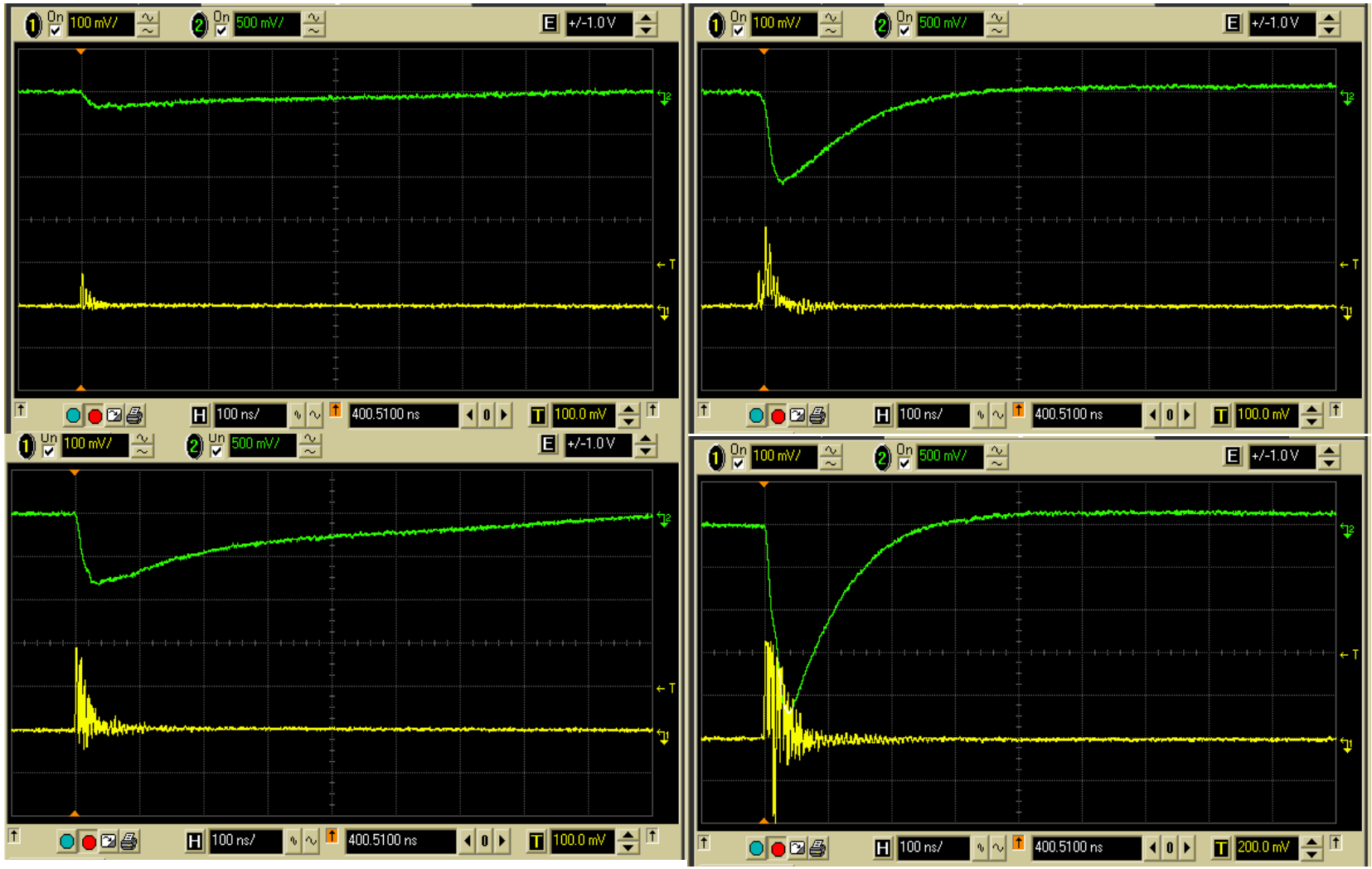



**4 gaps**

# An RPC signal.



# RPC Signals with different amplitudes.



# Frontend Design Considerations.

- high frequency boards

  <1 kHz / $cm^2$ RPC area
  x 100 $cm^2$ = 100 kHz
  x 31 channels = 3.1 MHz firing

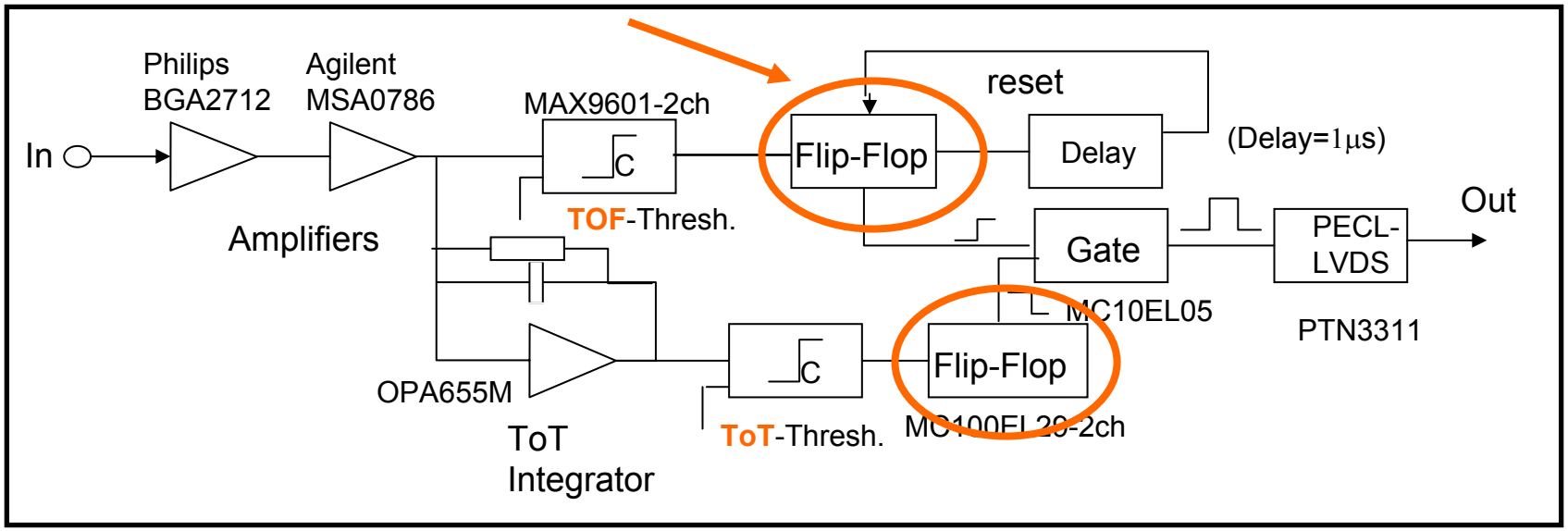
  power-to-ground has GHz components
  due to switching $\Delta t \leq 1$ ns

  requirements:

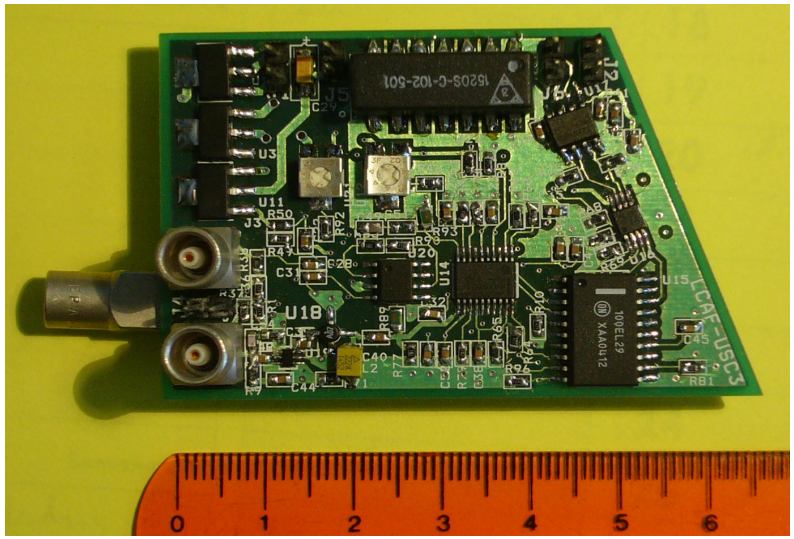
  - fast risetime
  - high frequency design rules (no sharp edges etc.)
  - many filter capacitors

- all signals = LVDS = low voltage differential signal

# DB STEP2 (Previous Iteration until 12/2004)



# DB STEP2 (previous iteration until 12/2004)



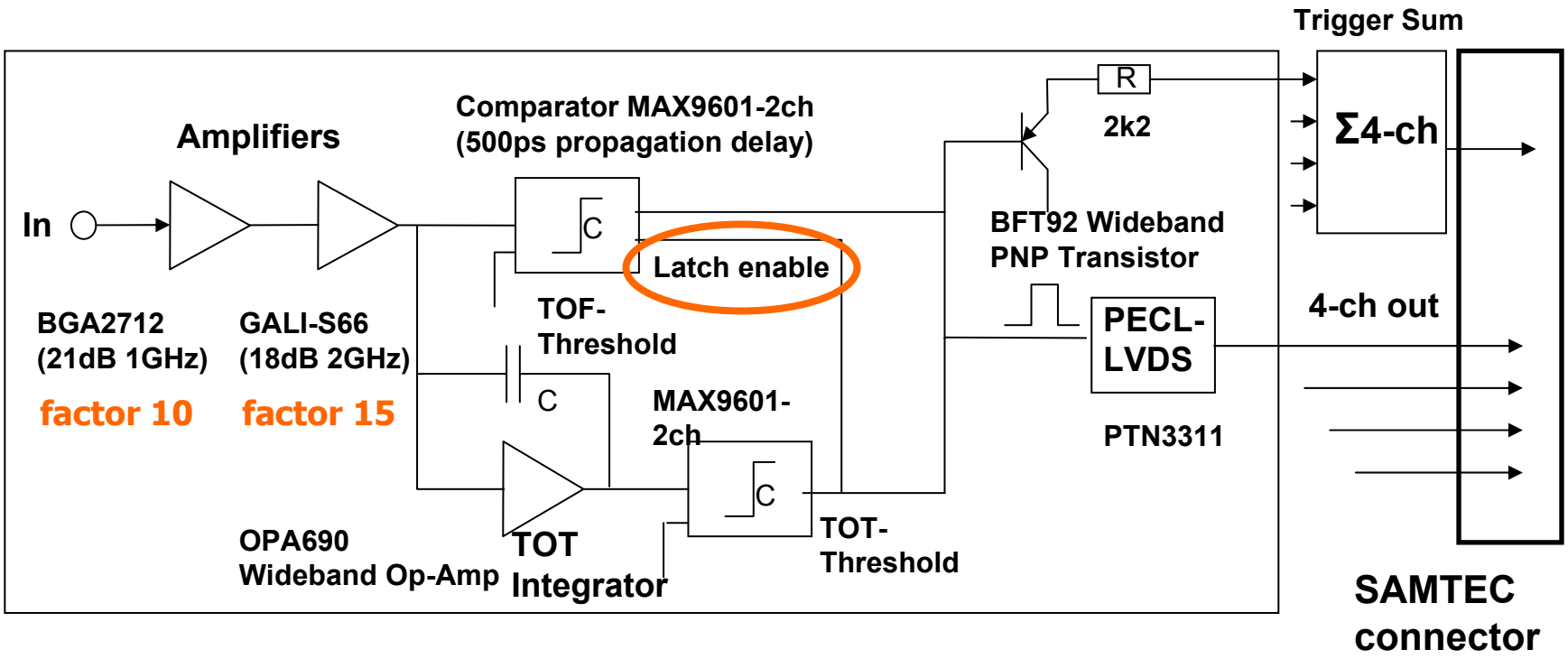

2-ch / 1 FEE

# From STEP2 to STEP3

- **STEP2**
  - long dead-time (1 us)
  - start/stop LVDS signal (flip-flop) by 1 signal (non-differential)
    $\rightarrow$ difficult if noise
  - concept of flip-flop + delay was adjusted
    to standard TDC concept
    but obsolete by choice of CERN HPTDC
    (free-floating adjustable fire-window
    even before external trigger)

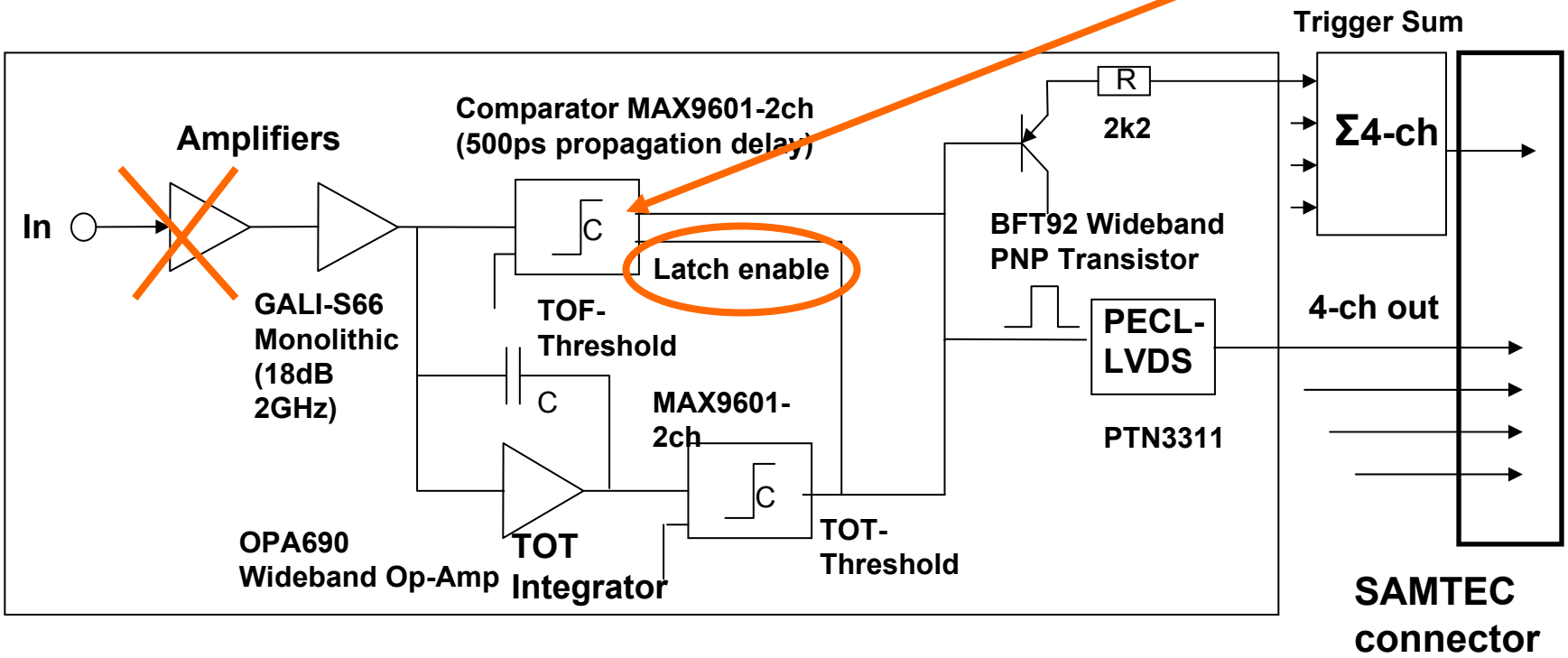
- **STEP3**
  - use comparator with latch-enable
  - advantageous side effect: 3 components less
    (more space available > 4 channels / 1 DB became feasible)

# DB FEE STEP3 (Previous Iteration until 08/2005)



# DB STEP4 (now)
## (minor changes)

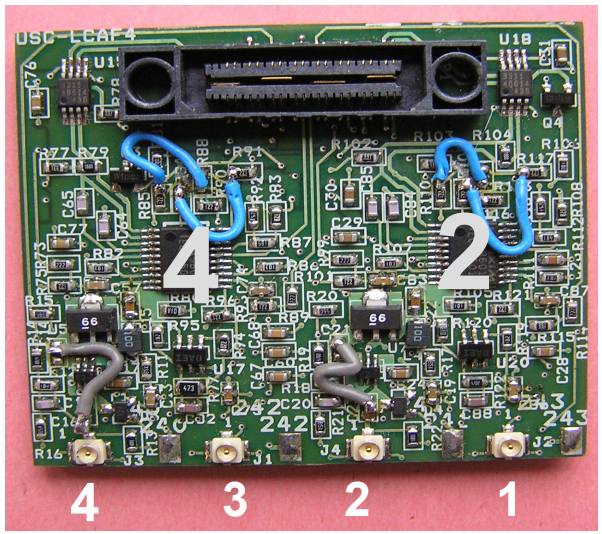
comparator hysteresis now ΔV=8 mV

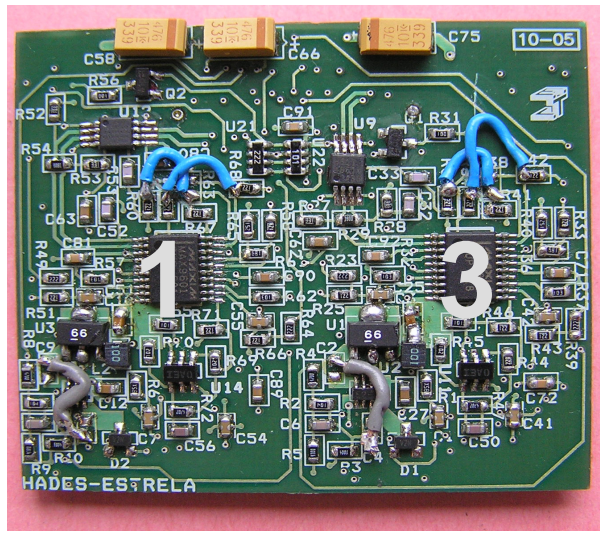



RC of TOT 2 ns (keep short to avoid ionic tail)

RC of Latch 20 ns

# DB FEE STEP4 (now)




μLEMO input from detector

# Pre-Amplifiers

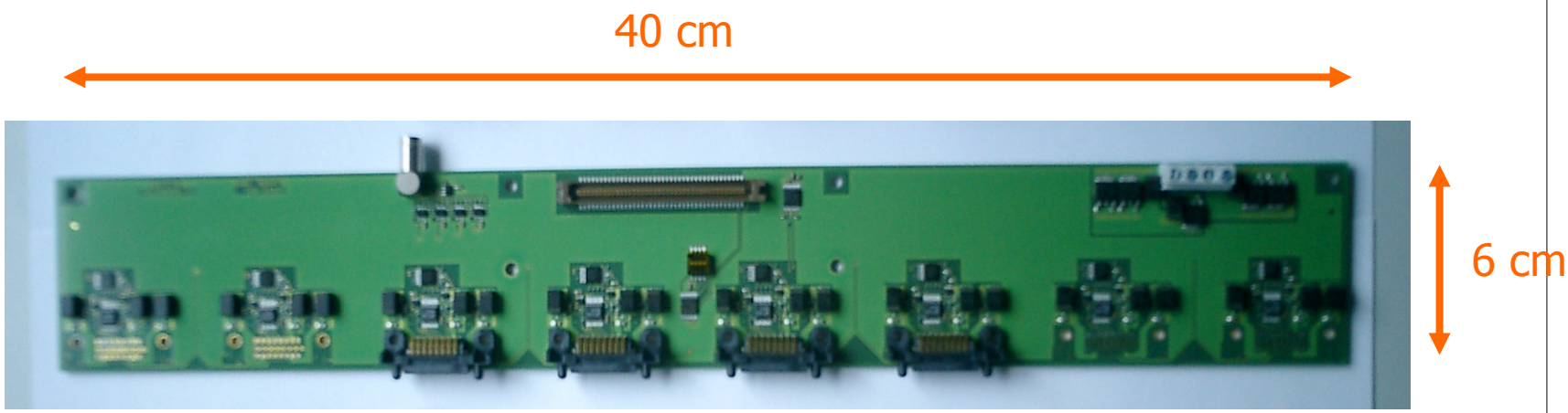
- impedance mismatch amplifies signal in a „natural" way
  ~factor 2.5 (20Ω/50Ω)
- STEP4
  only 1 pre-amp is sufficient
  - not 2 (HADES pre-final version)
  - not 3 (FOPI)
- choice: GALI-S66 by Mini-Circuits (same as FOPI)

| | BGA2712 | GALI-S66 |
|---|---|---|
| - wideband | ≤3.2 GHz | ≤8 GHz |
| - noise figure | 2.7dB (factor 1.86) | 3.9dB (factor 2.54) |

noise figure = ratio of amplification of noise output/input

- operate @ gain 15

# The Motherboard (MB)



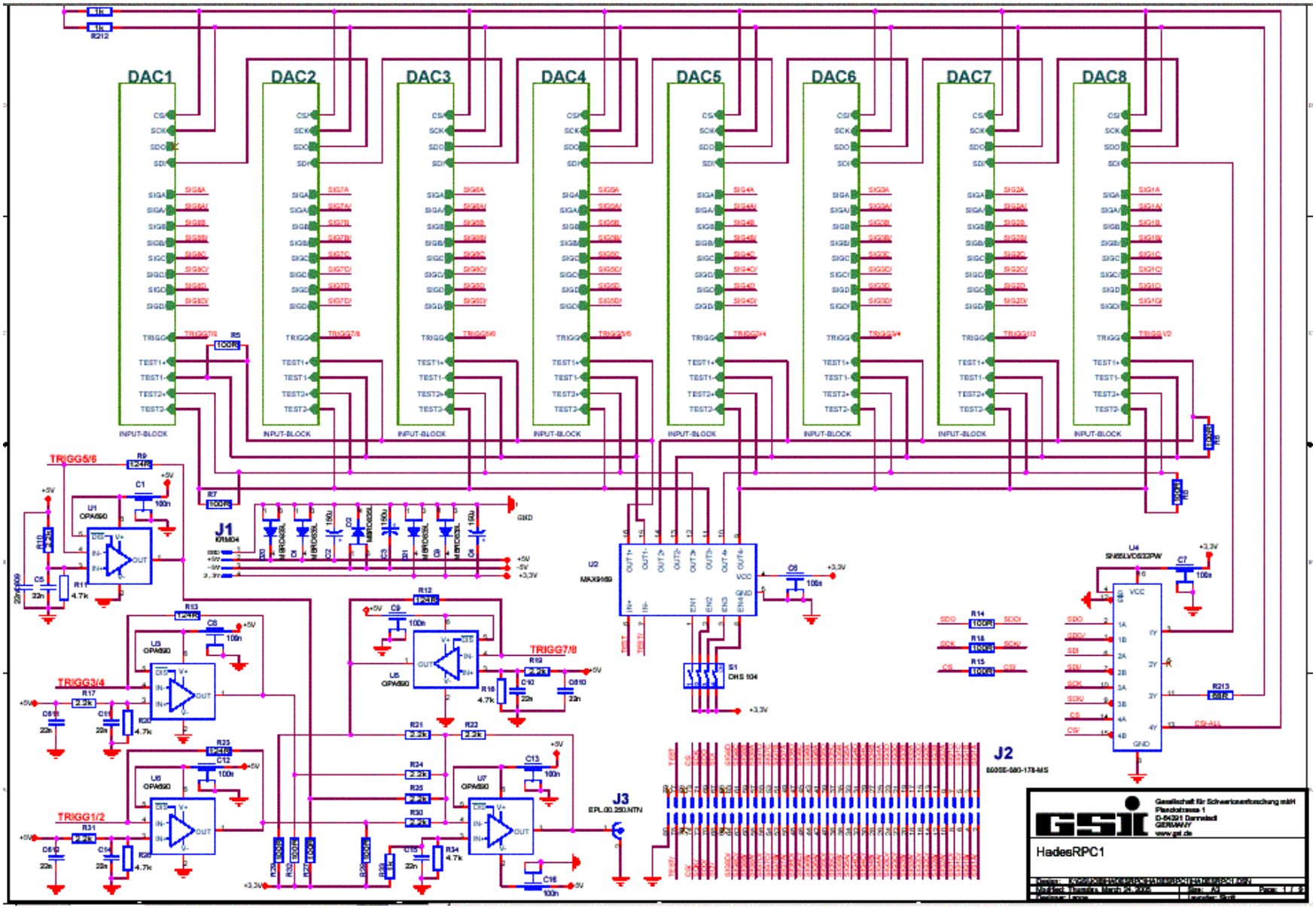

top/bottom appears empty, but it is not:
8-layers, in 3-dim (with vias) completely full (<6 cm not possible)

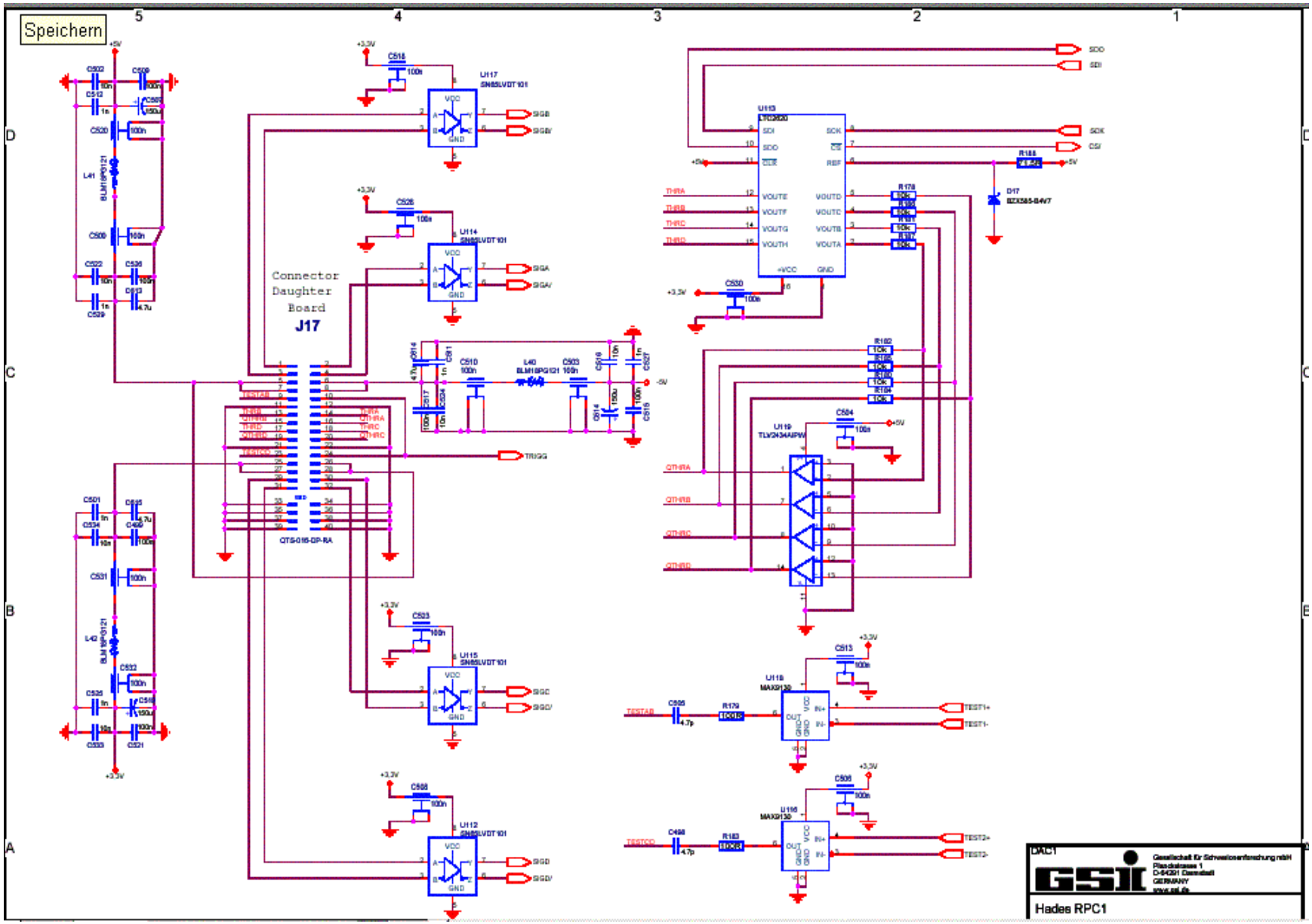
note: 8 DB per 1 MB, but only 31 channels
because TDC needs 1 channel for START

# 4 Main Tasks of the MB

- 1. supply stable voltage to DB
  +5 V
  +3.3 V
  -5 V
- 2. get logical signals (TOF and TOT) from 8 daughterboards and concentrate to 1 connector
  (then twisted pair HITACHI cable to TDC board)
- 3. generate multiplicity signal for trigger
- 4. set thresholds on DB
  for TOF and TOT
  use programmable DAC chips

- And a few minor tasks:
  multiplex/fan-out test signals 1→16 (from TDC board),
  invert polarity of TOT thresholds,
  LVDS repeaters etc.


DAC1
DAC2
DAC3
DAC4
DAC5
DAC6
DAC7
DAC8
INPUT-BLOCK
J1
J2
J3
TRIGG5/6
TRIGG7/8
TRIGG3/4
TRIGG1/2
HadesRPC1


Speichern
Connector
Daughter
Board
J17
Hades RPC1
GSI

# 8-layer
# total thickness d=1.438 mm

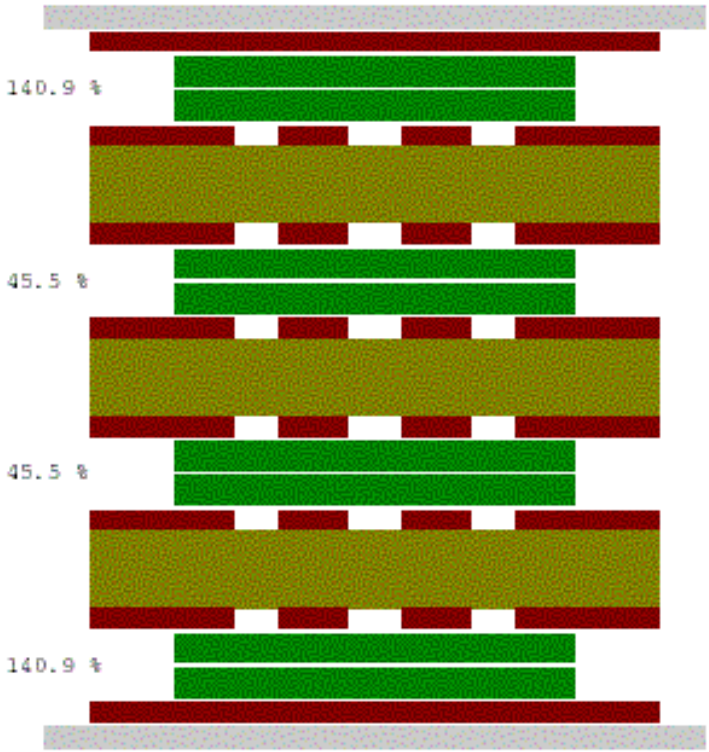
TTL Test Signals

GND
differential pair

+3.3 V
+5 V

differential pair
GND

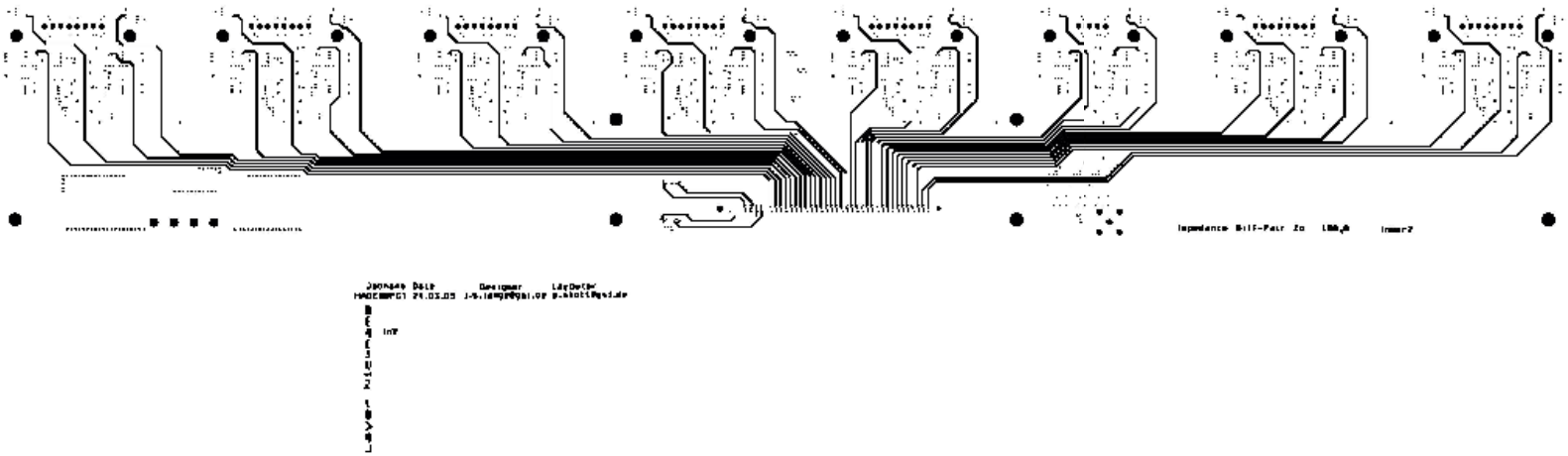
-5 V




5µm 100%
99.1 µm (2125 [AT 01])
99.1 µm (2125 [AT 01])
18µm 70%
200 µm [ 1x7628M]
18µm 50%
99.1 µm (2125 [AT 01])
99.1 µm (2125 [AT 01])
18µm 70%
100 µm [ 1x2116 ]
18µm 70%
99.1 µm (2125 [AT 01])
99.1 µm (2125 [AT 01])
18µm 50%
200 µm [ 1x7628M]
18µm 70%
99.1 µm (2125 [AT 01])
99.1 µm (2125 [AT 01])
5µm 100%

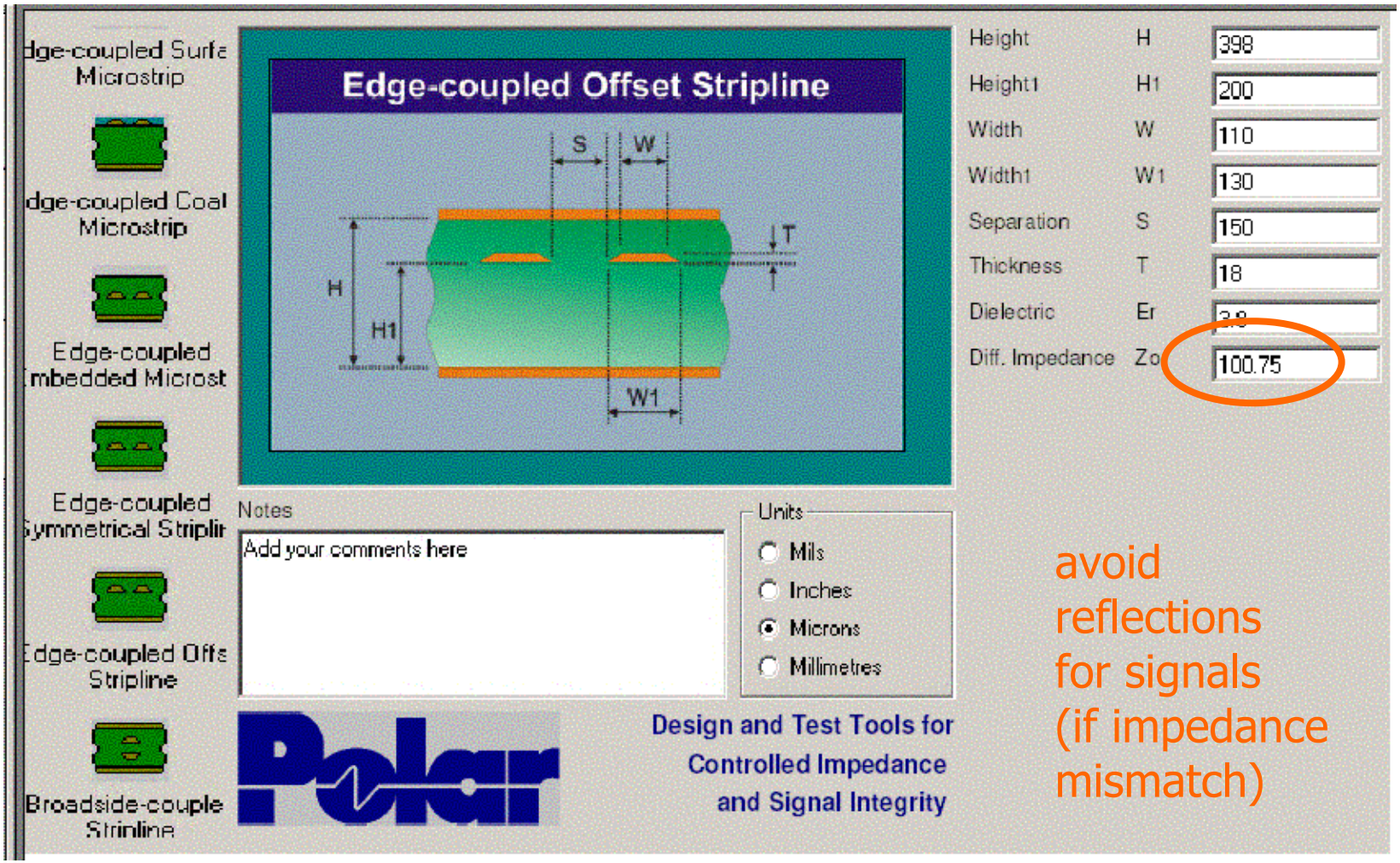
198.1 µm
198.1 µm
198.1 µm

# Layer 3 (from top): signals, differential routes

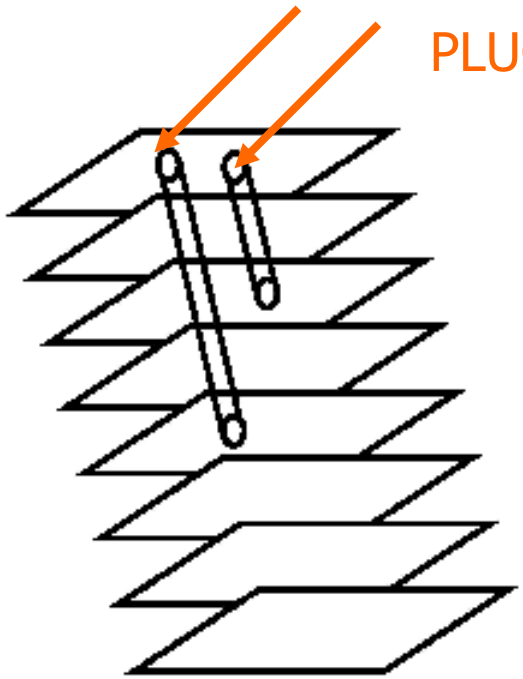


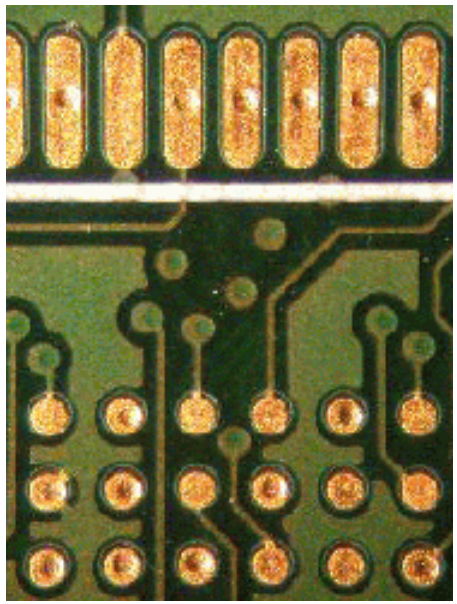
| | |
|---|---|
| 150 μm | in-pair trace-to-trace |
| 450 μm | pair-to-pair |
| 130 μm | trace thickness |

# Special Board Features #1: 100 Ω Impedance Matching



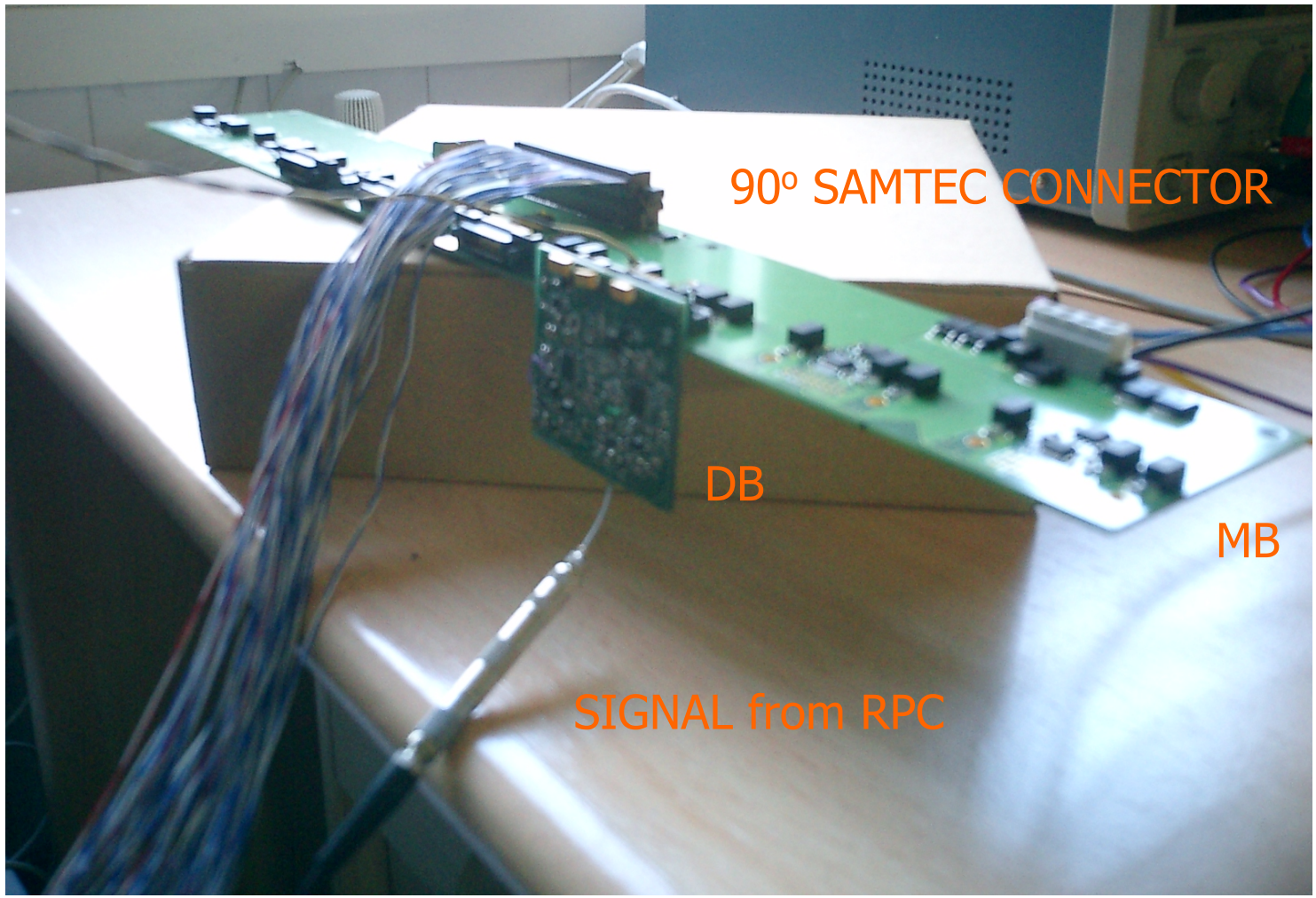
# Special Board Features #2: Plugged Vias



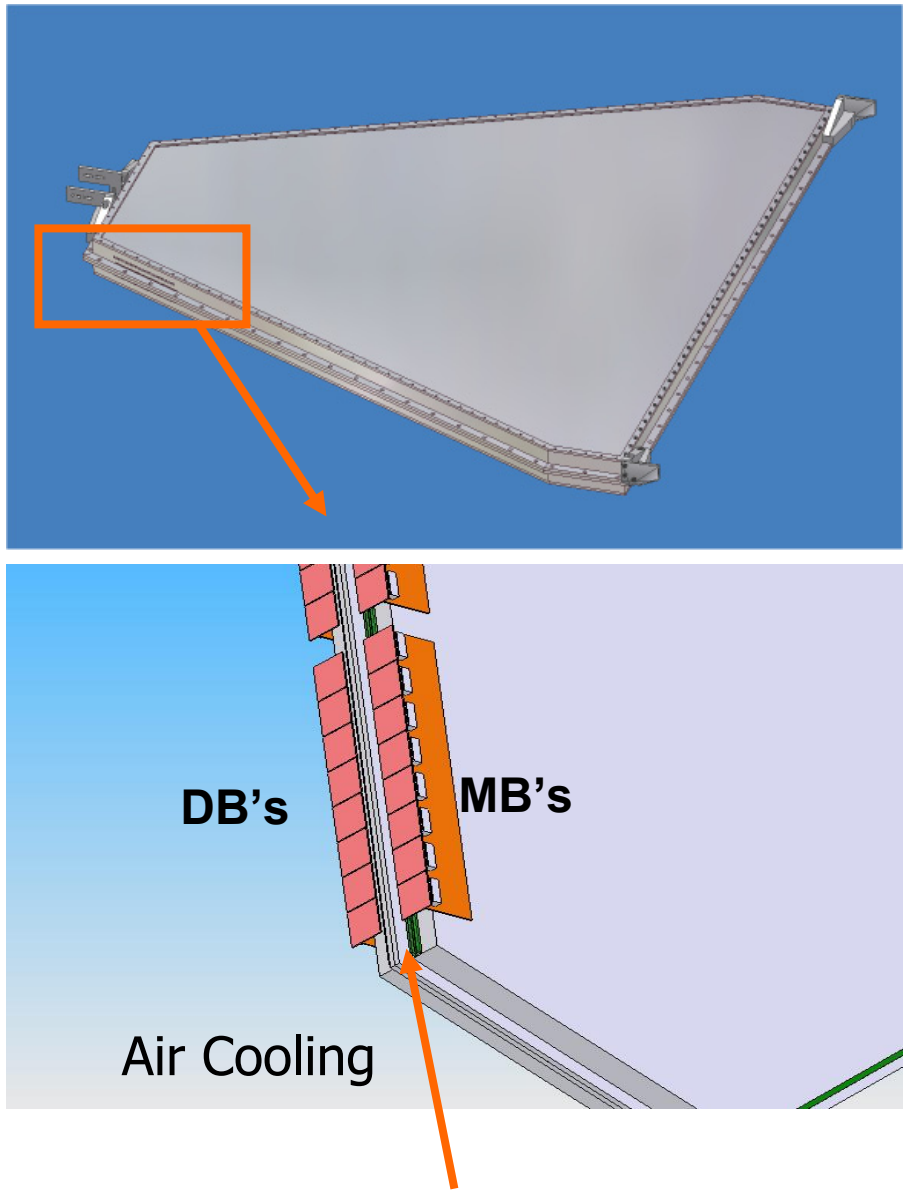



quite new (~1 year), only 2 PCB manufacturers in Europe
makes 6 cm MB width possible
(otherwise PCB and RPC would overlap)

# DB and MB

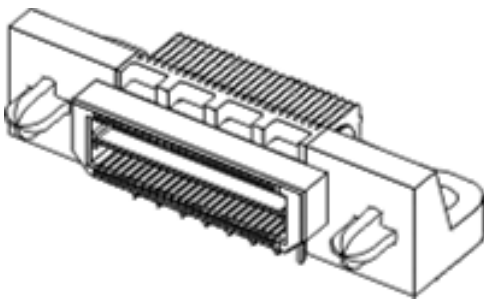


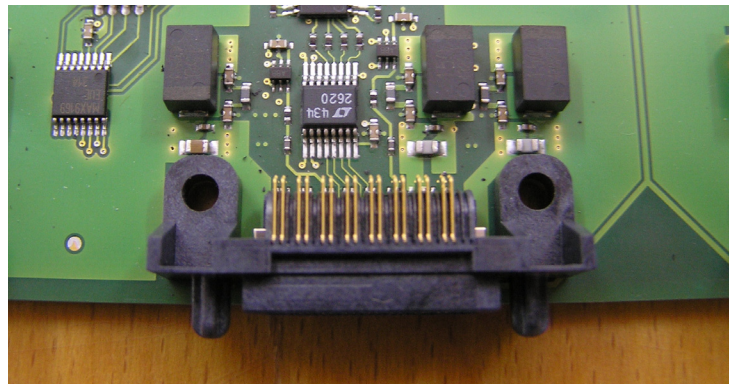
RPC Gas Box
(LIP-Coimbra,
P. Fonte et al.)



# Special Board Features #3: The SAMTEC connector

- between DB and MB
- small pitch 0.635mm
- right-angle 90° on MB side
  DB „hanging"
- differential
  every 3rd pin missing
- „high-speed" series
  @2 GHz
  impedance mismatch <10%
  crosstalk <3.6%

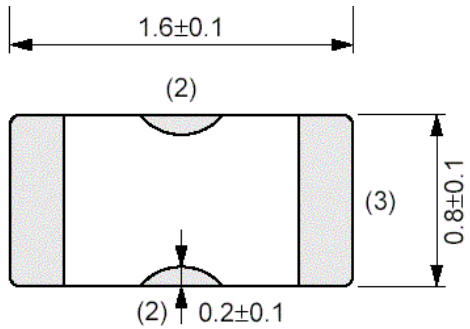


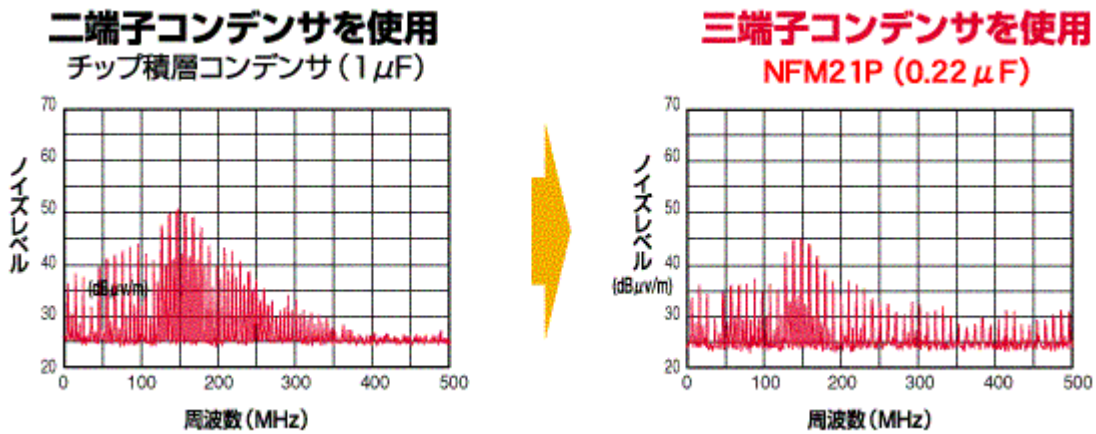


| | | | |
|---|---|---|---|
| TOF/TOT A low | 2 | 1 | TOF/TOT B low |
| TOF/TOT A high | 4 | 3 | TOF/TOT B high |
| -5 V | 6 | 5 | +5 V |
| -5 V | 8 | 7 | +5 V |
| mult-4 | 10 | 9 | Test Signal A/B |
| GND | 12 | 11 | GND |
| Threshold TOF A | 14 | 13 | Threshold TOF B |
| Threshold TOT A | 16 | 15 | Threshold TOT B |
| Threshold TOF C | 18 | 17 | Threshold TOF D |
| Threshold TOT C | 20 | 19 | Threshold TOT D |
| GND | 22 | 21 | GND |
| (mult-4) | 24 | 23 | Test Signal C/D |
| +5 V | 26 | 25 | +3.3 V |
| +5 V | 28 | 27 | +3.3 V |
| TOF/TOT C low | 30 | 29 | TOF/TOT D low |
| TOF/TOT C high | 32 | 31 | TOF/TOT D high |

# Special Board Features #4: The MURATA super filters

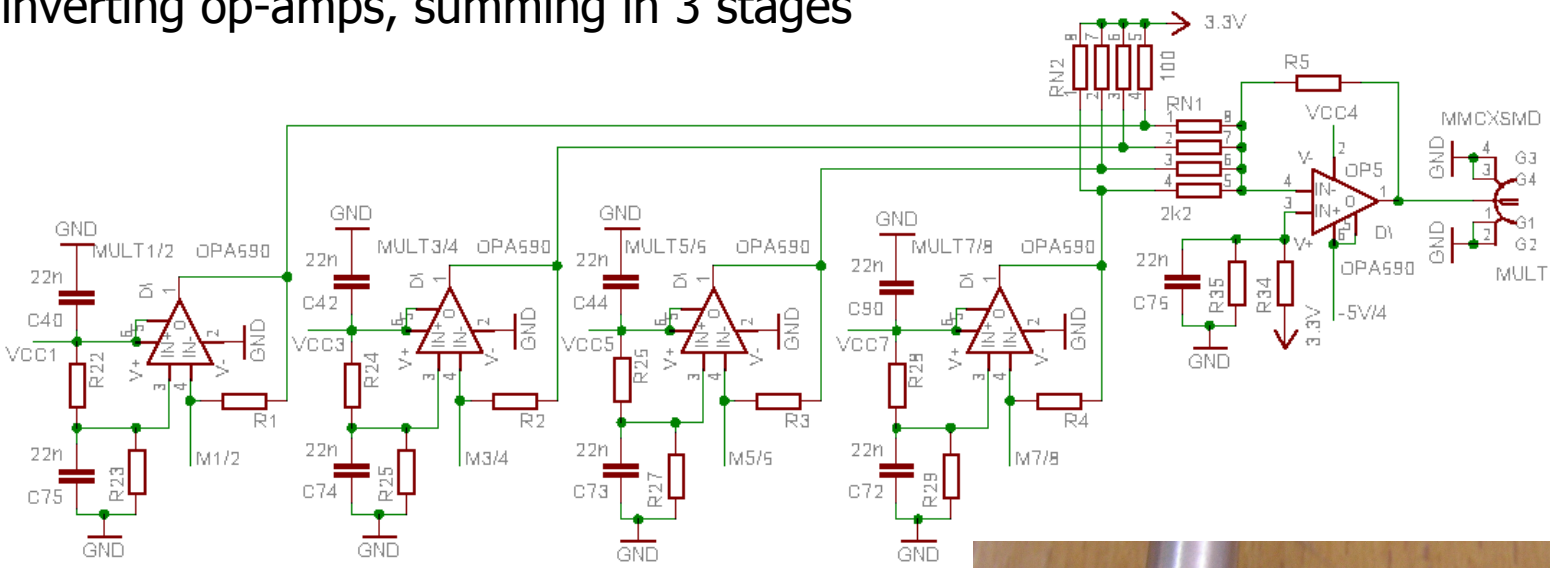
- NFM18PC
- multilayer ceramic
- 0603 size
  but unusual layout
- 2A high current
- low residual ESL
  i.e. factor ~10 smaller than
  comparable monolayer ceramic

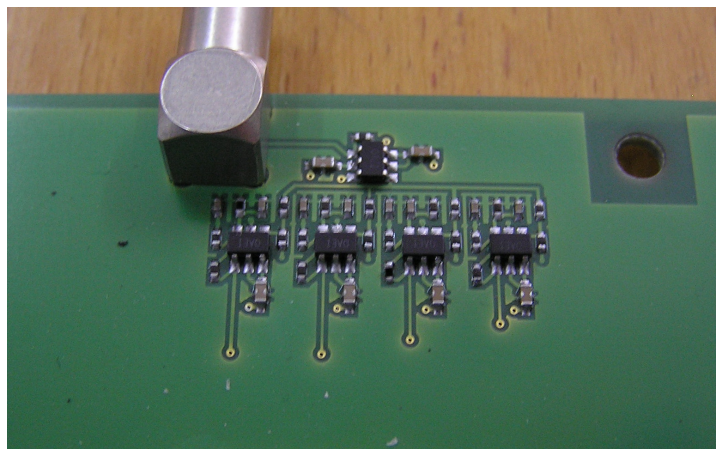


# Trigger

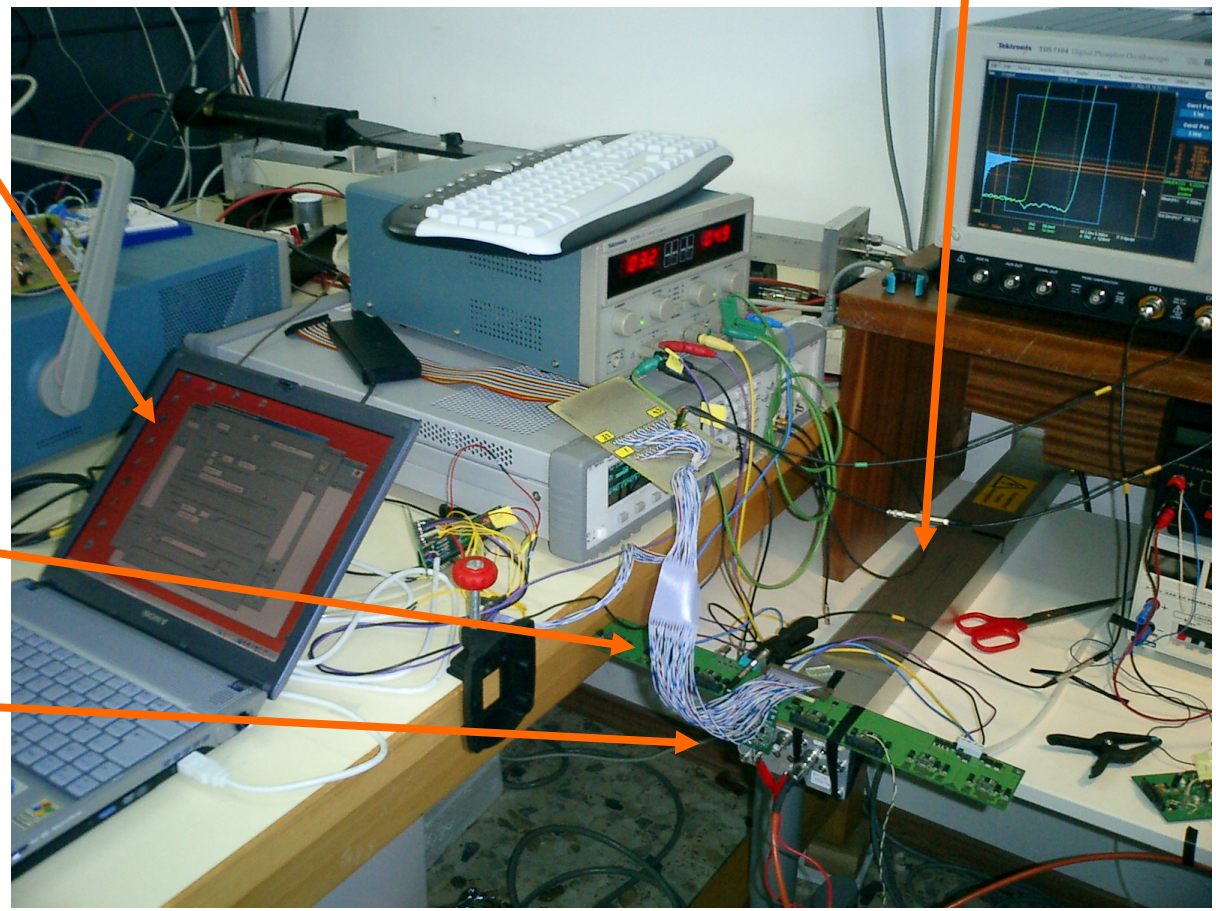
inverting op-amps, summing in 3 stages



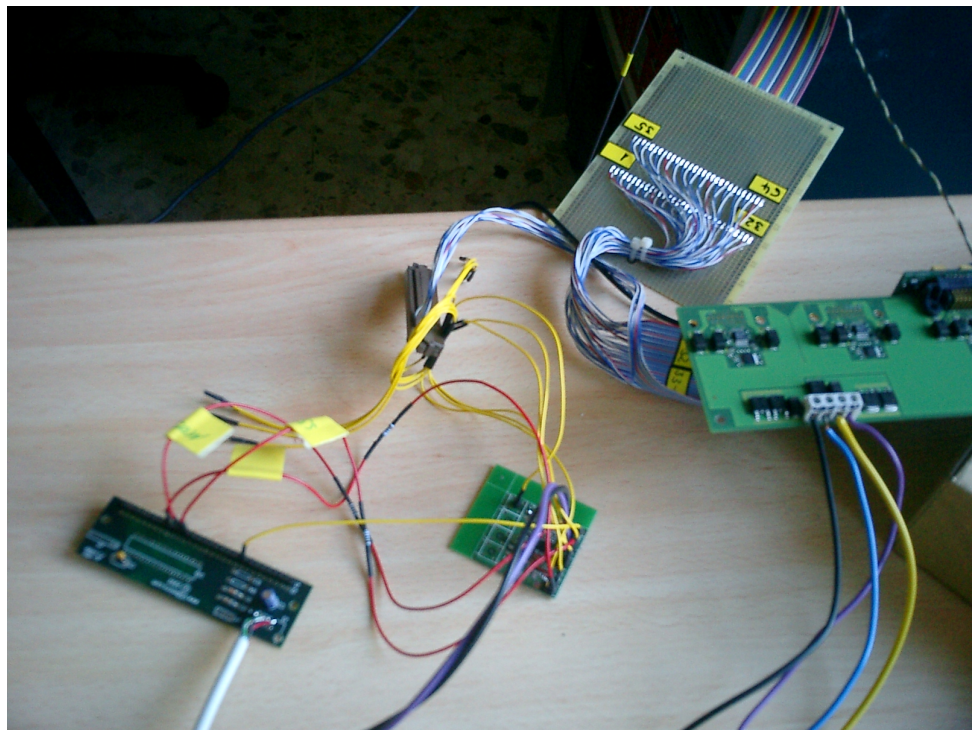
note: all resistors are on PCB top
→ easily exchangeable (if necessary)

# The Santiago Test Setup (May and August 2005)



# Slow Control

- SPI (serial peripheral protocol)
  62 kBit/s
- 1 DAC per 1 DB
- all DACs in daisy chain
- for Santiago test:
  connected to laptop
  (USB-SPI interface
  plus TTL-LVDS converter)
- plan for Nov test:
  by ETRAX chip
  (= single chip LINUX PC)
  on TDC board



# Results

- Time jitter
  42-48 ps FWHM
  (factor √2 due to
  start/stop with same signal)
- Crosstalk
  - 20 ns pulses
  - 450 mV (higher than nominal)
  - 2 μs puls-to-puls
  - neighboured channels
    on DB and MB

  no other channel fired
  in ~6.5 Mill. Events
- Propagation delay
  ≤5 ns

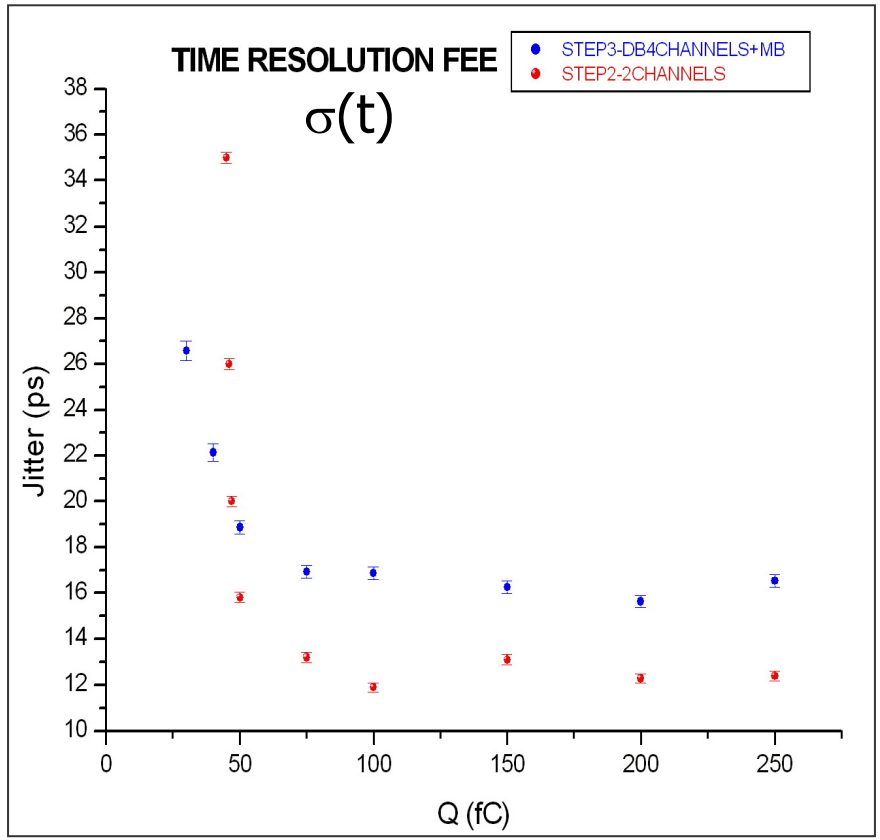
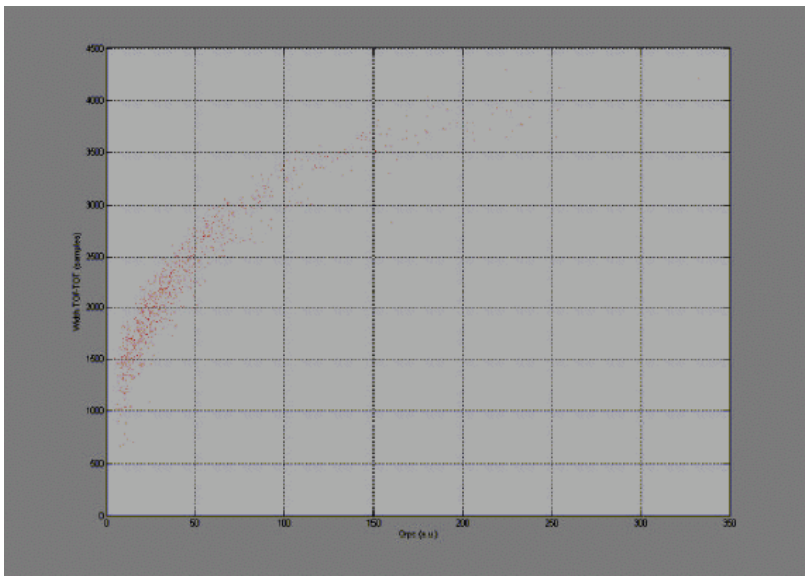


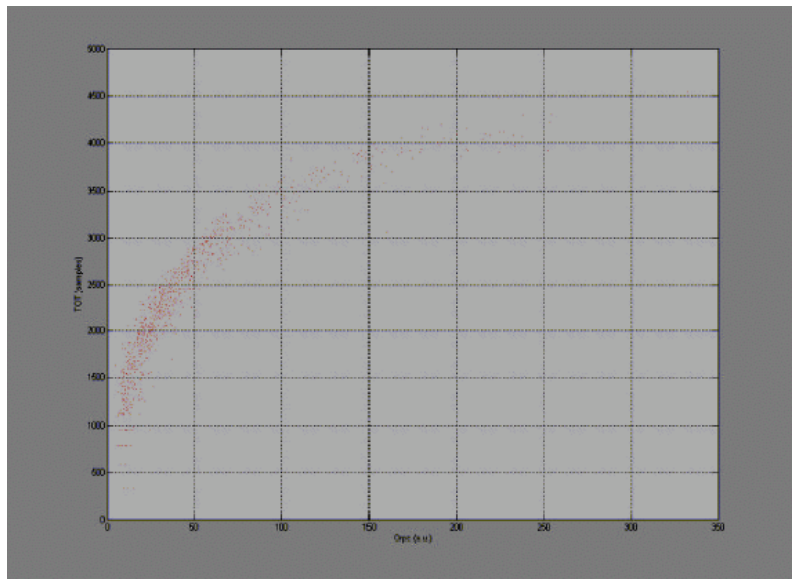

Fig.11- Time Jitter con pulser STPE3 vs. STEP2.

# TOT results from LIP test

- TOF+TOT
  (= length LVDS signal)

TOT only





charge (a.u.)

charge (a.u.)

# The RPC Power Supply Board (RPS)

- former concept (e.g. HADES drift chambers)
  LV (e.g. +5V) from power supply over long cable (10 m)
  to LDOs at the detector
  common ground
- new concept:
  point-of-load
  supply +48 V with low current over 10 m cable
  then use DC-DC converters with wide input voltage range (35-70 V)
  (and get high current)
- LDOs ?
  recent DC-DC converters have comparable ripple and stability
  ~20-50 mV
- ground loops ? No.
  Use galvanic separation.
- Use MURATA filters
- Use MURATA ferrit beads

# The RPC Power Supply Board (RPS)

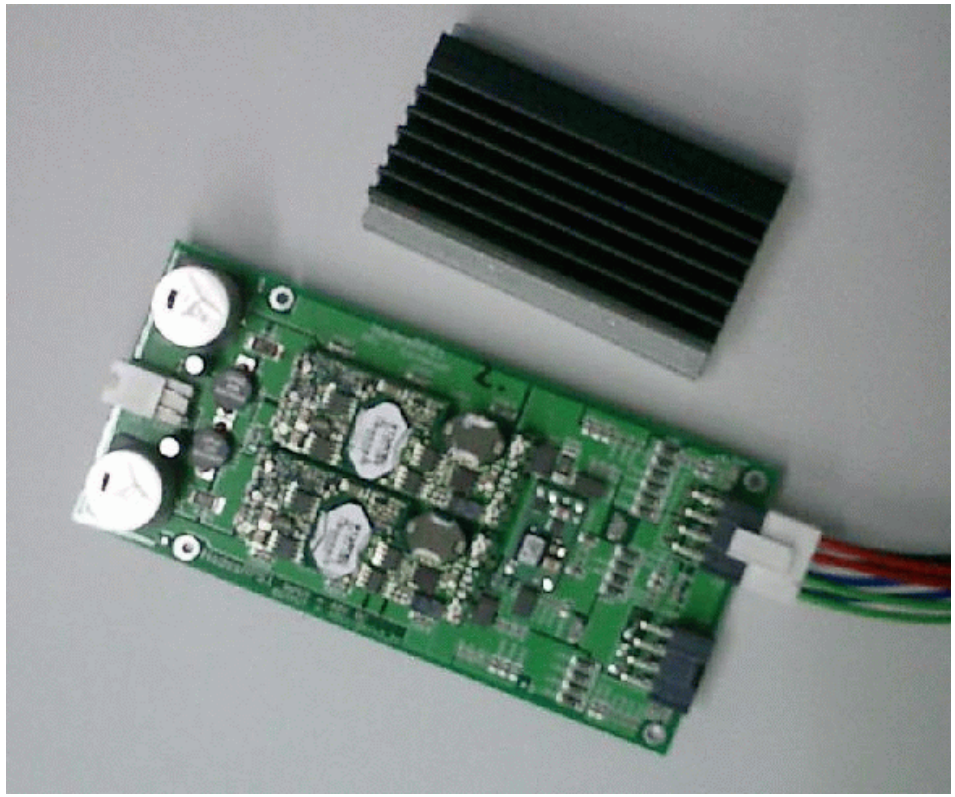
- input +48 V
- output –5, +3.3, +5 V
- ripple

  DATEL ULE-5/12-D48P
  48V → +5 V, -5 V (12 A)
  ±50 mV ripple peak-to-peak

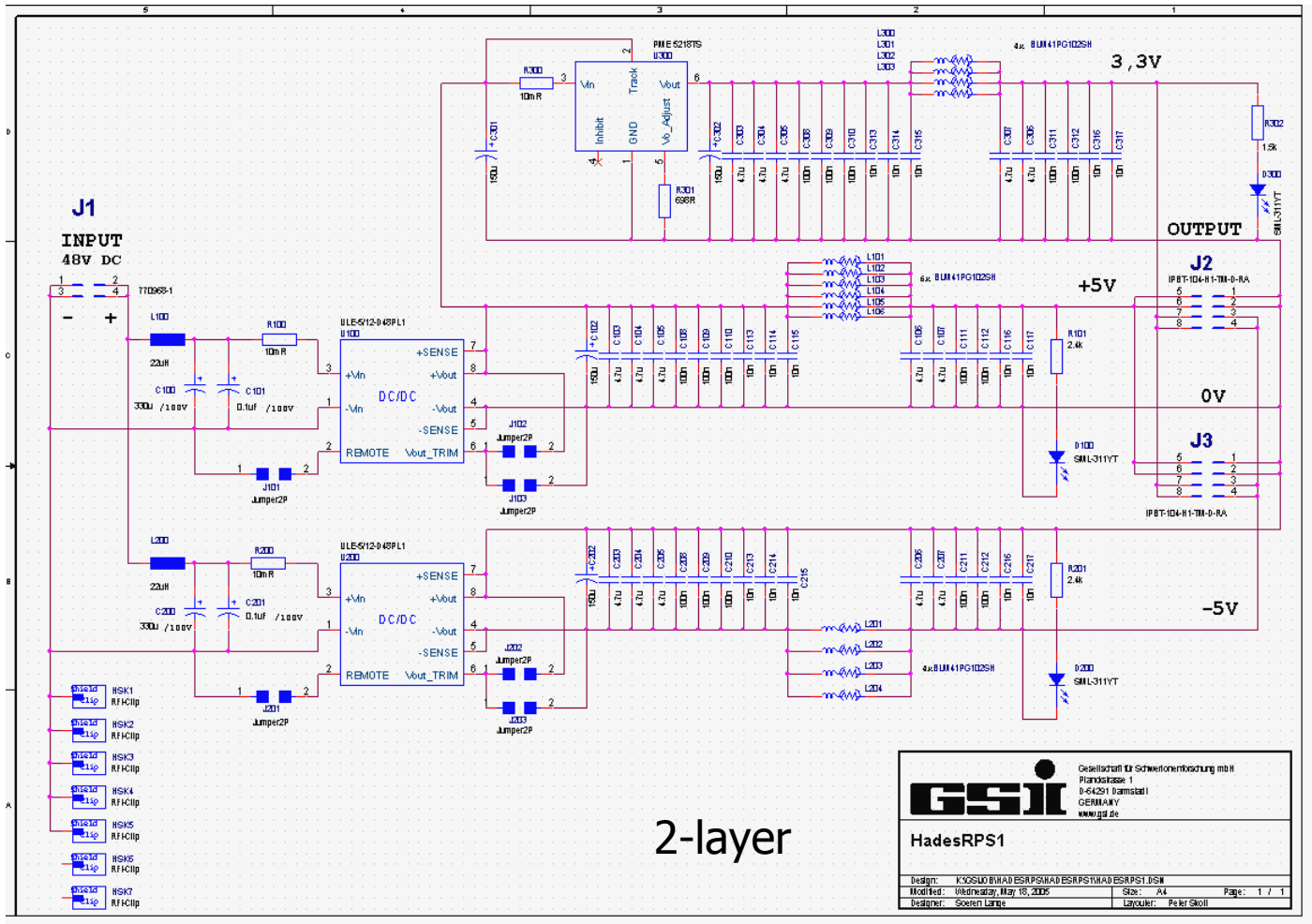
  POLA PME5218T
  +5 V → +3.3 V
  ±20 mV ripple peak-to-peak

- shielding box

- between chip and shielding:
  Bergstrom material
  (electric conductivity zero,
  heat conductivity high)

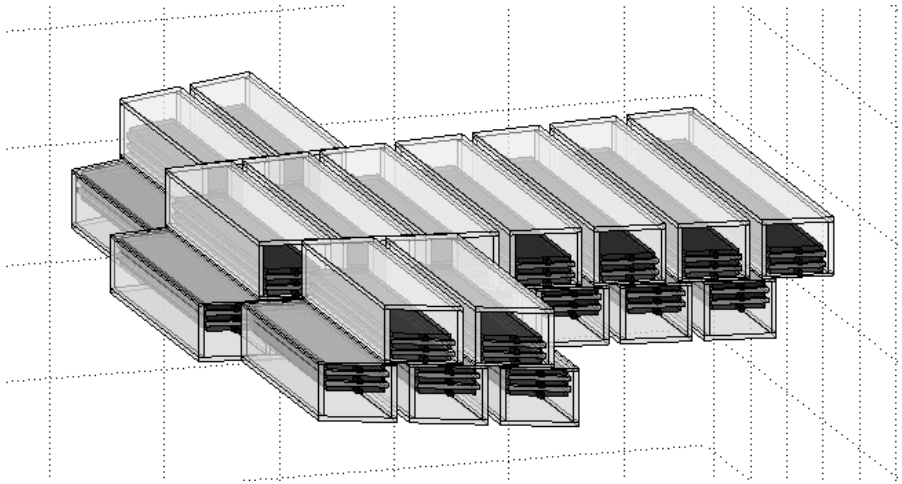


# The RPC Power Supply Board (RPS)



# Outlook

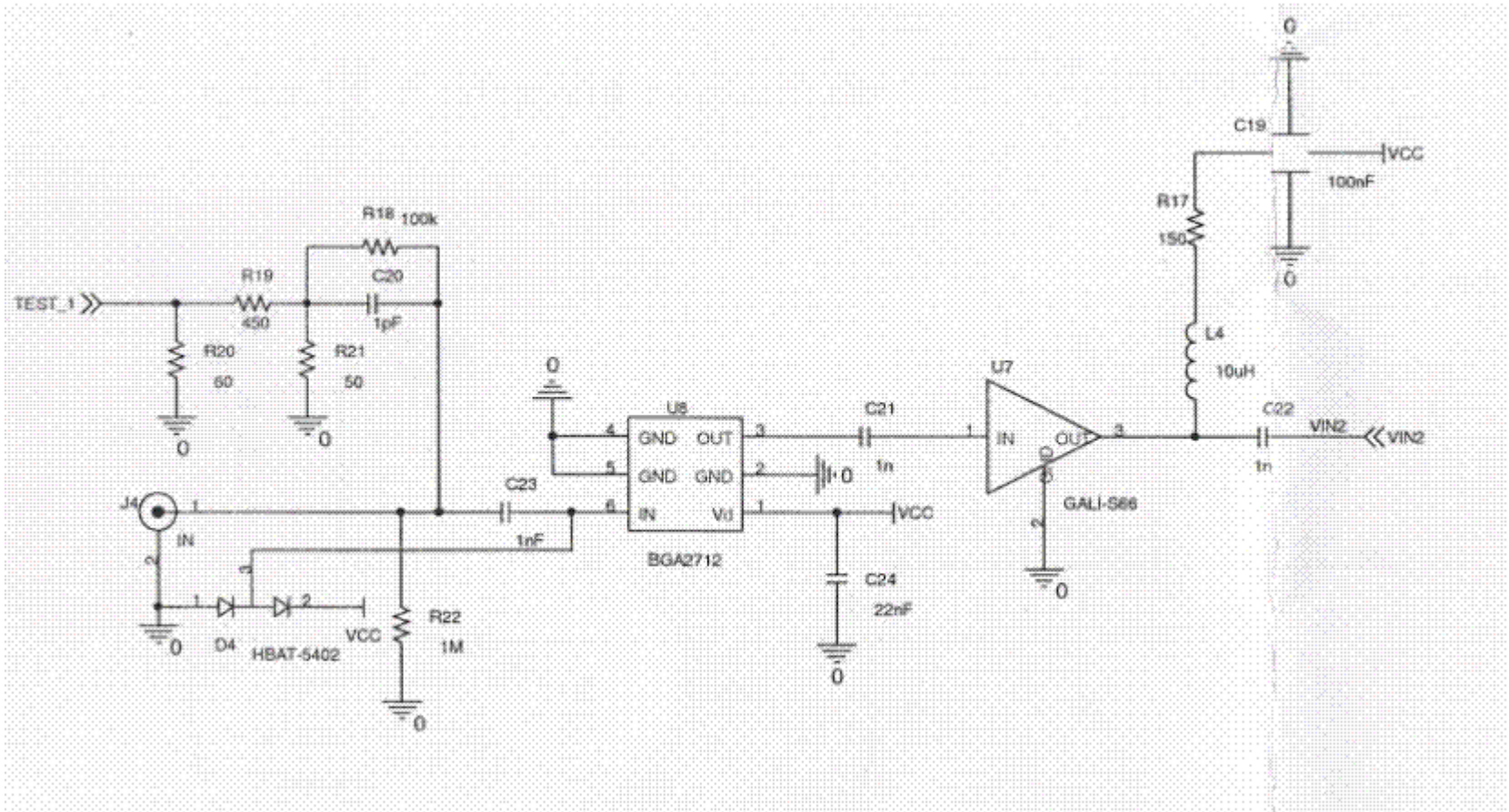
- Test in Beam at GSI in Nov 2005 (800 MeV/c $^{12}C$)
  24 detectors, full chain readout (DB+MB+TDC Board)
- Supported by EU under FP6 program (#515876)



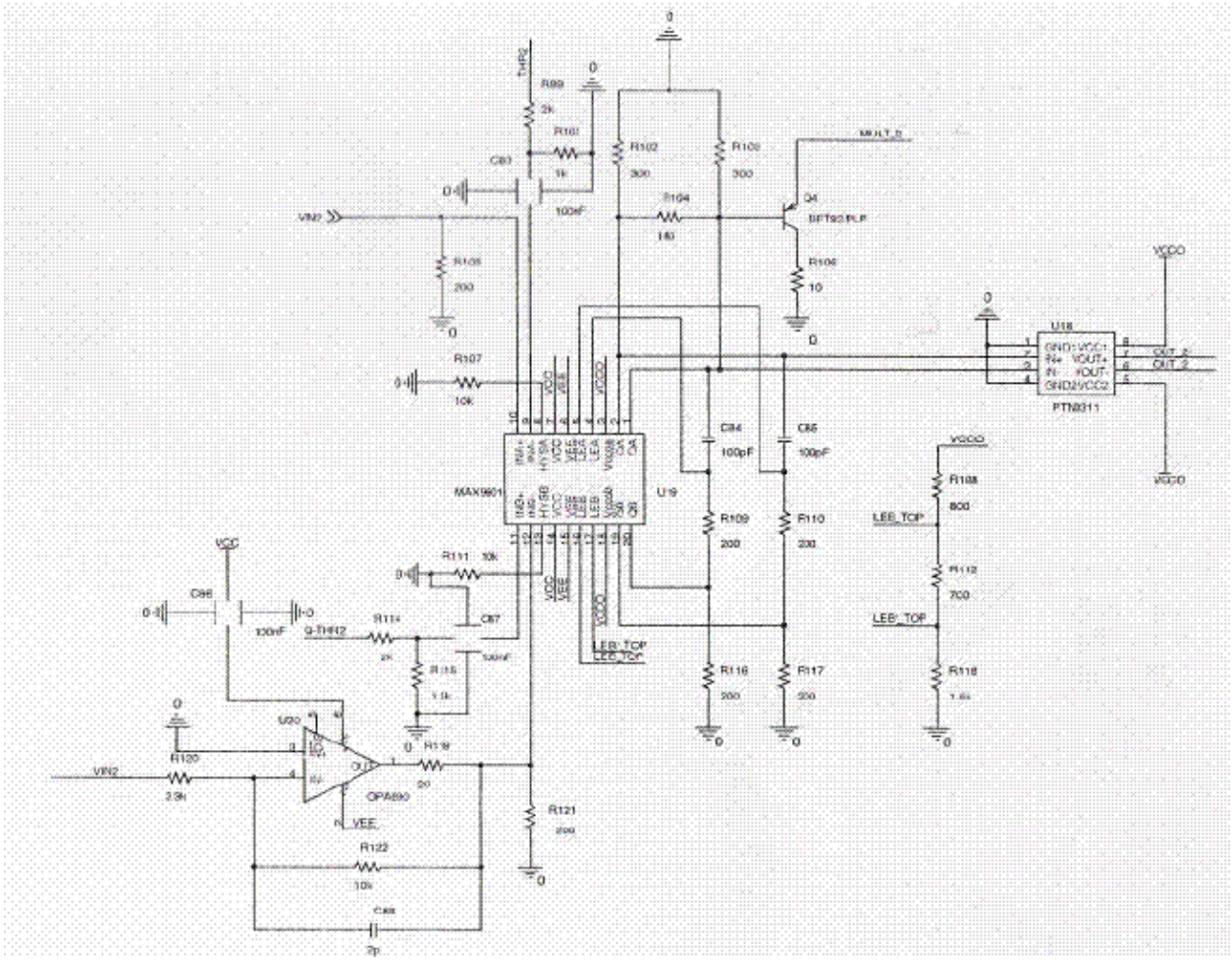
Acknowledgements:
LIP/Coimbra Detector Group: P. Fonte et al.
GSI DVEE: G. Eidmann, M. Wiegand
FOPI RPC Group: M. Ciobanu, K. Koch, A. Schüttauf

Additional Slides

# DB schematics #1 (Pre-Amp)



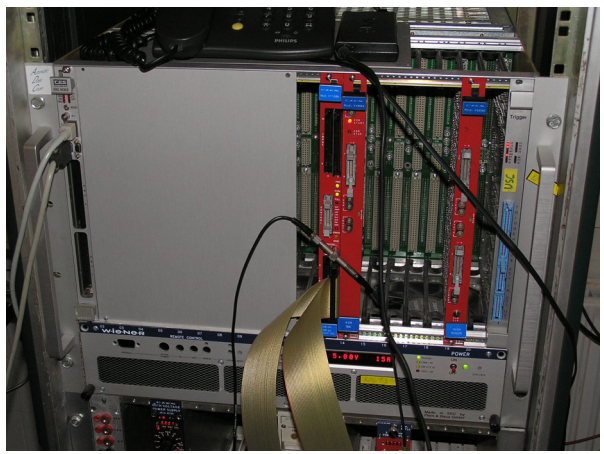
# DB schematics #2 (Comparator)

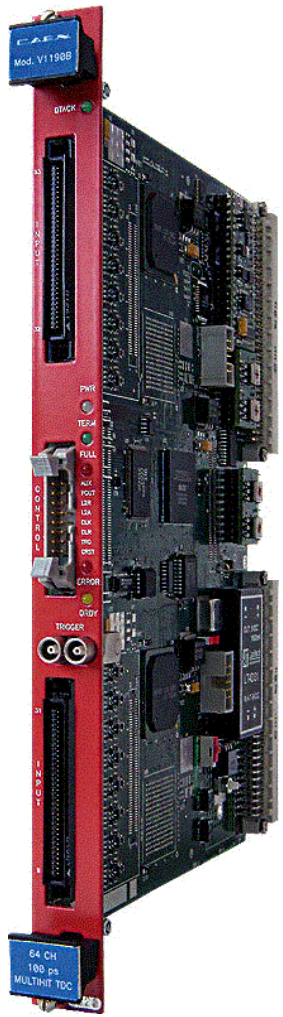


# CAEN TDC (used for Santiago Test)

- 128-ch in 1 slot VME module
- multi-hit (pipe-lined)
- 100 ps bin width
- same CHIP as TRB: HPTDC
- VME readout:
  self-written stand-alone
- TDC can fire **before** trigger
  (adjustable windows
  by registers through VME)
  → delay cable obsolete

RIO-2 LynxOS



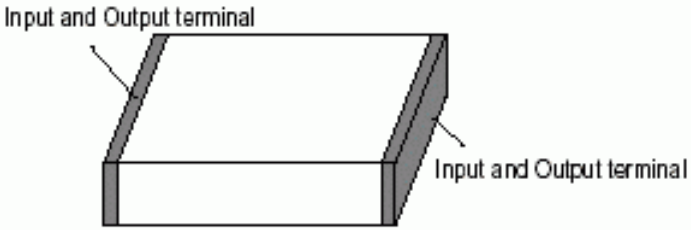


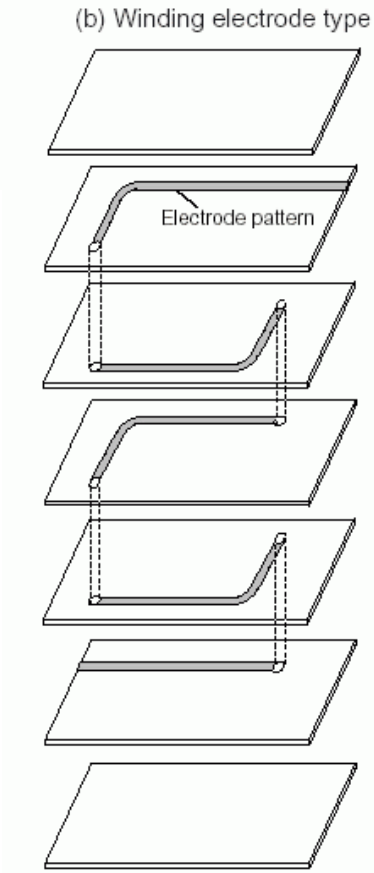
# The RPC Power Supply Board (RPS)

- filtering noise

- MURATA filters (see above, MB, we had to buy 4000 anyway)

- in addition:
  MURATA ferrit beads
  inductance at low frequencies
  resistor at high frequencies
  (1kΩ at 100MHz)
  resistor = „real" part of impedance
  = dissipates high frequency noise as heat
  high current 1.5A = O.K.



# How to measure time jitter.

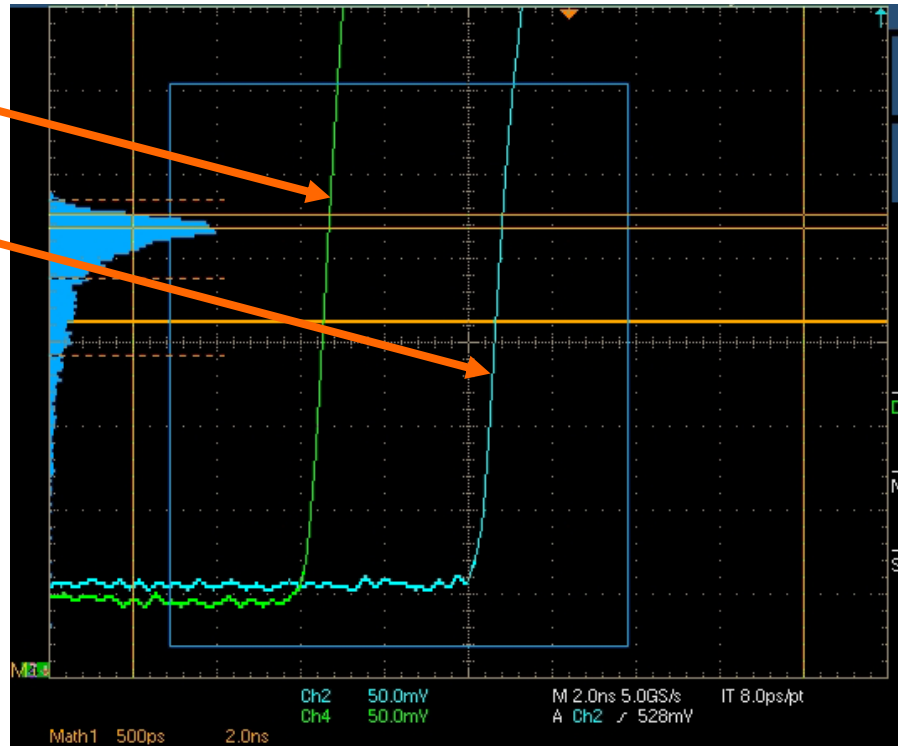
# Measurement of Jitter (DB+MB) with RPC Signals

2 LVDS signals

- from RPC near end

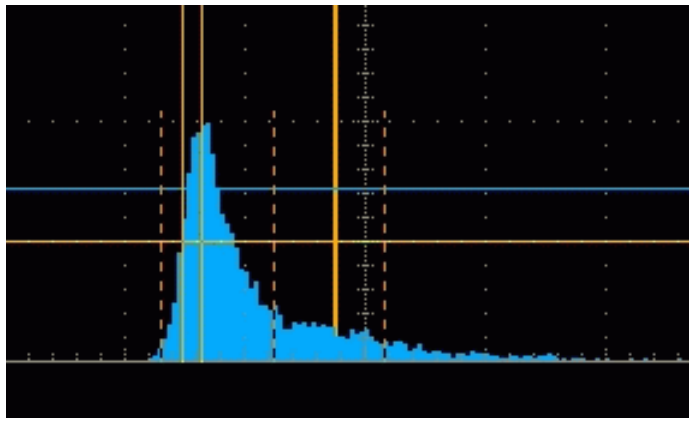
- from RPC far end

(both measured
at MB output =
signal propagated
through full chain)



# Measurement of Jitter (DB+MB) with RPC Signals

shortest geometrical possible
$\Delta t$=5 ns



shorter $\Delta t$ is
indicates
inherent electronics resolution

$\Delta t$

# Trigger on MB

- RPC multiplicity signal
- inverting op-amp's for summing
- design:
  - use the fact that high level of last pnp stage on DB (+3.2 V)
  - and also close to +3.3V supply on DB
- 3 stages:

| | | low (zero fired) | high (all fired) | |
|---|---|---|---|---|
| stage #1 | 4-ch | +2.4 V | +3.2 V | on DB |
| stage #2 | 16-ch | +3.2 V | +4.0 V= pECL | on MB |
| stage #3 | 31-ch | 0 V | -3.2 V = nTTL | on MB |

- LEMO out
- op-amp's on stage #2 are on GND, but on stage #3 on –5 V

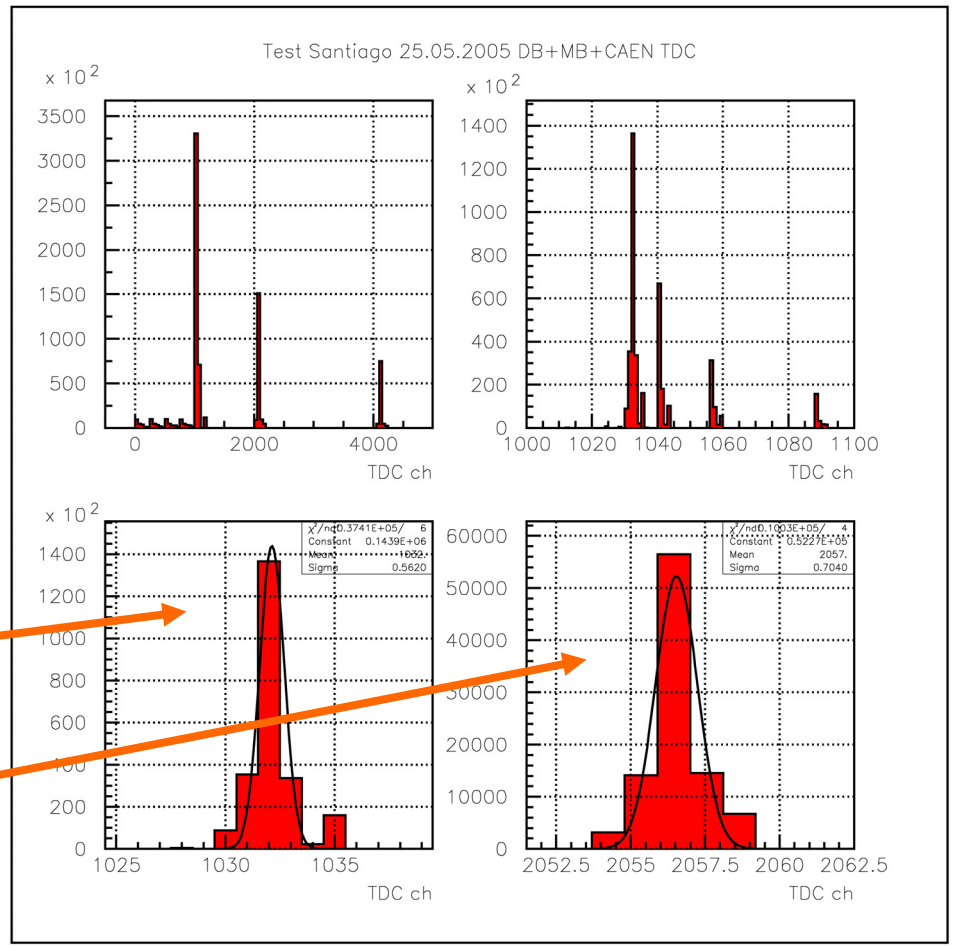
100 ns 10 ns

# Test with Pulser

- „full chain“ (DB+MB+TDC+VME), but pulser (not RPC)
- 10 ns pulses
  100 ns puls-to-puls
  → multi-hit TDC multi-fires for 8-9 subsequent pulses
- $\Delta t \sim 160$ ps FWHM
  incl. 100 ps TDC bin width

leading edge of 1st puls

leading edge of 2nd puls



# TDC can fire before trigger signal

- windows must be adjusted by writing registers through VME (opcodes = hex number sequences)
- delay cables obsolete

**1st case: the trigger matching window precedes the trigger arrival:**