An Interleaved Sampling ADC Module

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Outline

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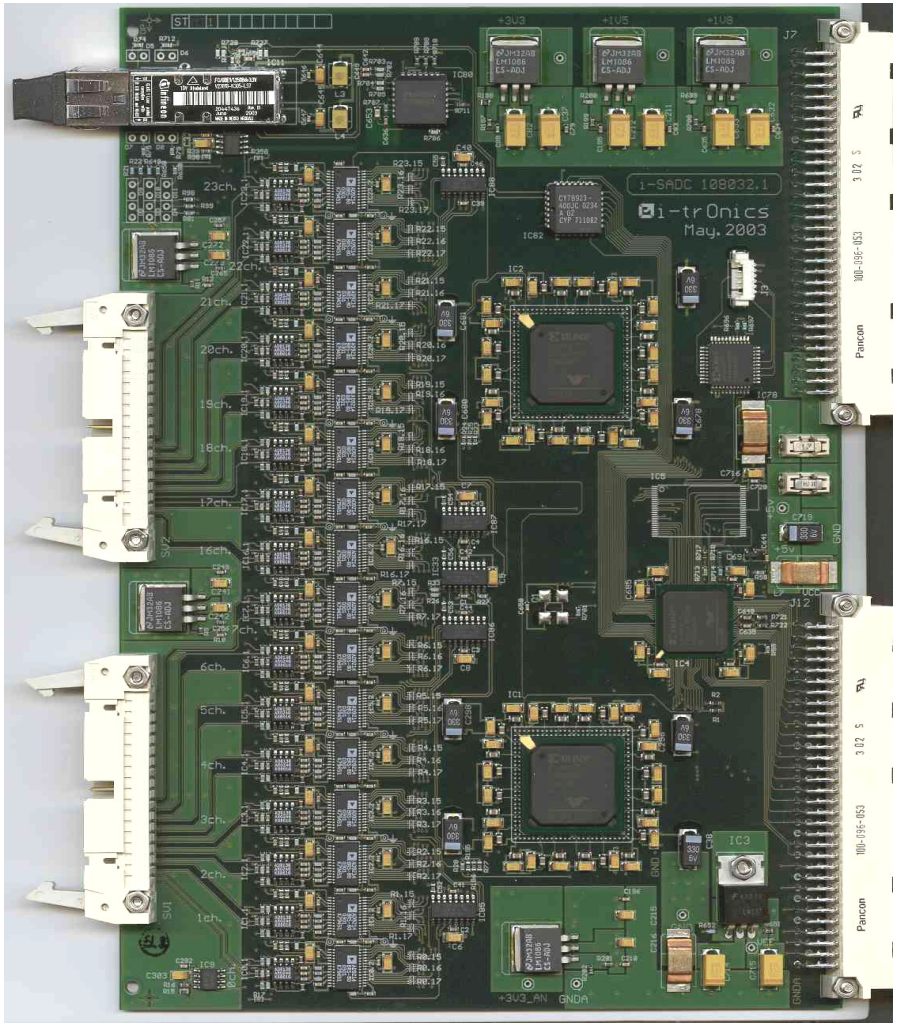
- Wish List for the new SADC
- Interleaved SADC System Overview
  - System Control
  - ADC Operation
  - Calibration for Interleaving
- First Prototype Module
- Outlook

The "old" SADC Module

- 6U VME module
- 32 channels, differential input with amplifiers
- 80 MHz sampling rate
- 10 bit ADC resolution
- 1.5 V dynamic range
- 1.5 mV/LSB sensitivity
- optical data interface
  - synchronous clock
  - HotLink data interface



Wish List

- different module shapes to match to detector frontends
- component reduction (FPGAs, ADCs)
- easier data access for debug/development and small lab-setups
- less power consumption
- environment monitoring (temperature, voltages, currents)
- local firmware memory
- unique ID for every module

➔change to serial multicannel ADCs

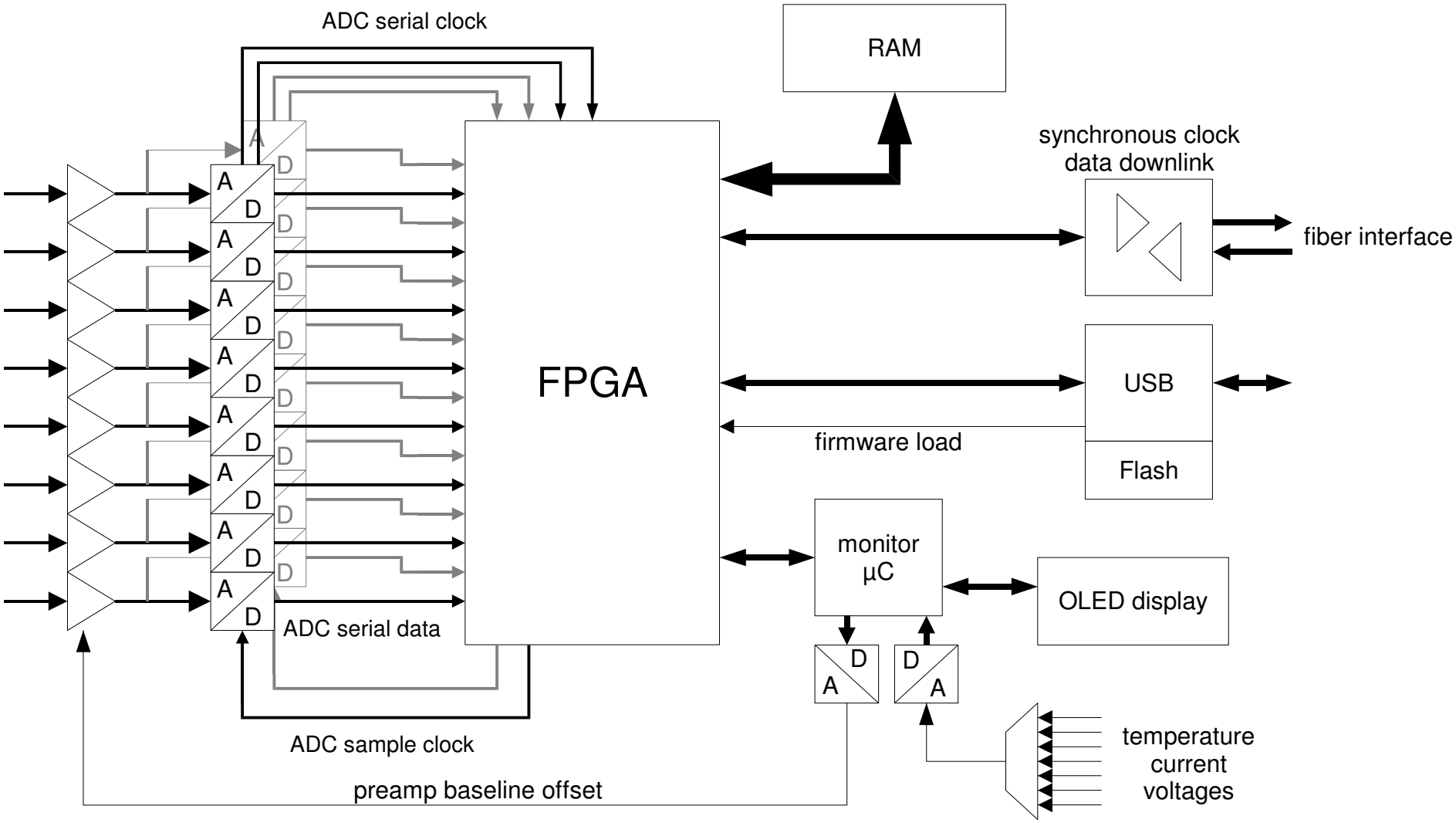
➔interleaved operation for higher sampling rate (option)

➔common PC interface (USB)

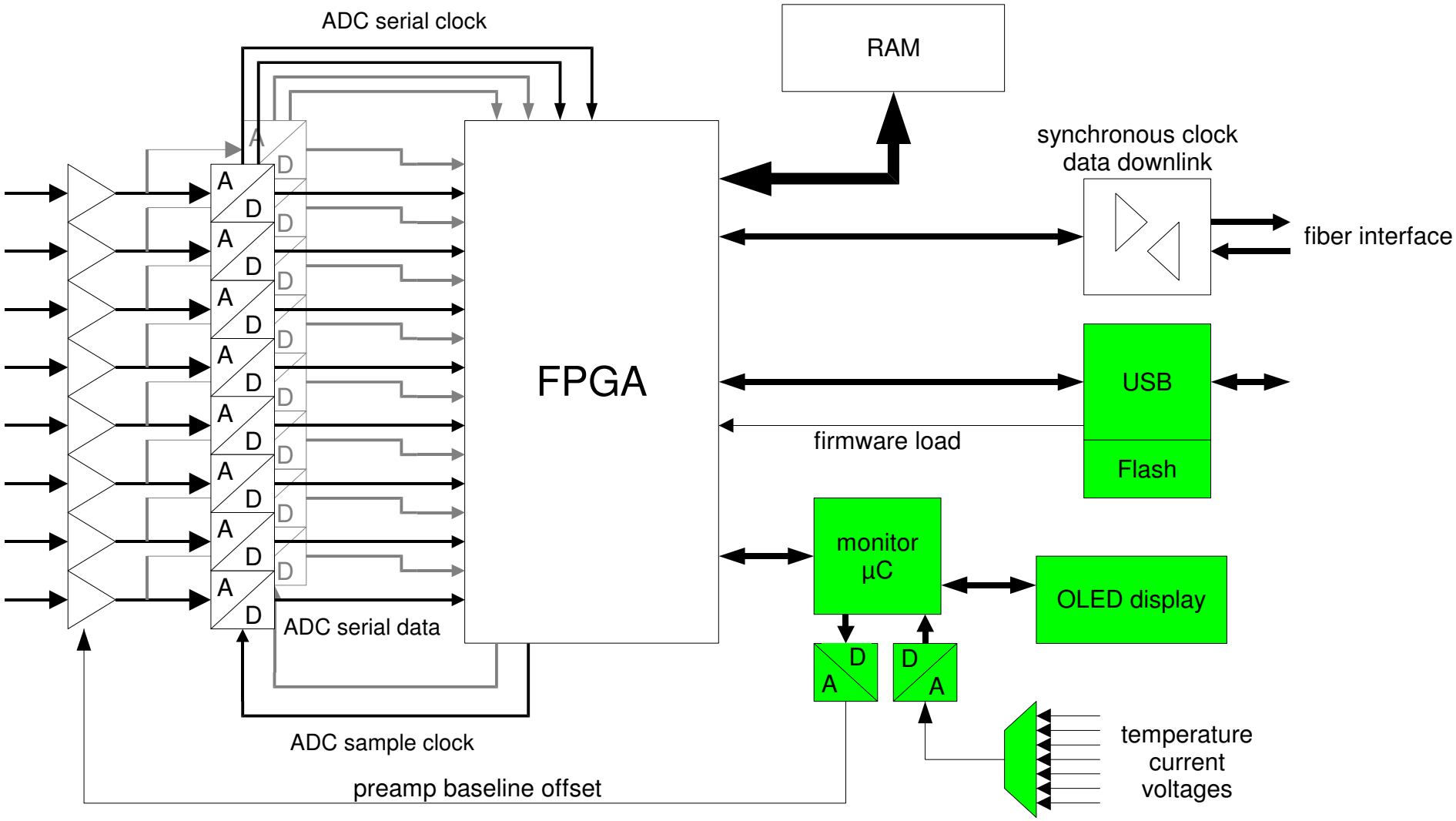
➔display for debug output

➔dedicated microcontroller for monitoring tasks

New System Overview



System Control



System Control (2)

- Cypress CY7C68013 USB 2.0 interface chip
  - 8051 based controller
  - KEIL C compiler demo version available (limited to 4K)
  - USB-Firmware loaded via USB or from external EEPROM

➔handles all USB data/control transfer via FIFOs

➔controls FPGA-Firmware flash memory

➔loads firmware(s) to FPGA

➔flash holds also module ID (write protected)

System Control (3)

- Atmel AVR ATmega128 as monitor controller
  - C optimized RISC processor core
  - free GNU C compiler available
  - free AVRStudio from Atmel for simulation/debugging
  - AVR-Firmware loaded via JTAG, SPI or self-programming

➔temperature, voltage and current monitoring via SPI ADC (10bit)

➔power control of frontend modules

➔setting of preamplifier offset via SPI DAC (16bit)

➔handling of OLED display and switches

➔bus interface to FPGA firmware registers

System Control (4)

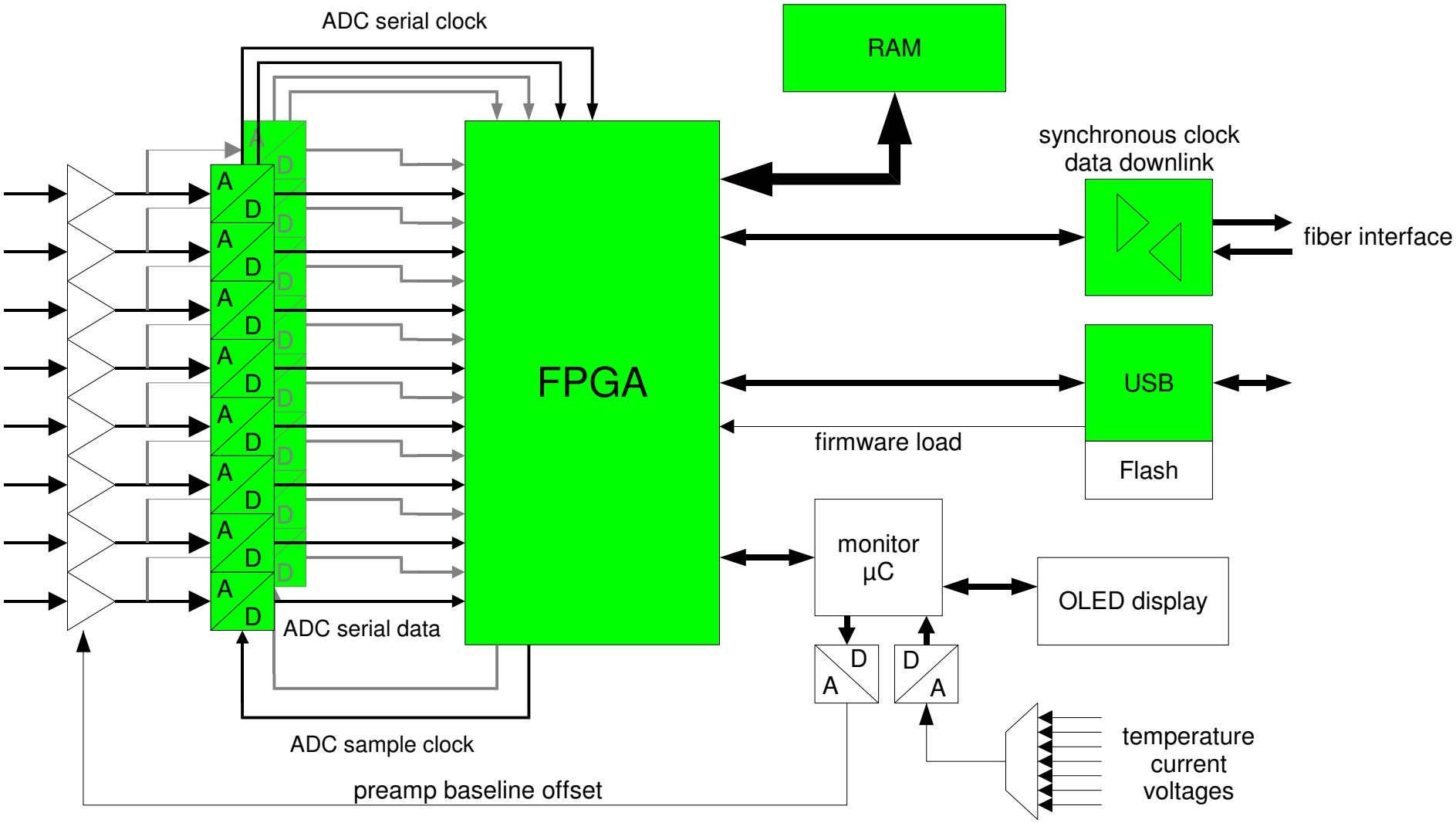
- OSRAM Pictiva OLED display
  - 128x64 full graphic display (no character set)
  - 16 grayscales per pixel
  - simple display memory write access
  - easy readable (self-emitting)

➔character generator implemented in AVR controller

➔8 lines x 21 ASCII characters (5x7)

➔display temperatures, voltages, buffer fill levels, ...

ADC Operation



ADC Operation (2)

- TI ADS5270 - pipelined 8 channel ADC
  - 10 and 12 bit versions available, up to 75 MHz sampling rate
  - 3.3 V analog and digital power supply
  - 907 mW power consumption (12 bit @ 40 MHz)
  - same clock for all 8 channels
  - serial data output for each channel via LVDS lines (240 MHz DDR)
  - slow SPI interface for ADC control

ADC Operation (3)

- Xilinx Virtex4 XC4VLX25 FPGA
  - 24192 logic cells, 1296 Kb block RAM, 448 user IO pins
  - SERDES included in IO cells

➔ADC data interleaving

➔noise suppression

➔trigger detection, feature extraction (time, amplitude)

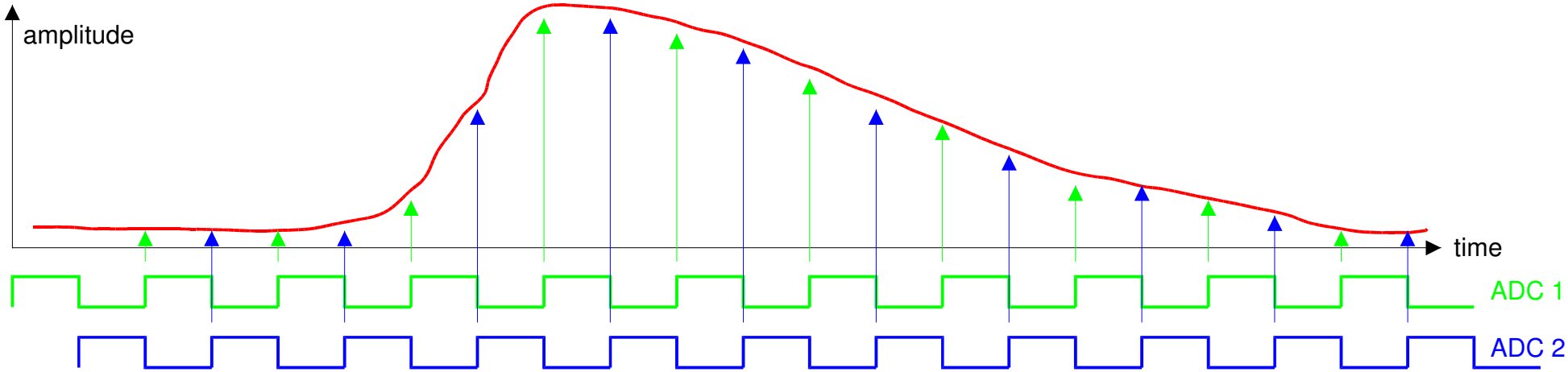
➔data buffering (external 32 MB DDR RAM)

➔handling of data/control messages (USB, fiber interface)

Interleaved ADC Operation

- price comparison
  - 12 bit @ 40 MHz : ~ 45 $
  - 12 bit @ 75 MHz : ~ 121 $
- Virtex4 allows precise phase adjustment of clocks via DCMs

➔get 12 bit @ 80 MHz from two interleaved 40 MHz ADCs



Interleaving Problems

- different clock path delays for the two ADCs
- offset and gain differences
- component variations between the 8 channels of one ADC

➔additional noise in interleaved data

➔clock delays can be compensated by DCMs in the Virtex4

➔offset correction is simple ADD/SUB operation on ADC data

➔gain correction by ADD/SUB of amplitude dependent value calculated from gain mismatch

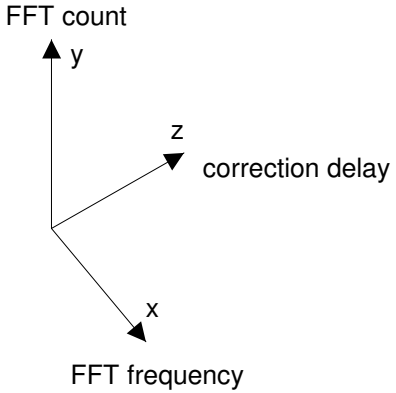
➔inter-ADC mismatches may be corrected by additional digital filters

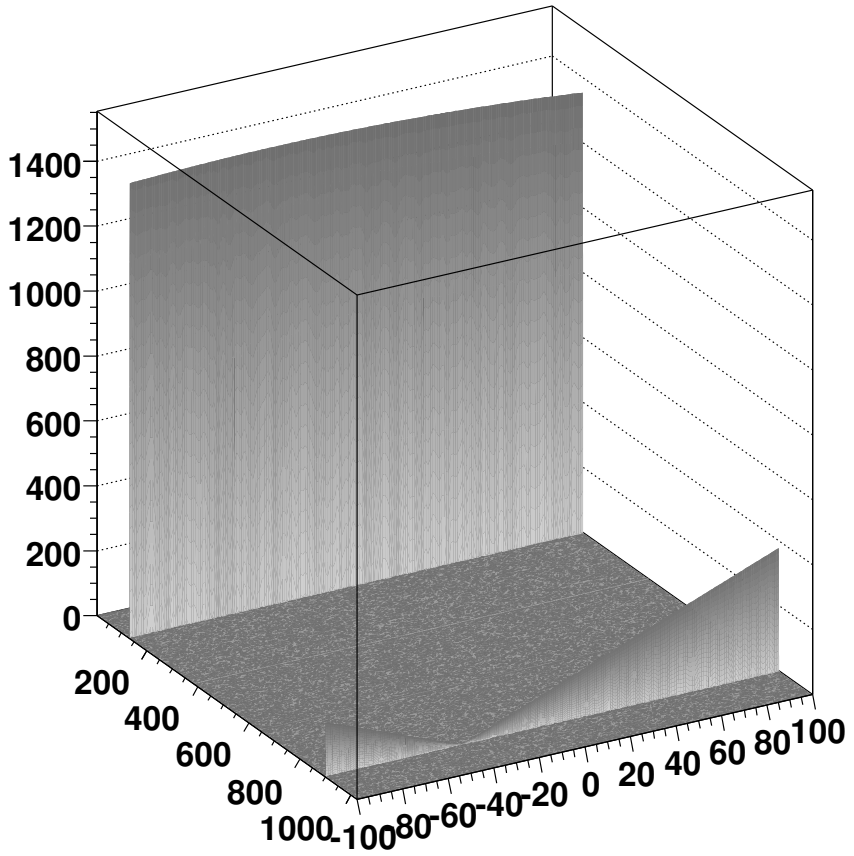
Clock Delay Correction

FFT calculation of interleaved ADC data:

simulation with
sine input signal
and added gaussian noise

sigma = 2





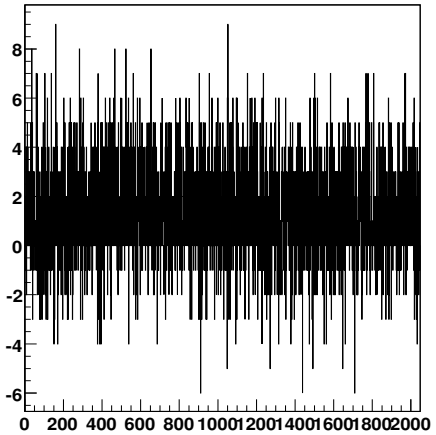
Calibration Procedure

- determine offset error
  - ➔FFT of data with ADC input = 0 V
  - ➔minimize peak at $f_s/2$
- determine gain error
  - ➔FFT of data with ADC input = max. value
  - ➔minimize peak at $f_s/2$
  - ➔calculate gain correction slope
- adjust clock phase
  - ➔FFT of data with ADC input = fixed frequency f_i
  - ➔minimize peak at $f_s/2 - f_i$

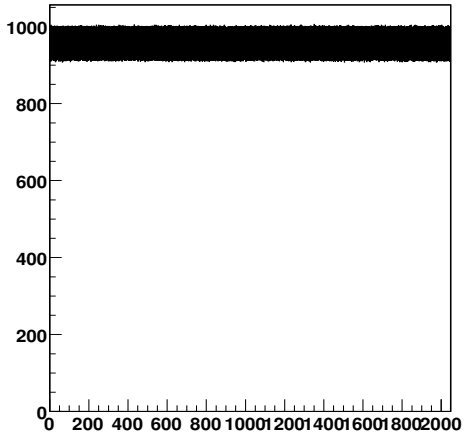
Calibration Procedure

simulation with
gaussian input noise

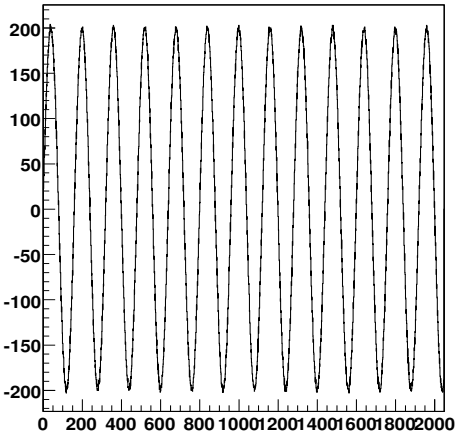
sigma = 2



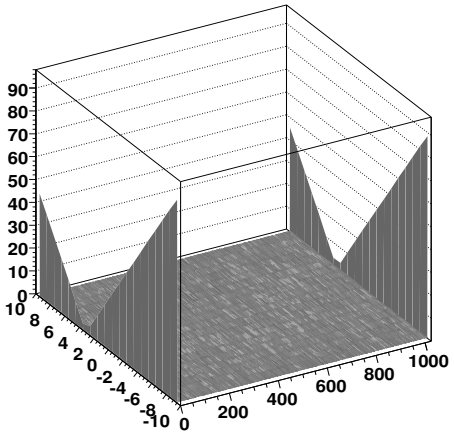
offset = 3

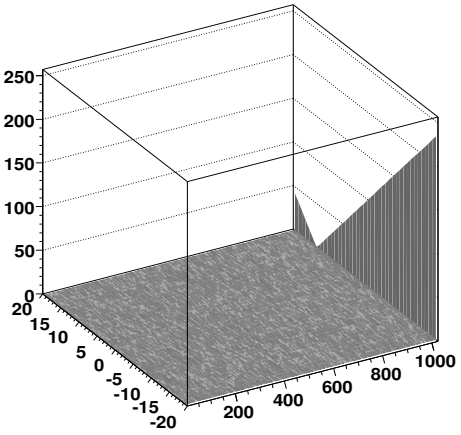


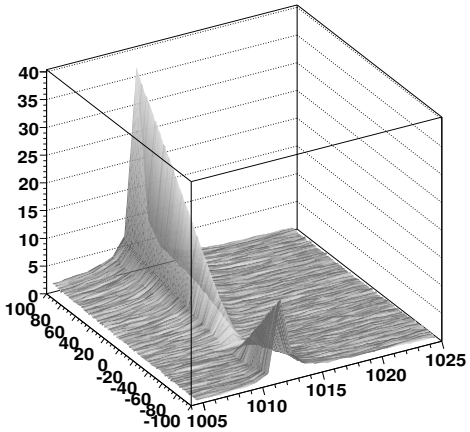
gain mismatch = 0.01

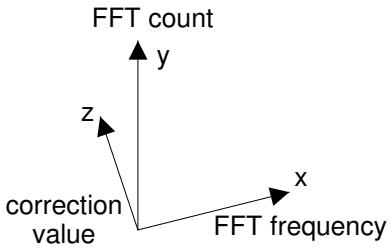


delay mismatch = 0.4

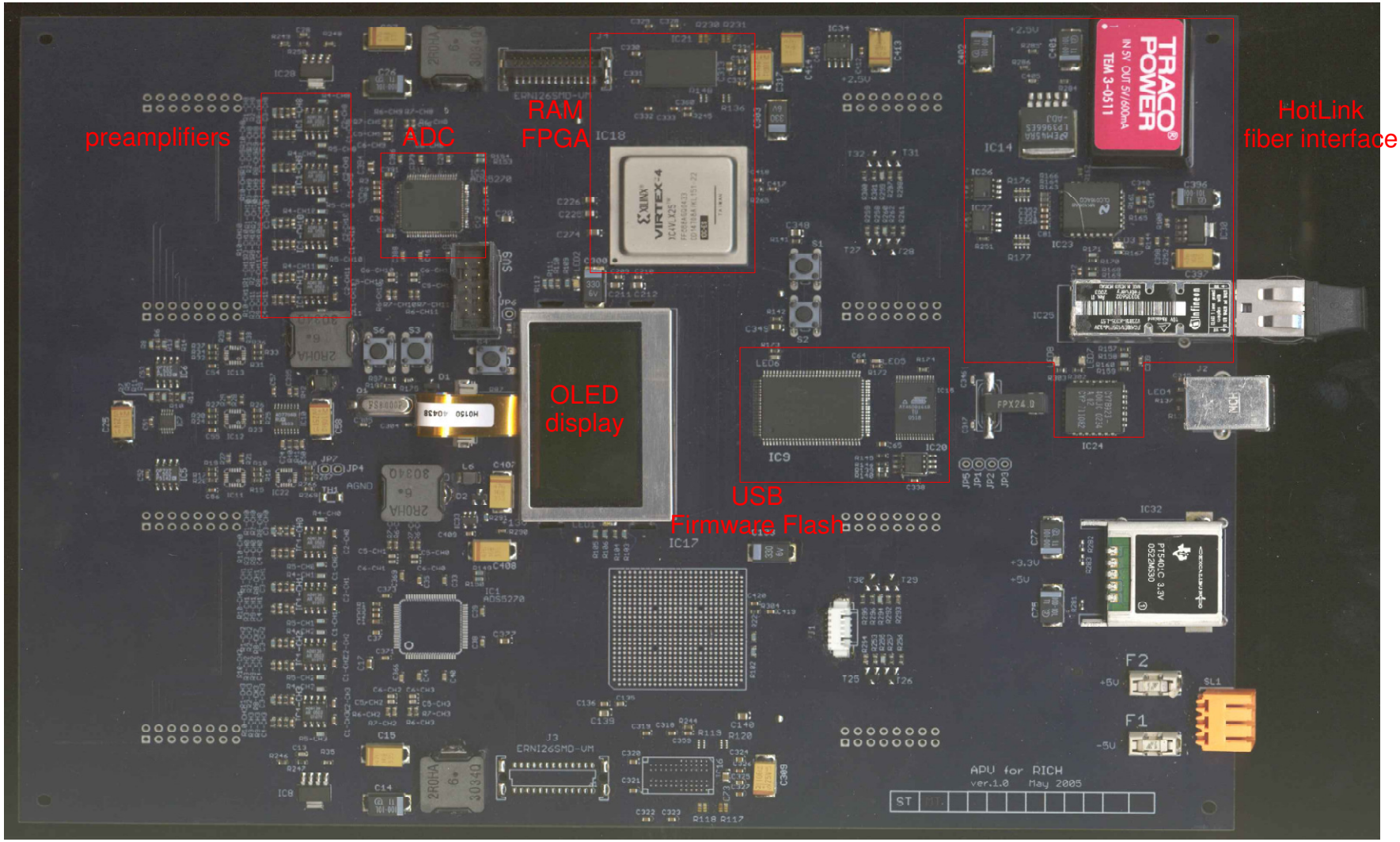








First Prototype Module



Outlook

- test interleaved ADC operation
- automated system test and calibration procedures
- change outdated HotLink interface (gigabit SerDes)

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