Si-Strip FEE development for CBM

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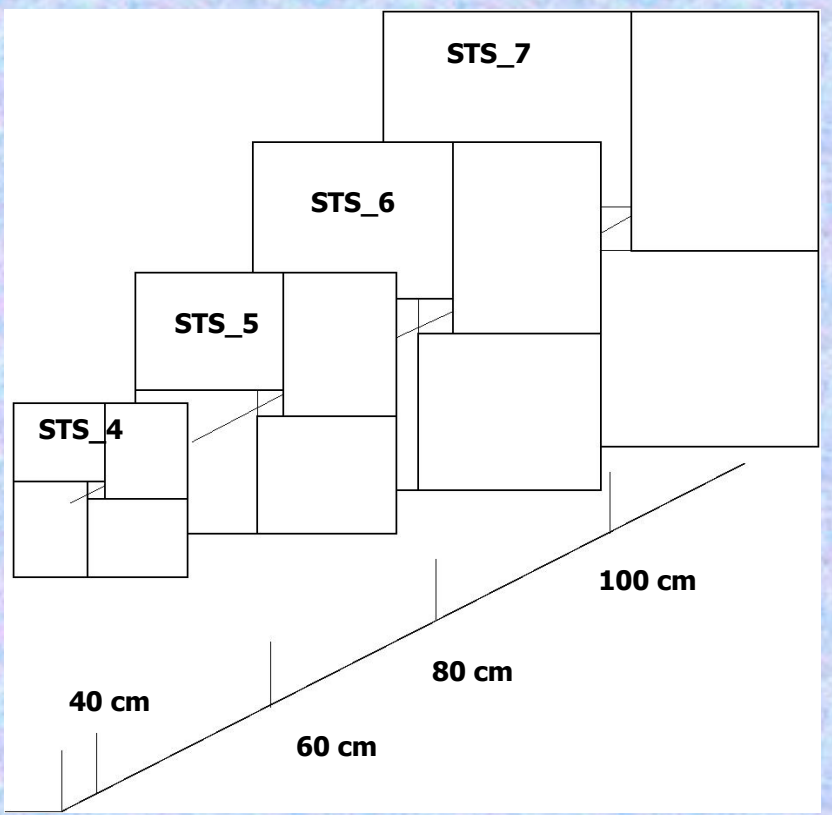
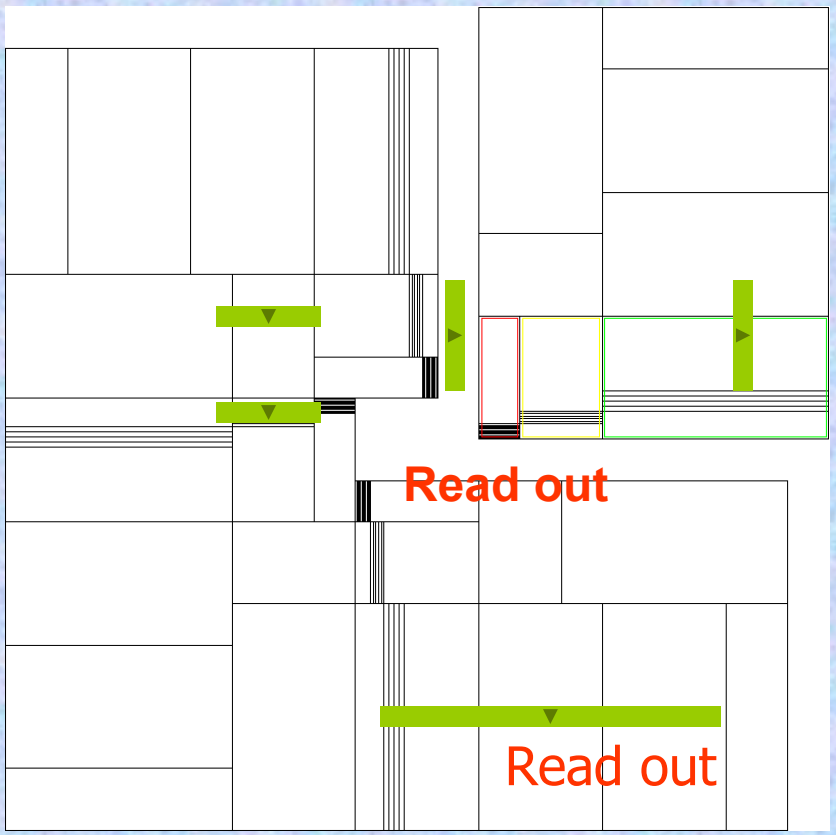
Introduction and Status

- Silicon Strip part of the CBM Tracker applies thin Silicon strip detectors and Multichannel FEE ASICs





Introduction and Status

- Silicon Detector R&D on double sided and thin CBM detectors has been started

- FEE R&D has been started

- First prototype of the FEE building blocks for analog part of FEE is manufactured

- UMC L180 CMOS mixed-mode technology 1P/6M (1.8V/3.3V) +RF option used as a first CBM run

- Lab tests will be started this month

Requirements for Si-strip FEE

Silicon detector

- Detector thickness is 100 um (150-200???)
- Detector pitch is 25 um (50???)
- Double sided
- Strip length is 2, 4, 6 cm (???)
- Strip Detector capacitance is up to 70 pF according to the strip length
- Bias voltage up to 15 V
- AC coupled detector

Requirements for Si-strip FEE

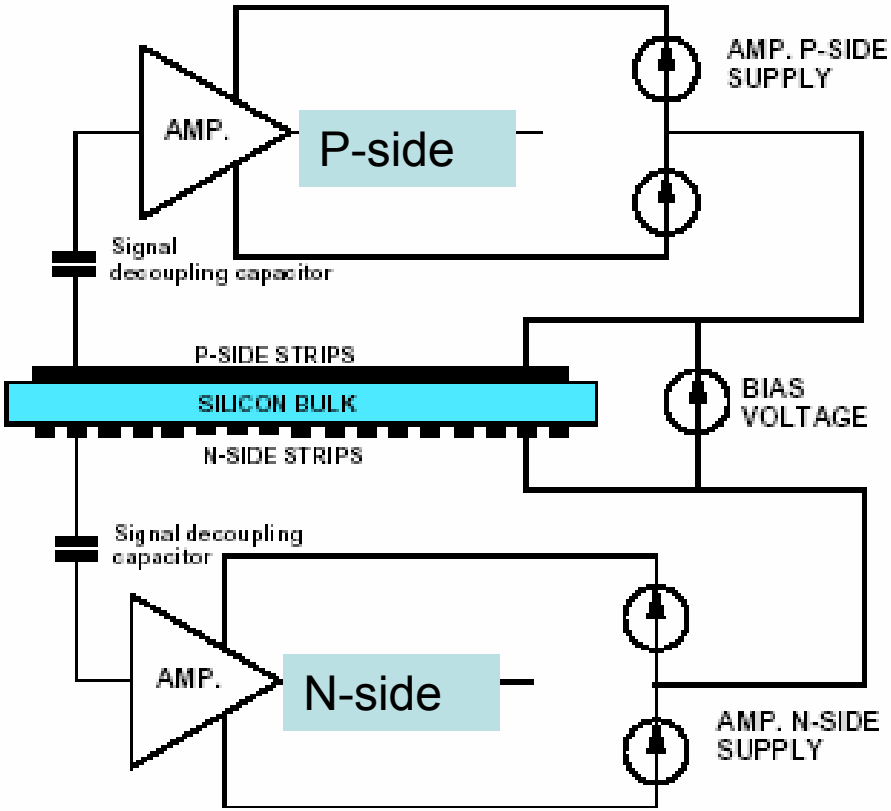
Input FEE parameters

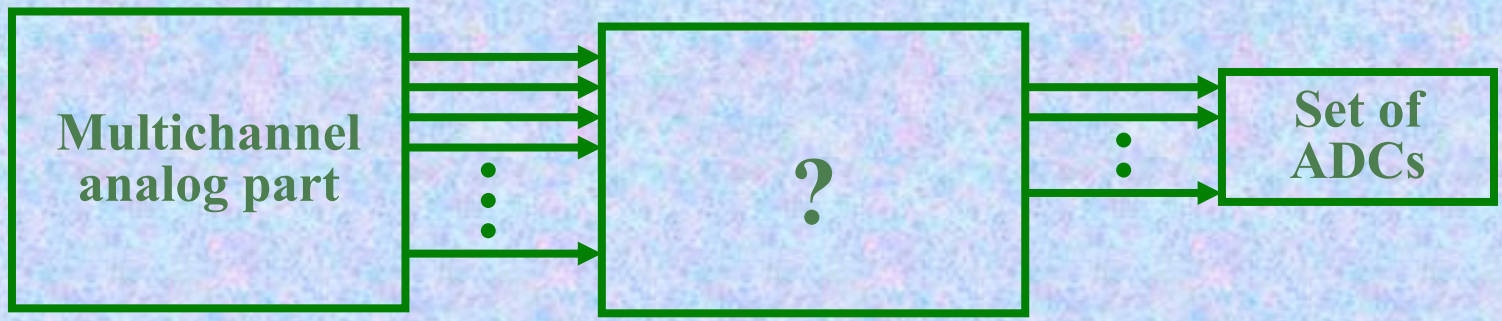
- MIP is 7000 electrons
- Input capacitance depends on how many strips will be combined to one equal strip. Input capacitance value is up to 70 pF.
- Signal/noise ratio more than 10 (15 is preferable)
- Maximal event frequency is 10 MHz
- Dynamic range is 10 MIPs.
- Both polarities input pulse

Requirements for Si-strip FEE

- Amplitude and time signal processing
- Event time recognition accuracy is 2-4 ns
- Dead-time free
- Self-triggered
- High radiation hardness up to 15 Mrad
- Preferable chip technology is CMOS according to general FEE conception. Nowadays that is a 0.18 um CMOS mixed mode one.
- Working temperature is 0…50 grad
- Power consumption not more than 2 -3 mW per channel (depends on the cooling system)
- Supply voltage(s) is 1-3.3 V of both polarities (in fact defined by breakdown voltages of 0.18 um CMOS process)

FEE Structure (very simplified)





Derandomizer

Analog ***derandomizer*** is a unit performing neuron-like processing, but in analog field.

It is a deadtime free analog unit with ***n***-inputs and ***m***-outputs, ***n>m***.

Thus it allows to reduce the number of following ADCs.

The derandomization procedure implies the skipping of empty channels and thus is indivisibly bound with data sparsification.

Efficient processing of the randomly appearing signals by blocks, having a dead time, needs the choice of a proper architecture.

Relevant starting references:

1. Design of a derandomizer with a buffer controller. University of Stockholm http://www.sysf.physto.se/kurser/digsyst/project1.html, 1999.
2. P. O'Connor, G. De Geronimo, A. Kandasamy. Amplitude and Time Measurement ASIC With Analog Derandomization: First Results. IEEE Trans. on NS, v. 50, N 4, 2003, p.892-897.

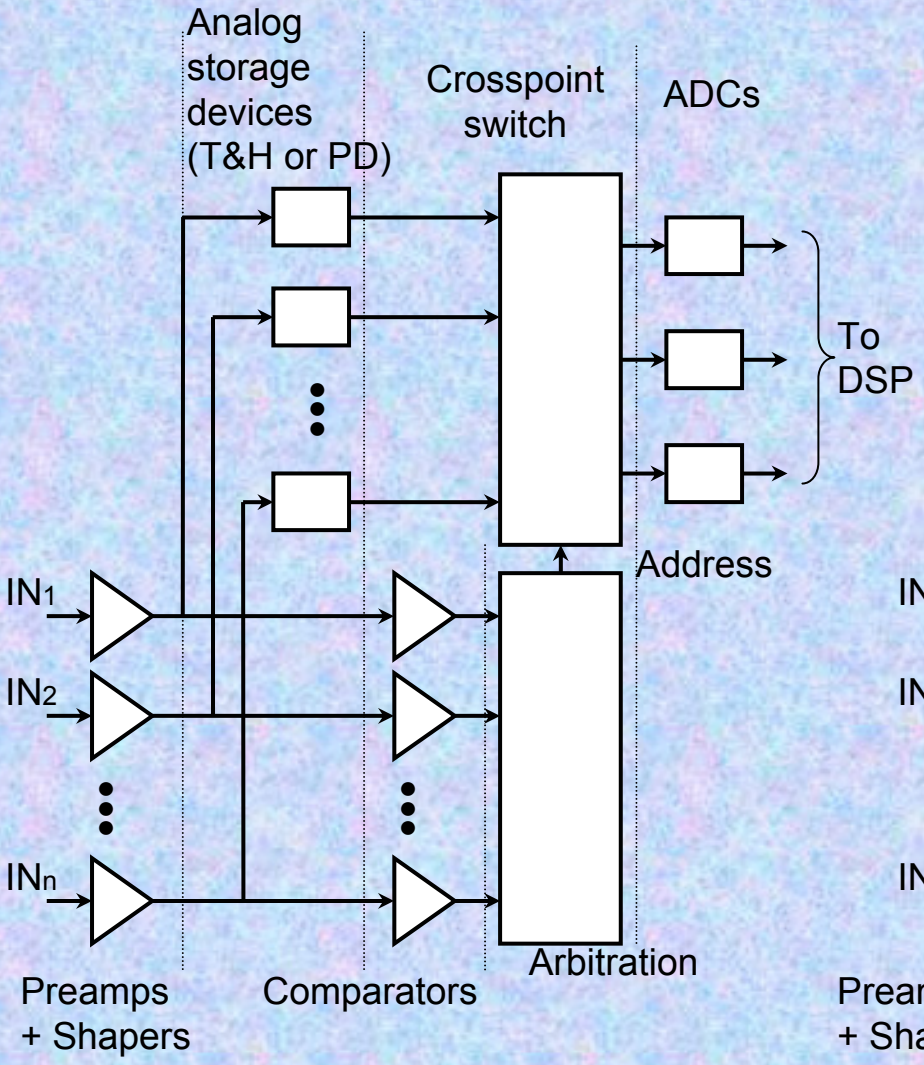
Derandomizer

Usually a derandomizer incorporates or is followed by such functional blocks as:

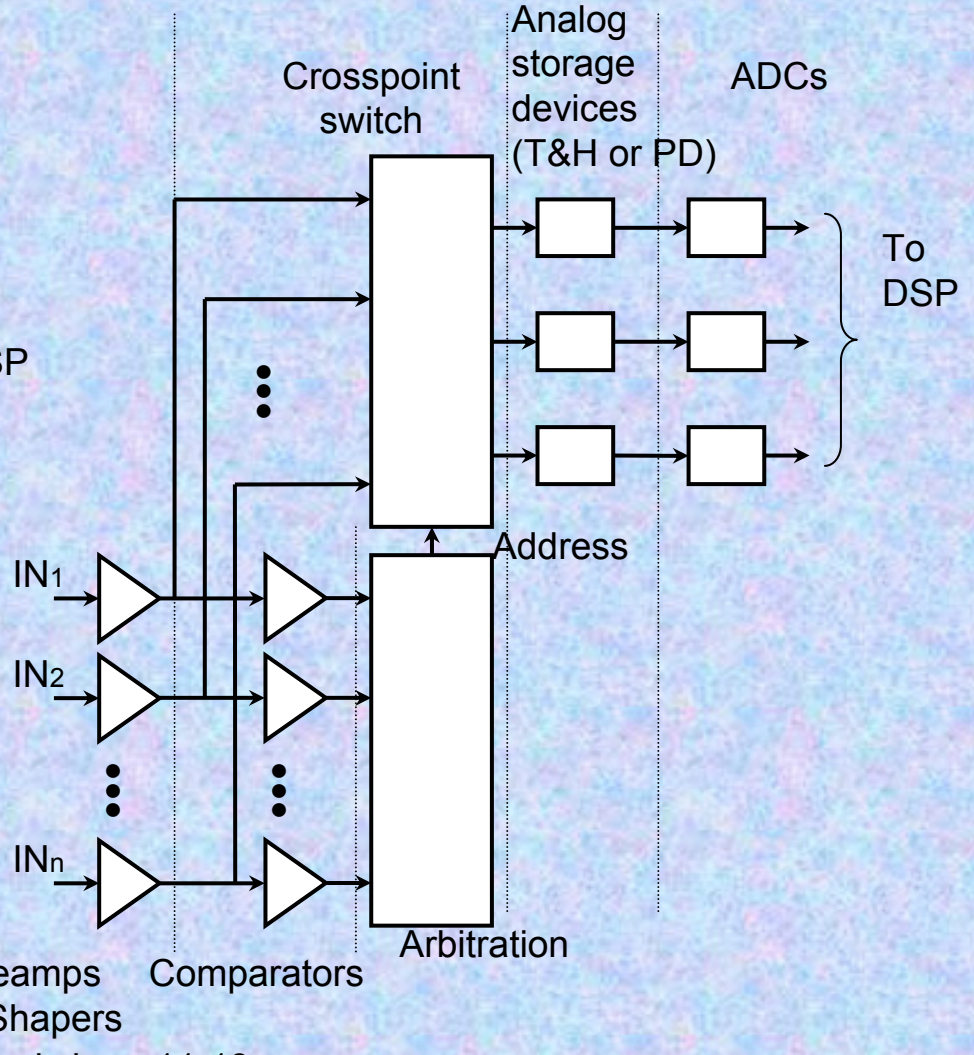
- peak detectors (T&Hs) for amplitude measurement
- TACs for time measurement
- hit finder (fast low threshold LE discriminator)
- arbitration logic
- crosspoint switch
- analog multiplexer

Derandomizer options

One storage per channel



Multiple storages shared by channels (from BNL)



Prototype goals

Development of building blocks for data-driven architecture, according to UMC CMOS 0.18 µm. These blocks are:

- **Preamp**
  - Amplitude (slow) antialiasing and dynamic range saving shaper
  - Timing (fast), hit defining shaper
- **Low offset high-speed comparator** both for hit finder and ADC.
  - **Studying** both **clocked** and non-clocked options
- Threshold DAC (6-8 bit)
- Fast low-bit (4…6 or 8 bit ?) ADC
- Analog Derandomizer (deadtime free analog unit with n-inputs and m-outputs, n>m)
- **Rail-to-rail op amp (high speed buffer)**
- **Common issues are: low power consumption, reasonable speed & chip area**

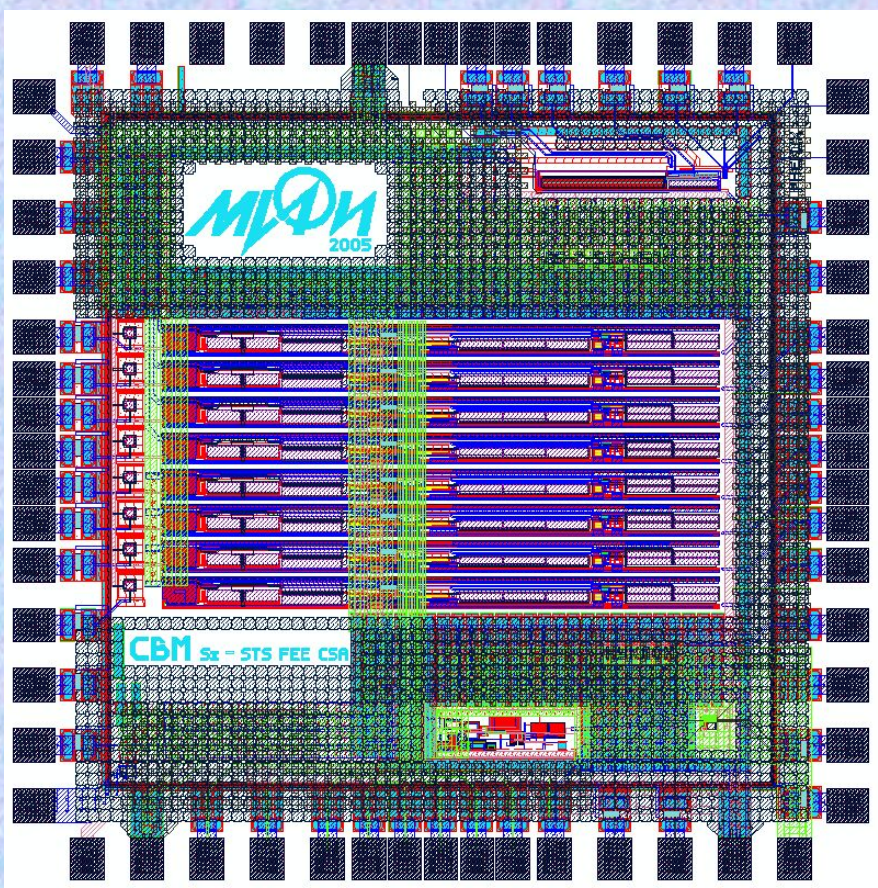
First prototype

Main steps: Schematic, layout, verification, GDSII files, test station and board design, testing

60 pads, 1.5*1.5 sq.mm, min pitch 59 um

2 full-time engineers + 4 diploma students, half a year for design

Structure blocks: 8 CSAs, test purpose CSA core, rail-to-rail opamp, clocked comparator



Realized in a 0.18 um, single poly, six metal, salicide CMOS process from UMC, Taiwan.

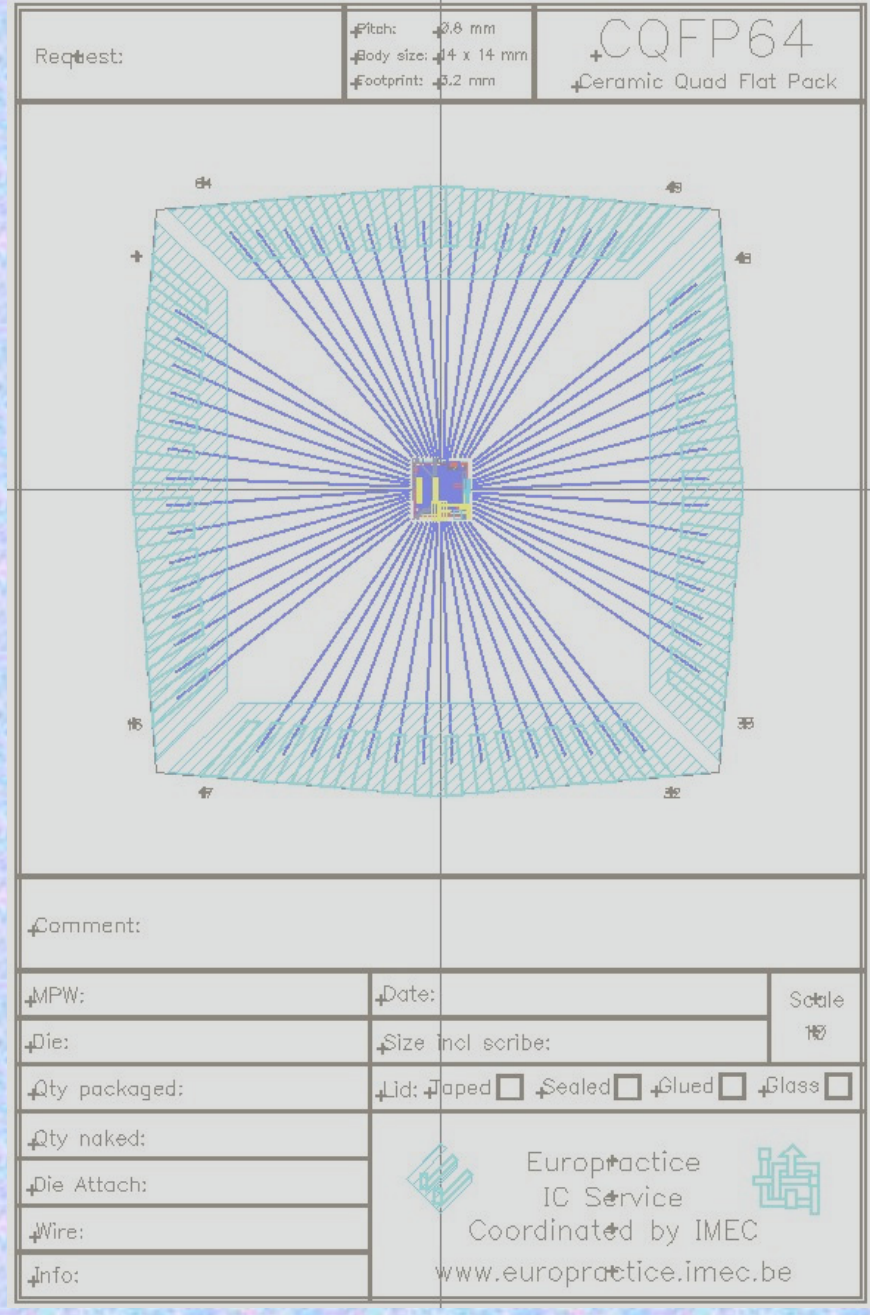
That was a mini-ASIC run, scheduled via Europractice

CSA schematic

- CSA is based on folded cascode architecture
- DC and AC input coupling are available
- Two mirrored versions of CSA has been studied. These are:
  1) version with PMOS input transistor and
  2) one with NMOS transistor.
  In accordance to the foundary Design Kit models at reasonable shaping the PMOS version showed a greater noise performance and was selected for the input device of CSA
- Input PMOS: 0.5 mA (half power budget), 1.2mm*0.18um
- Feedback cap 2pF sets the gain to 0.5 mV/fC. Feedback is optimized for up to 100pF capacitive detectors (pads, strips and so on)
- Noise at CSA output (wide bandwidth) at 100 pF of Cdet: 200 uV rms for CSA core only, 350 uV rms for CSA with active feedback
- Maximal signal at 5% non-linearity – 0.5 V (at ±1V supply and Cdet up to 100 pF)
- Supply voltages: 1) 0 and +1.8V or 2) -1.0 and +1.0 V
- 1.0 mW/channel

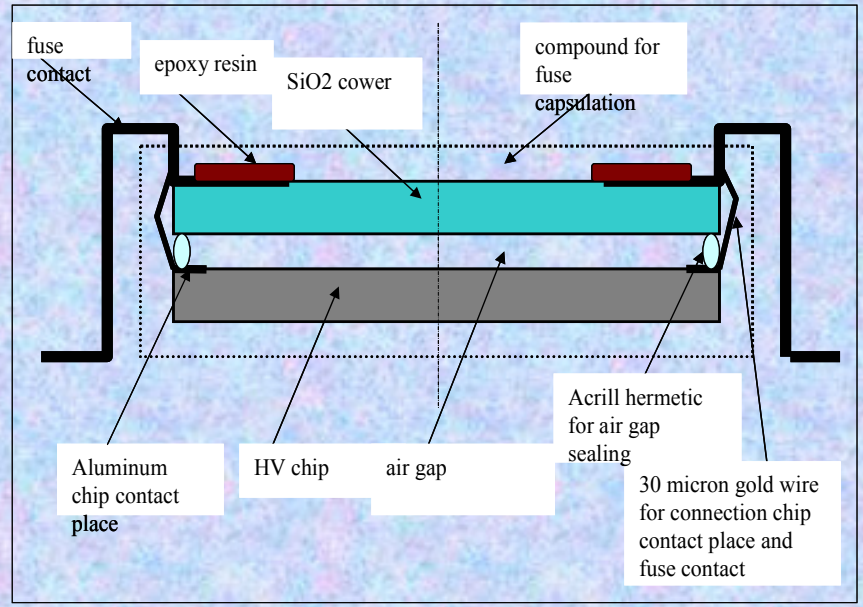
Remarks

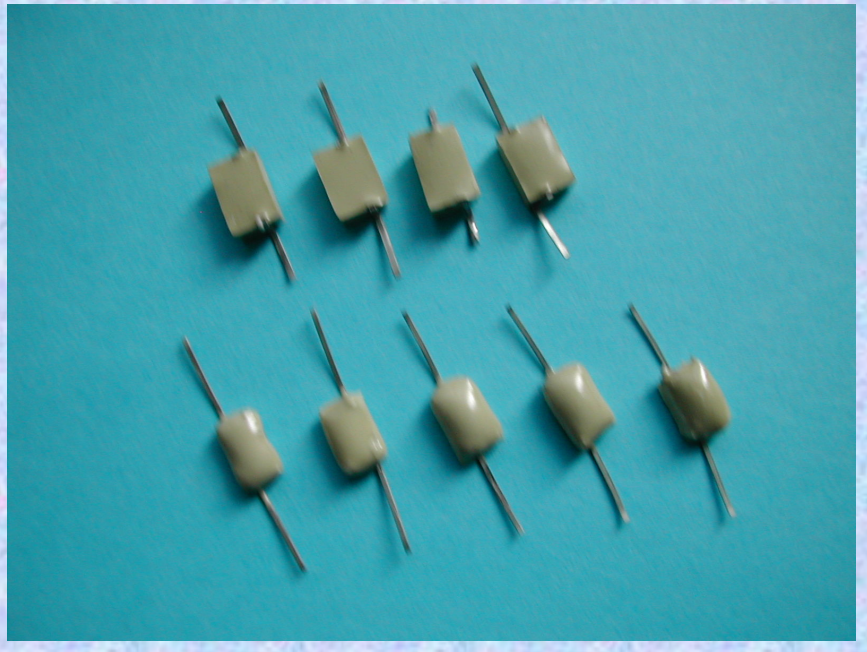
- This prototype ASIC blocks focus on study of possibilities and merits of UMC 0.18um process.
- All 8 CSAs are different each other. It is needed to optimize the structure and biasing of CSA
- Optional 3.3V CSA block



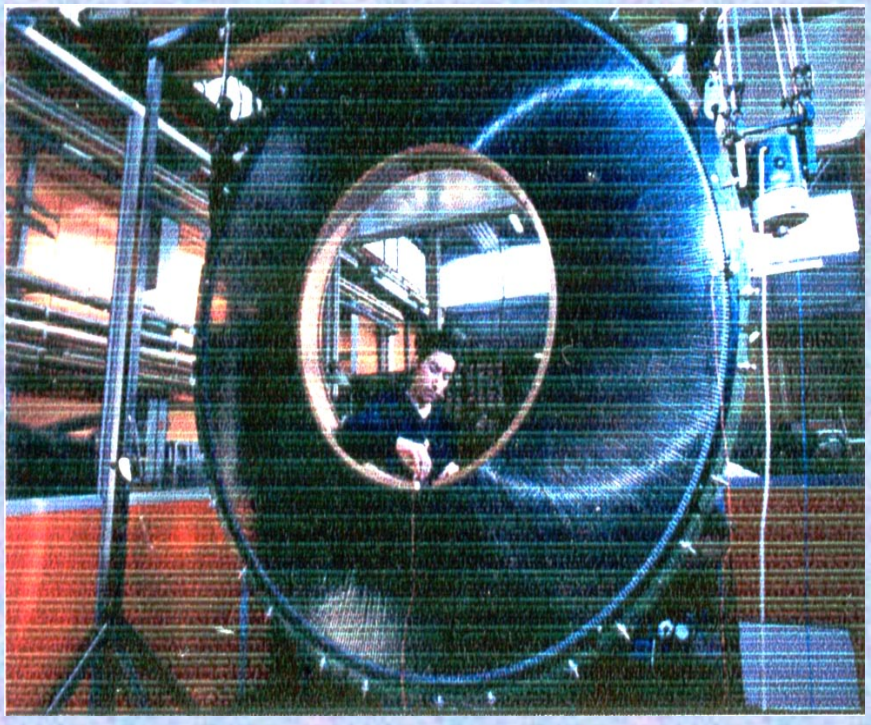
Other developments

Desing of HV Fuses





Microelectronic high-voltage fuses for TRT systems of ATLAS experiment (CERN)



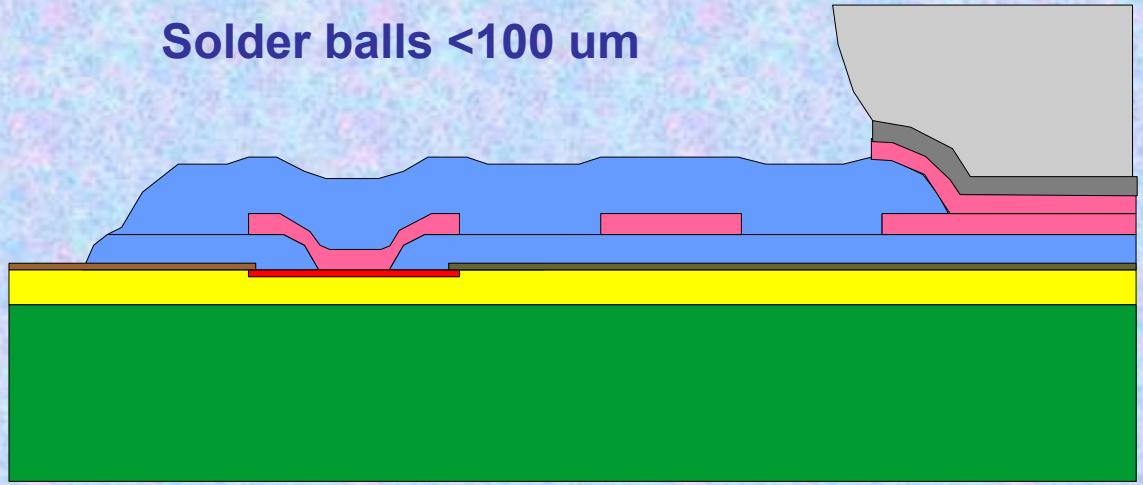
The main characteristics:

- **resistance – 91 кОм±10%;**
- **size – 5,8 мм x 3,8 мм x2 мм;**
- **burning time 15 – 40 мs.**
- **Leakage current (at 2 kV) less than 1 nA**
- **Today more than 50 000 fuses were manufactured and supplied**

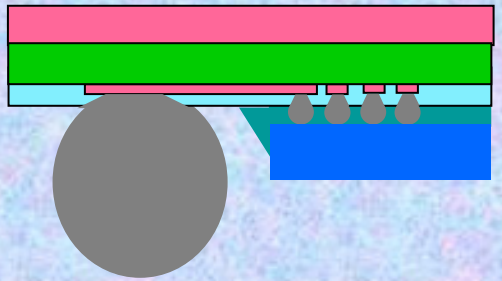
High Density Thin Film Interconnects

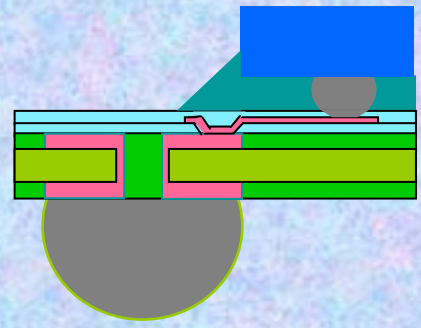
By Eric Beyne (IMEC),

Solder balls <100 um



60 um flip chip bump pitch

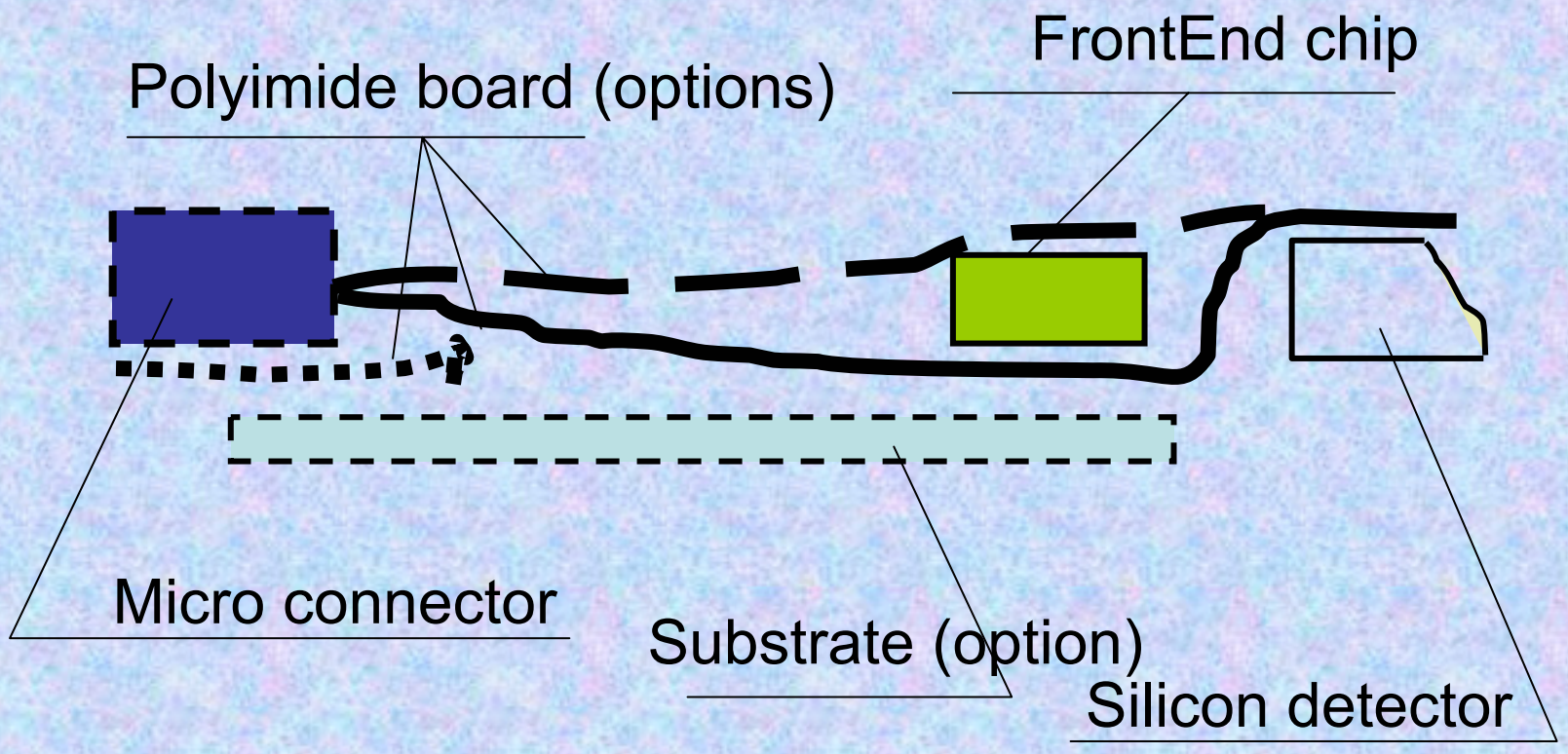




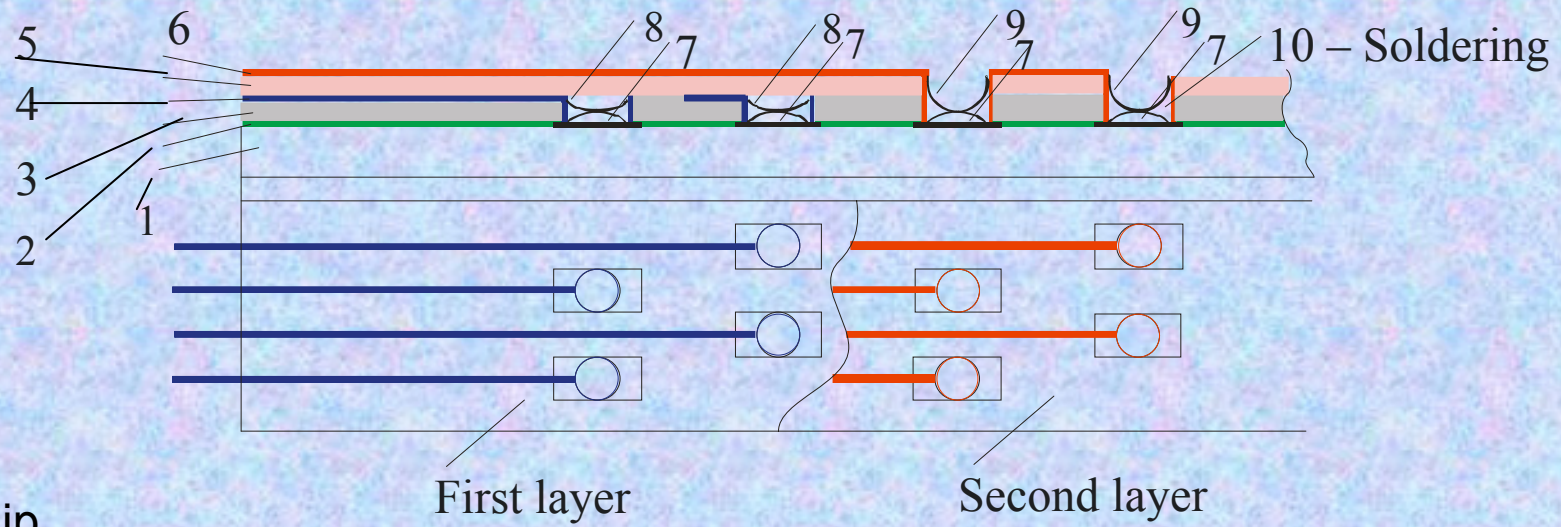
Si wafer
Cu/low K interconnect
Cu bond pad
Chip passivation
BCB Dielectric
Electroplated Cu
Electroplated Ni (UBM)
Electroplated solder bump

BCB -benzo-cyclobutene

Multilayer thin film technology RrontEnd module R&D



Multilayer thin film technology RrontEnd module R&D



1. Chip
2. Additional protection
3. First Insulate layer
4. First conductor layer
5. Second Insulate layer
6. Second conductor layer

7. Soldering pads
8. Internal Metallized hole
9. Second layer soldering hole
10. Soldered contact