The VLSI/ASIC based readout technology for the spectroscopic signal processing of the UHV compatible Si multi detector system (CHICSi).

Pavel Golubev and the CHIC* collaboration

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- Lund University, Department of Physics, Sweden
- Uppsala University, TSL, Sweden
- University of Jyväskylä, Finland
- SINTEF Electronics and Cybernetics, Oslo, Norway

* CELSIUS Heavy Ion Collaboration

Outlook

- *The CHICSi detector*
- *Front-End Readout Electronics CHICSi ASIC chip (Mk.2)*
- *ASIC card in UHV*
- *Practical experience*
- *PICA Project (Pulse Instrumentation Chip for analytical Applications)*
- *Summary and outlook*

Publications

"CHICSi – a compact ultra-high vacuum compatible detector system for nuclear reaction experiments at storage rings".

I. General structure, mechanics and UHV compatibility.
NIM A 500 (2003) 84

II. Detectors.
NIM A 500 (2003) 96

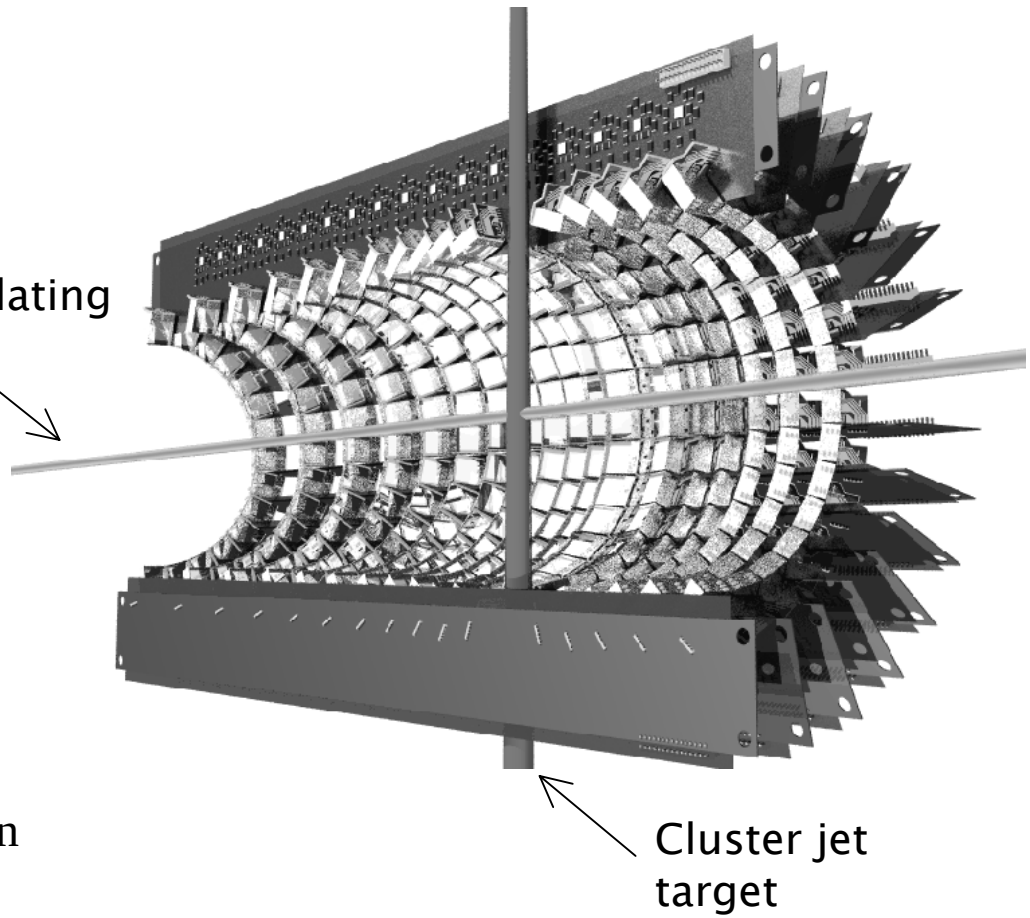
III. Readout system.
NIM A 516 (2004) 327

The CHICSi detector

- **CHICSi -program**
- Modular
- UHV compatible
- 3π covering
- Cluster-jet target

- **Missions**
- IMF
- Event characterizing device
- Event-by-event
- Energy range 0.7 – 60A MeV

One half of central CHICSi detector



- **Major challenges:**
  - –> Reduce costs
  - –> Compact for in-UHV operation
  - –> High granularity
  - –> Integrate readout of different types of detector

Detector telescope

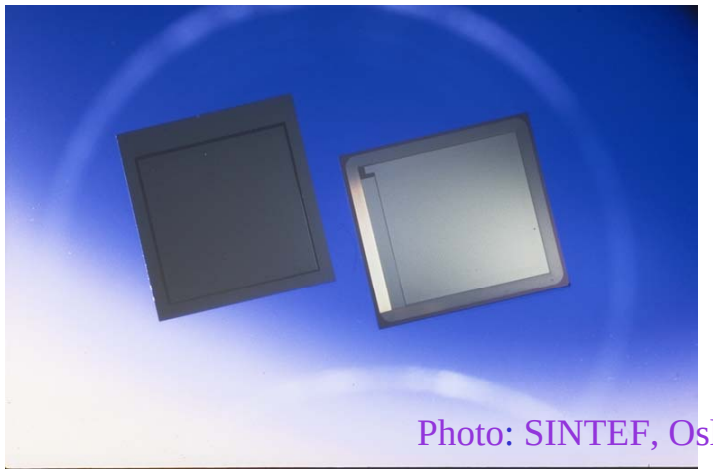
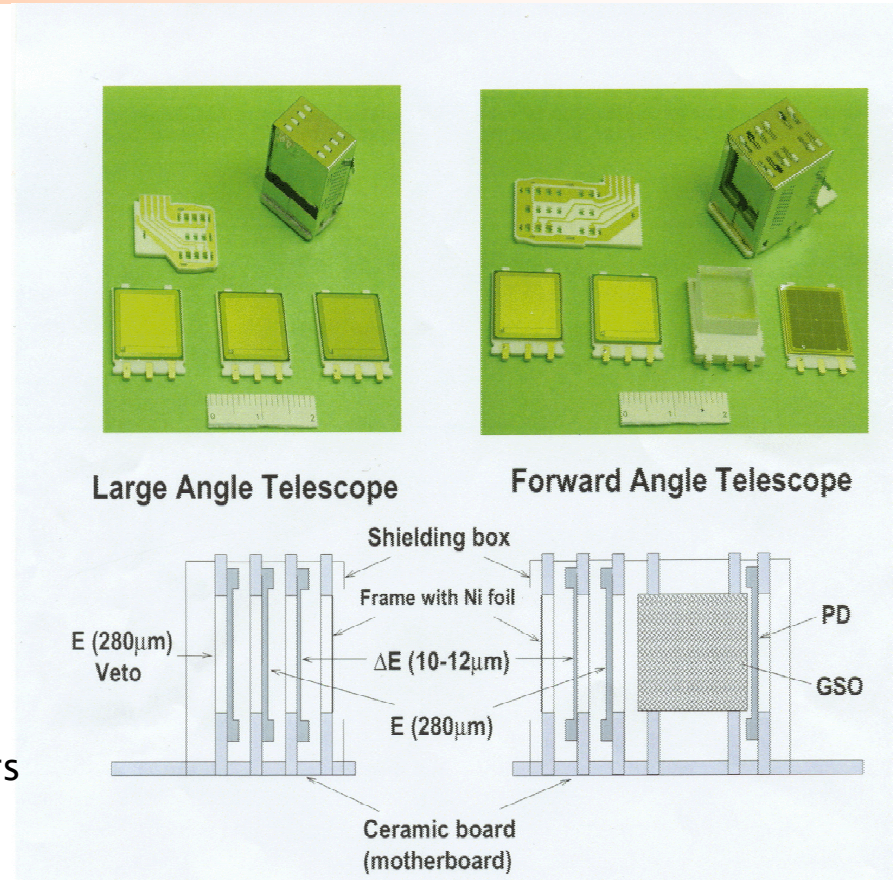
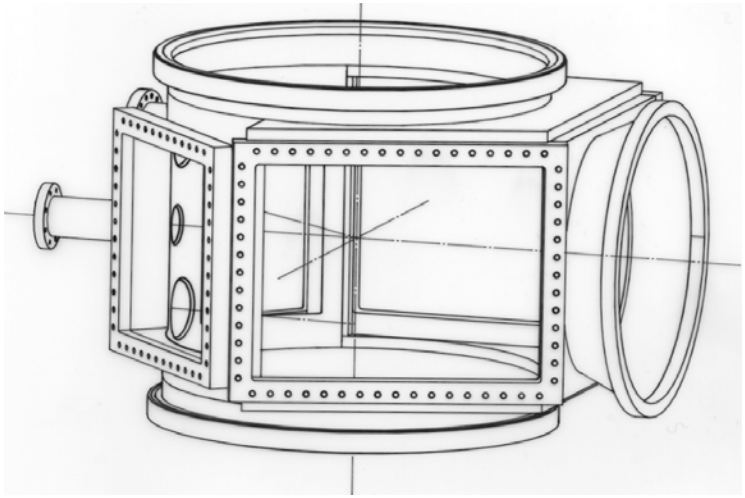


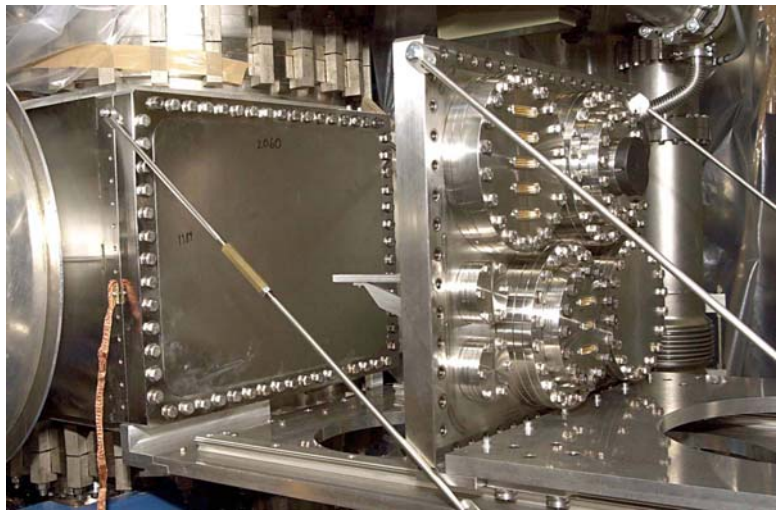
Photo: SINTEF, Oslo



- Construction of CHICSi readout chip with SINTEF Oslo/Austria Mikro System/IMEC
- Industrial production of 10-12 μm Si DE detectors developed with SINTEF Oslo
- Development of detector mounting with Monolitsystem AB Gothenburg
- Multilayer UHV compatible circuit boards and wire bonding FyTech Malmö

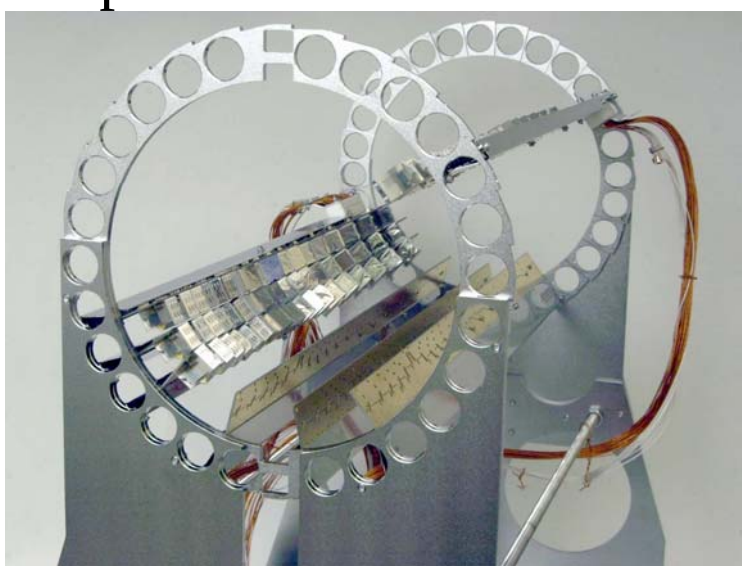
Scattering chamber

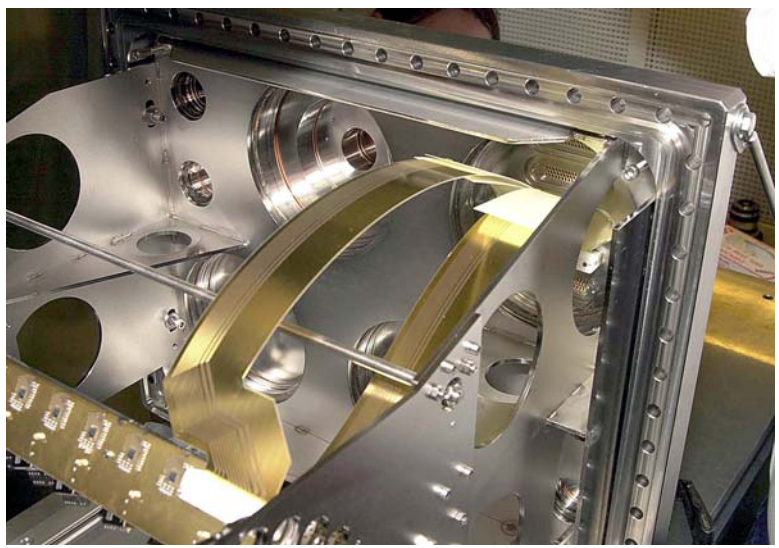




Kapton-insulated cables

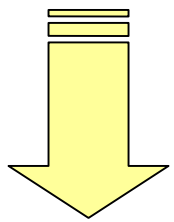
Printed-circuit board cable





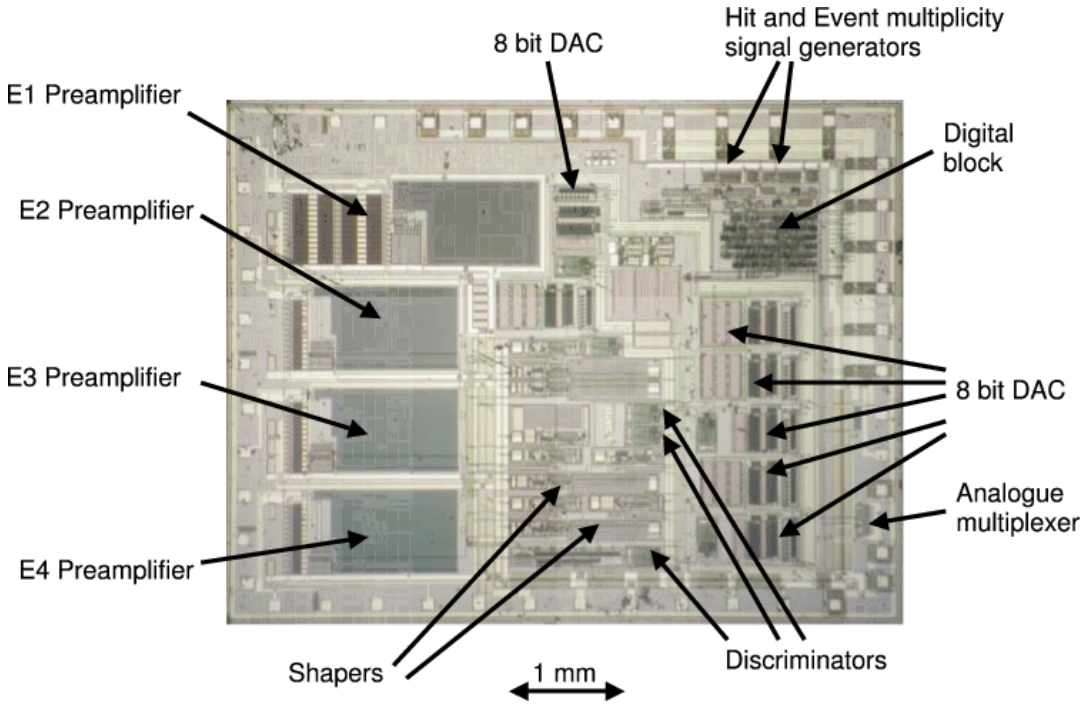
Front-End Readout Electronics

- Read out a large number (~2000) detectors
- UHV environment (~10^{-8} Pa)
- Free-running spectroscopy channels
- On-line trigger decision (particle- of IMF's multiplicity)
- Best and most economical readout scheme
- High-quality spectroscopy, wide dynamic range
- Singles event rate ~10^4/sec, valid ev. rate ~ few 100/sec
- ...



Readout scheme based on Application Specific Integrated Circuit (ASIC) with Very Large Scale Integration (VLSI)

CHICSi ASIC chip (Mk.2)



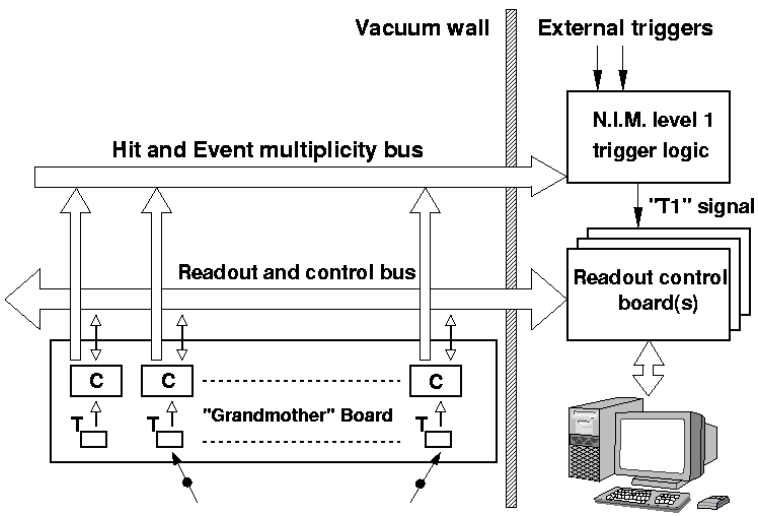
- **0.8μm high resistive poly2 BiCMOS technology**
- **Area 5.67×4.370 = 24.78 mm²**
- **Power consumption ~ 45 mW**
- **Analogue/Digital ASIC**
- **Power ±2V, 4 groups**

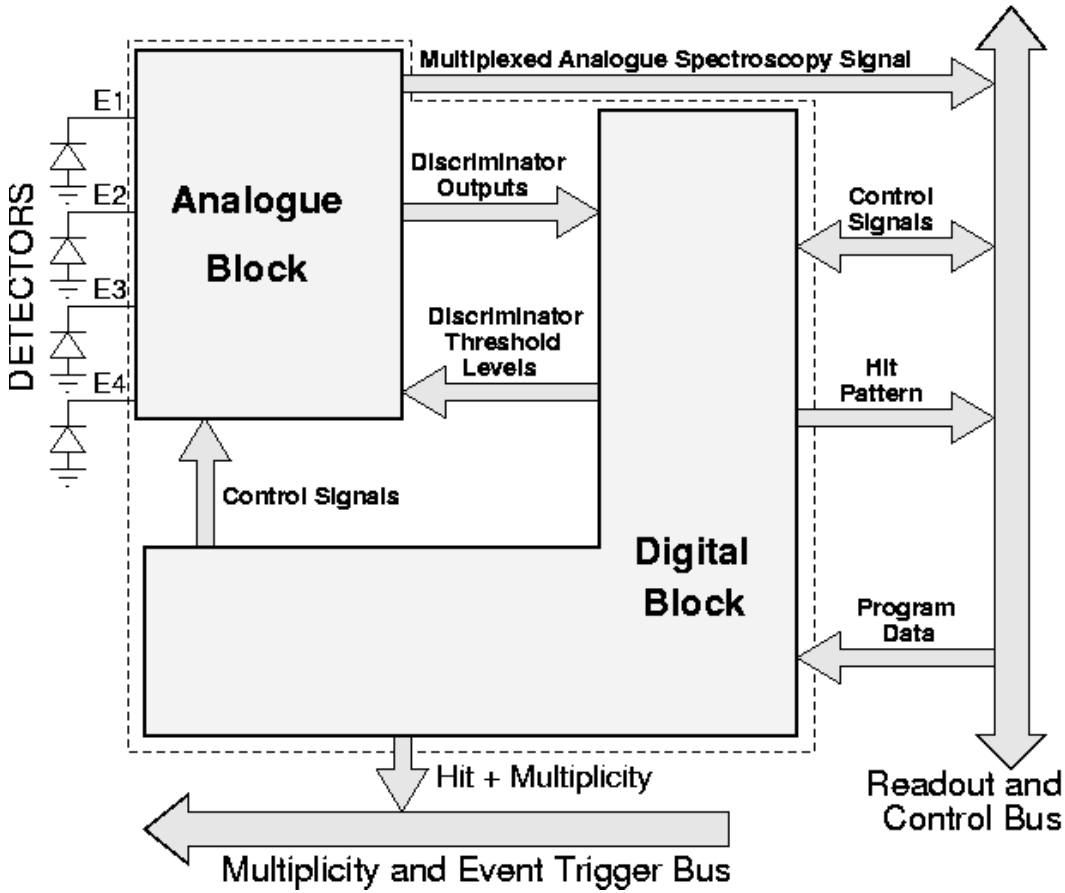
- **Chip technical specification – Detector development group, LU**
- **ASIC design – SINTEF Instrumentation, Oslo**
- **Processed – Austria MicroSysteme International (AMS)**

CHICSi ASIC chip (Mk.2)

Detector telescope + FEE readout chip:

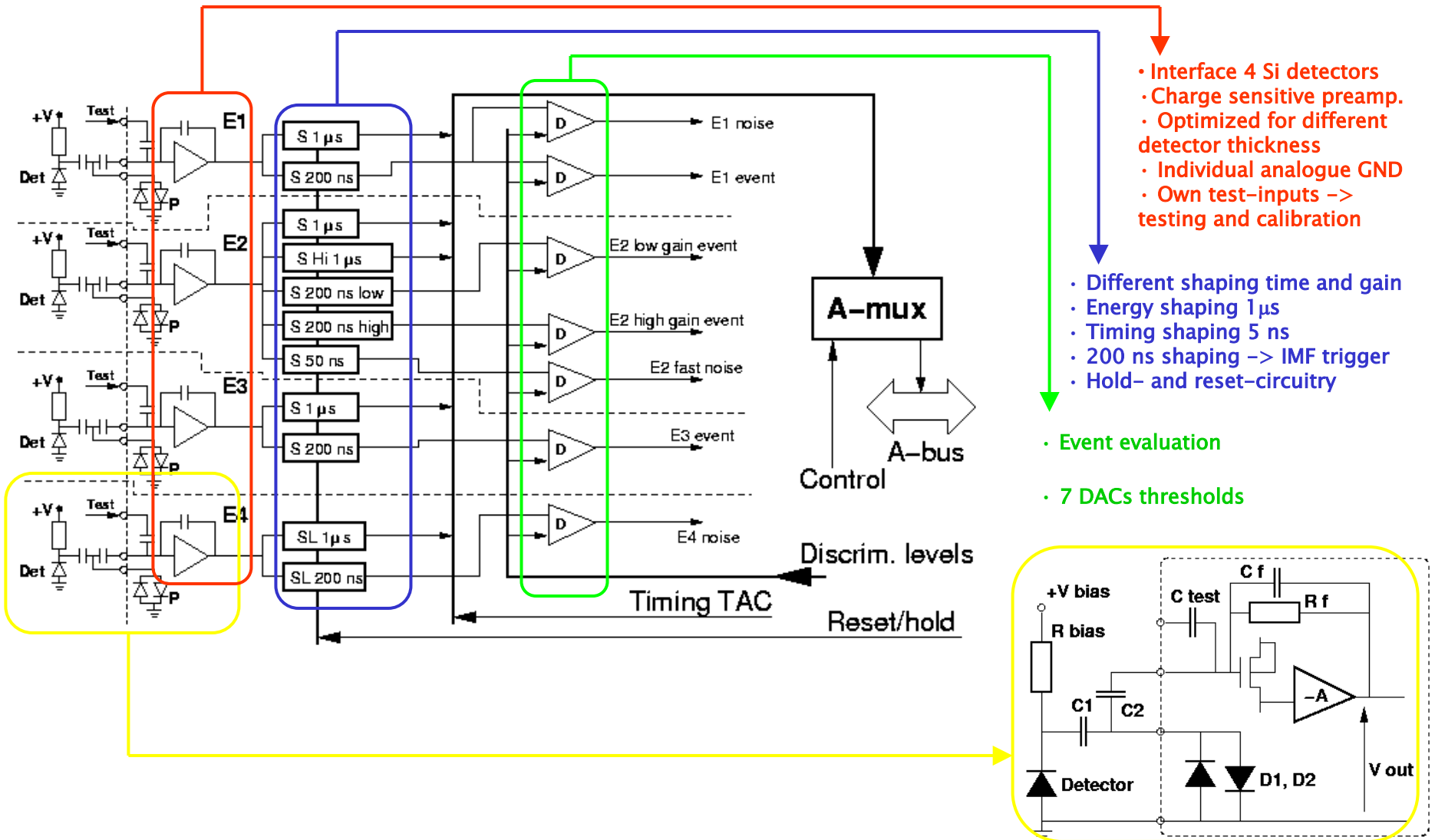
1. Signal conditioning
2. Analogue memory
3. Trigger signal
4. Interface to serial buses readout





CHICSi ASIC chip (Mk.2)

Analogue block schematic



- Interface 4 Si detectors
- Charge sensitive preamp.
- Optimized for different detector thickness
- Individual analogue GND
- Own test-inputs -> testing and calibration

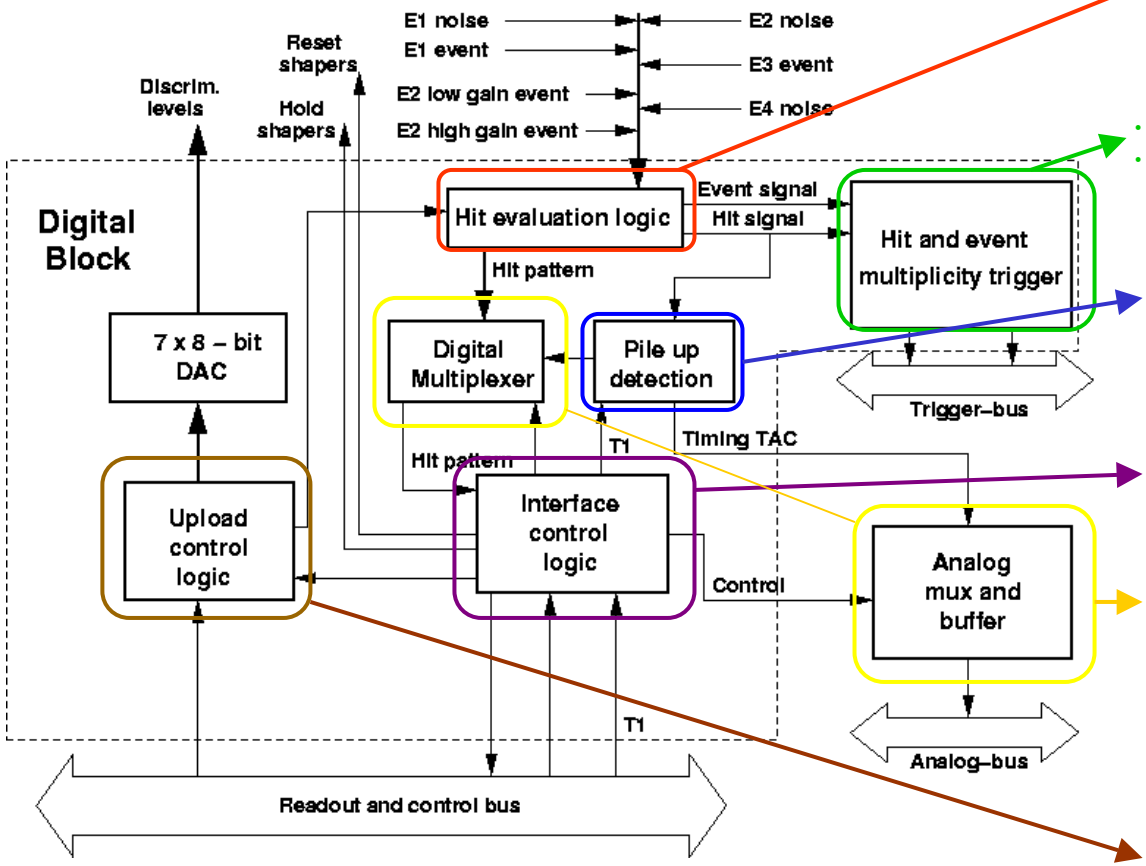
- Different shaping time and gain
- Energy shaping 1µs
- Timing shaping 5 ns
- 200 ns shaping -> IMF trigger
- Hold- and reset-circuitry

- Event evaluation

- 7 DACs thresholds

CHICSi ASIC chip (Mk.2)

Digital block schematic



- Continuously monitor 7 discr. -> searching for interesting particle hits
- Digital info for later readout

- Two defferential current sinks
- HIT -> time 50ns, EVENT -> 200ns

- Local (on chip) pile-up inspector
- Automatic resetting of E-shapers
- Analogue timer

- Controls the readout of analog/dig. data from the chip

- Shifts out sequentially analog/dig. Data
- Dig. and analog data is readout in parallel
- Up to 100kHz (CLK) analogue data
- Up to 10MHz (CLK) only digital info

- Upload programmable parts of the circuits
- 7 x 8-bit DAC
- Trigger signal ON/OFF
- Boolean expression (discr. outputs)-> IMF trigger

CHICSi ASIC chip (Mk.2)
Typical operations

- **Start up**

Power_Up_Reset, Reset, R_WR, CLK, D_Bus: 58 bits/chip (7 x 8 bit DACs + 2 conf. bits)

- **Trigger → Data readout**

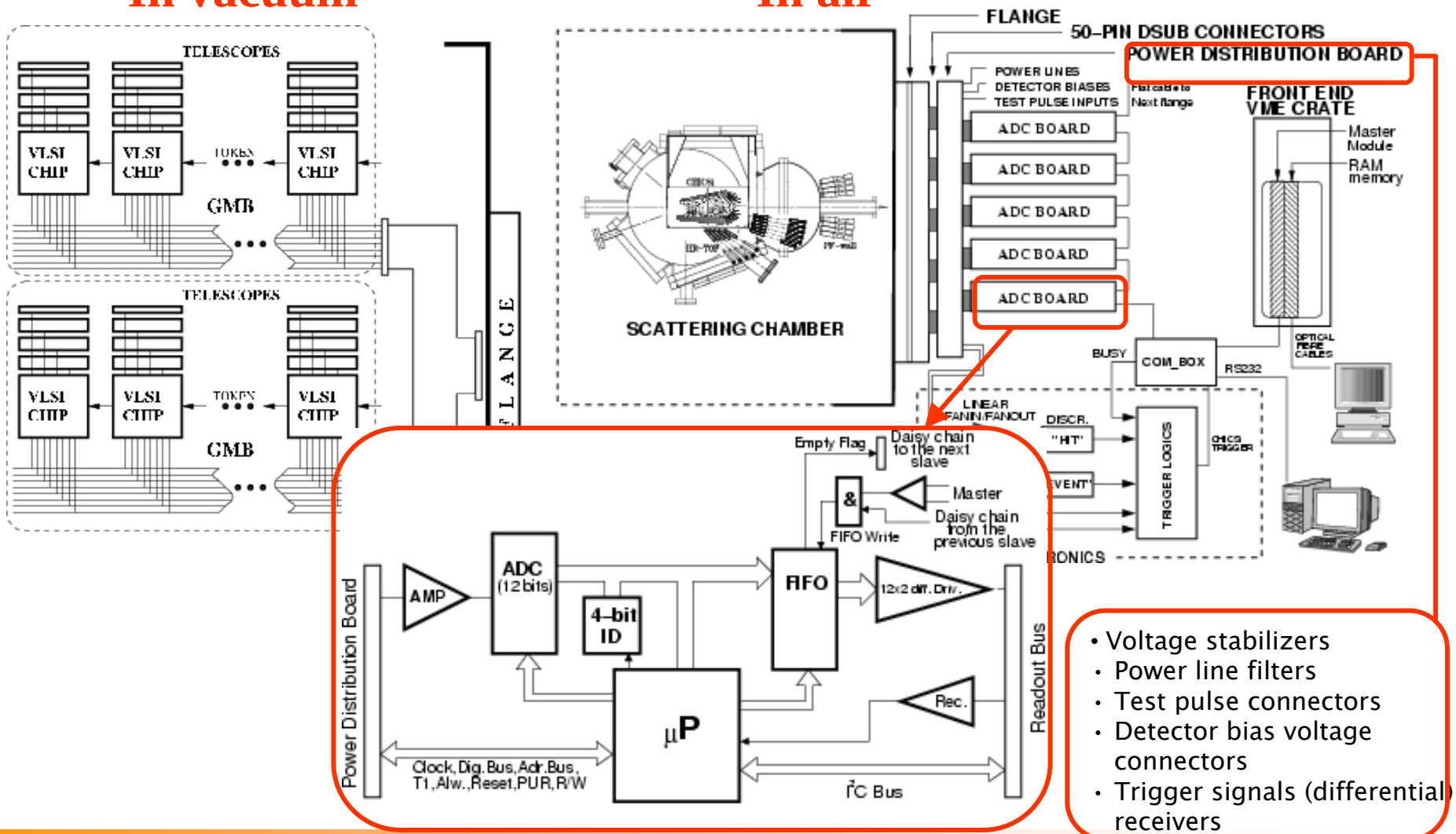
Silent until hit → Level 0 Trigger (HIT, EVENT) → T1 signal from DAQ (1μs) → Readout (8 ***CLKs, Token_in,*** ...) analogue/digital info
IF (no data on chip) → zero data suppression (1 ***CLK, Token_out***)

- **On-line slow control (re-programming)**
  - Change DAC settings
  - Re-program trigger logic
  - ON/OFF chip

CHICSi ASIC chip (Mk.2)

Data Acquisition System

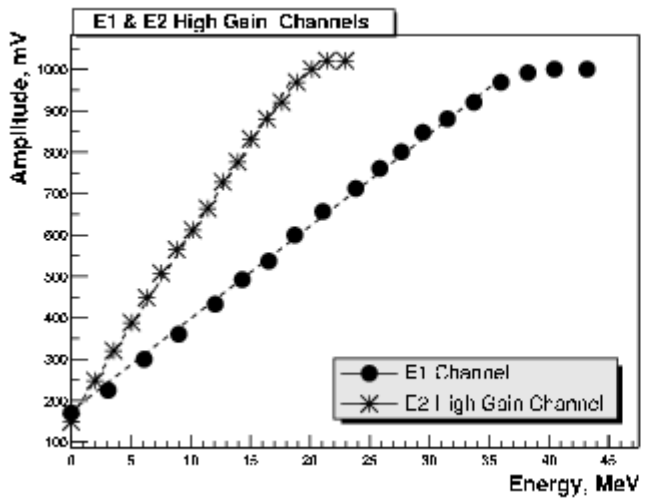
- **In vacuum**
- **In air**

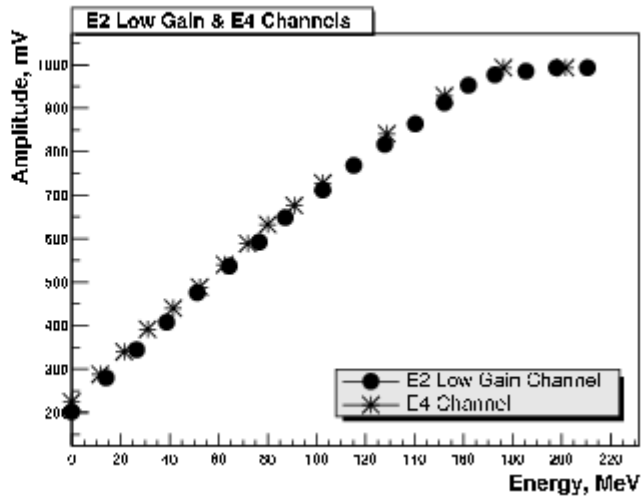


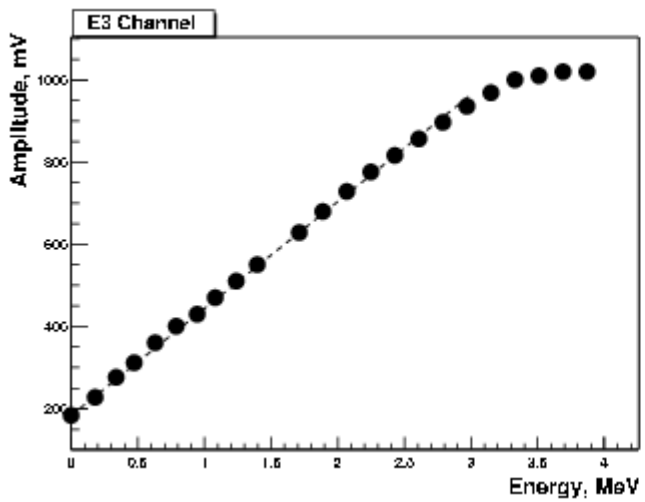
- Voltage stabilizers
- Power line filters
- Test pulse connectors
- Detector bias voltage connectors
- Trigger signals (differential) receivers

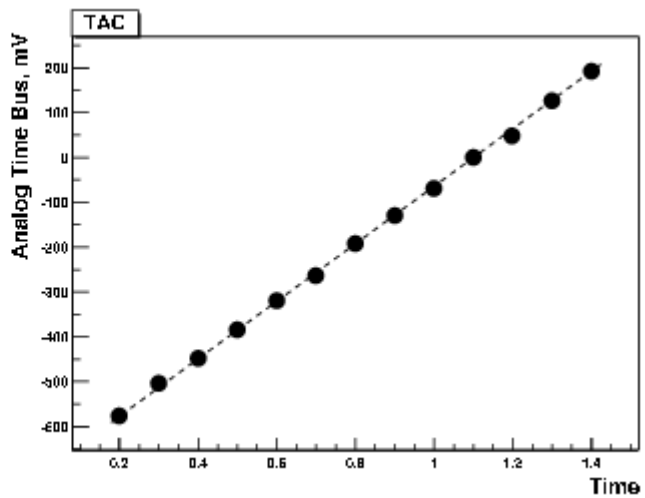
CHICSi ASIC chip (Mk.2)

Chip performance





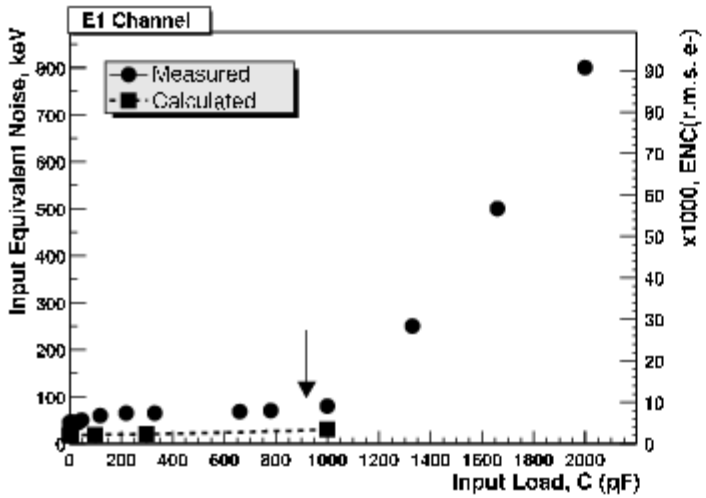


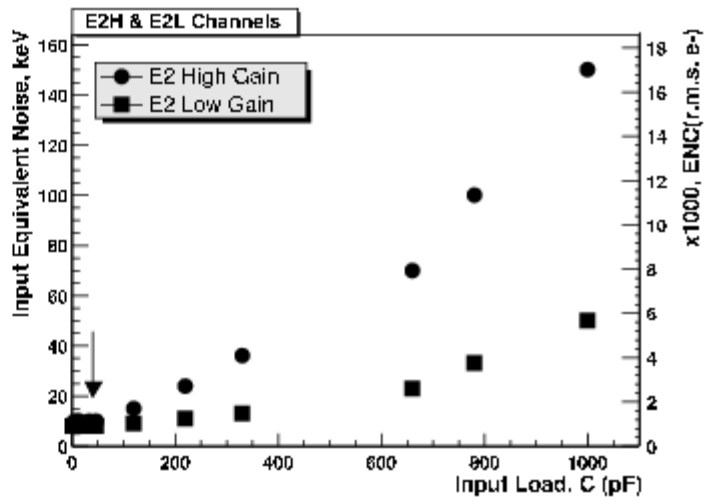


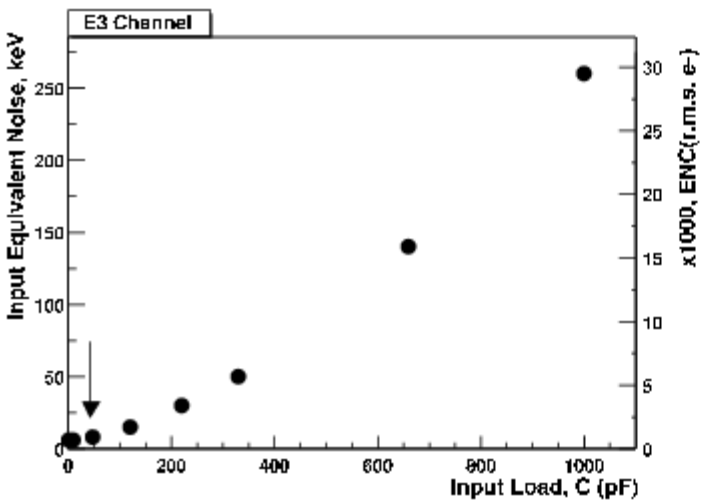
HIT → T1, μs

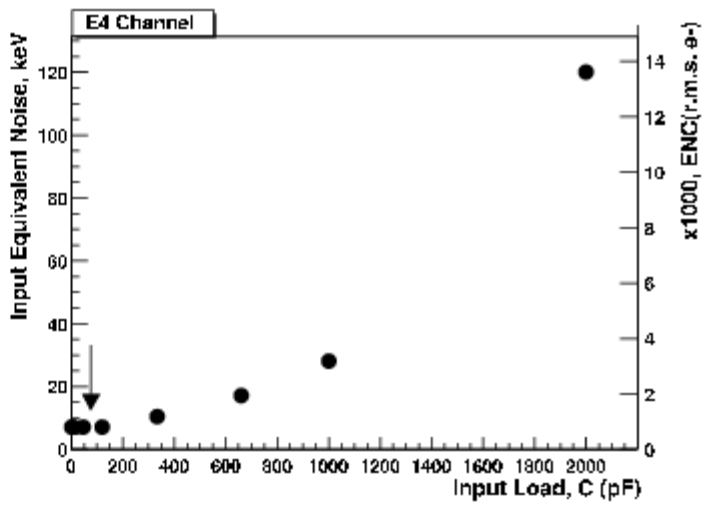
CHICSi ASIC chip (Mk.2)

Chip performance



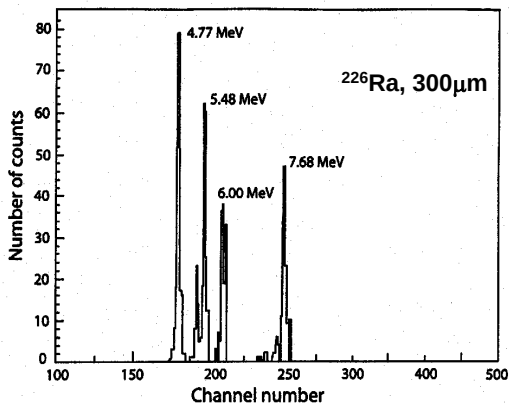


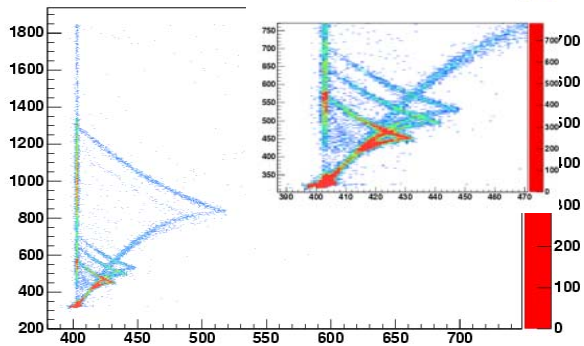


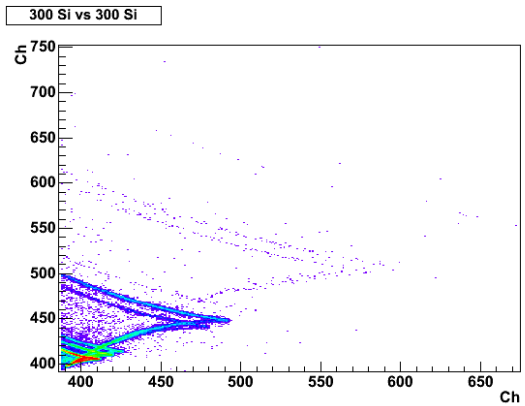


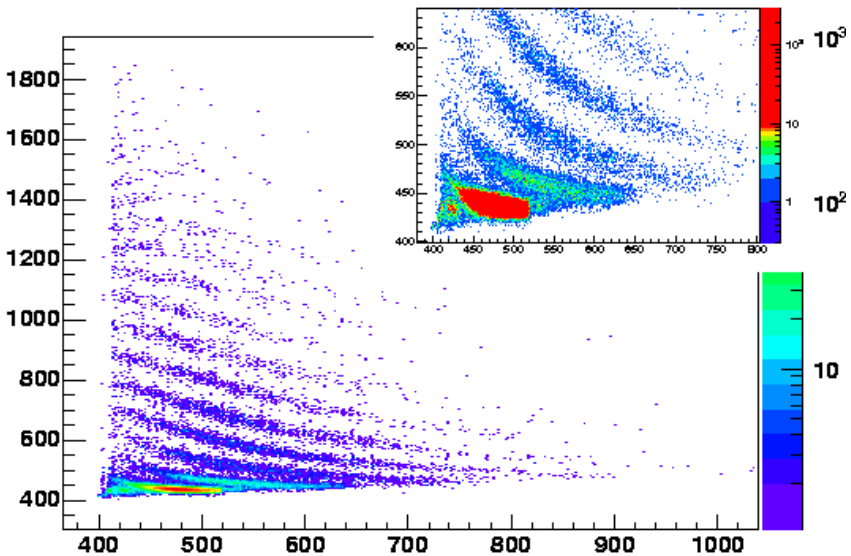
CHICSi ASIC chip (Mk.2)

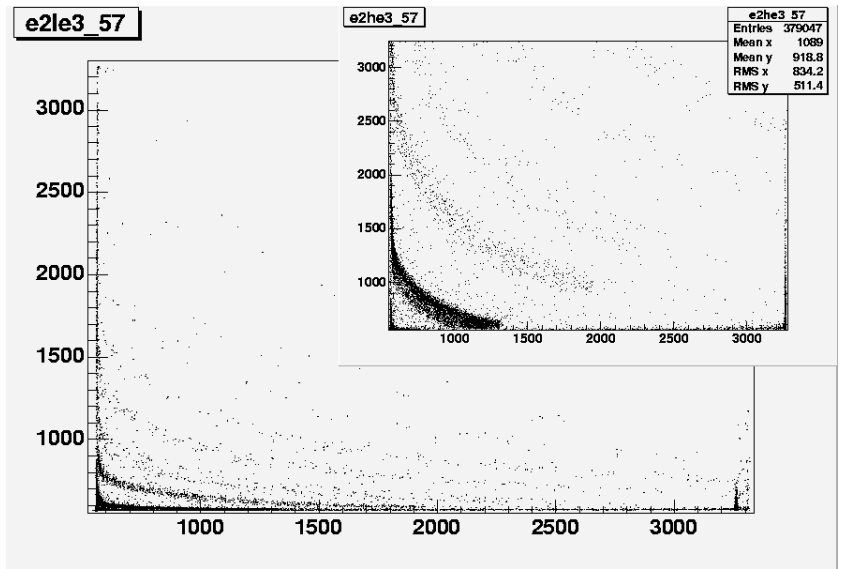
Chip performance



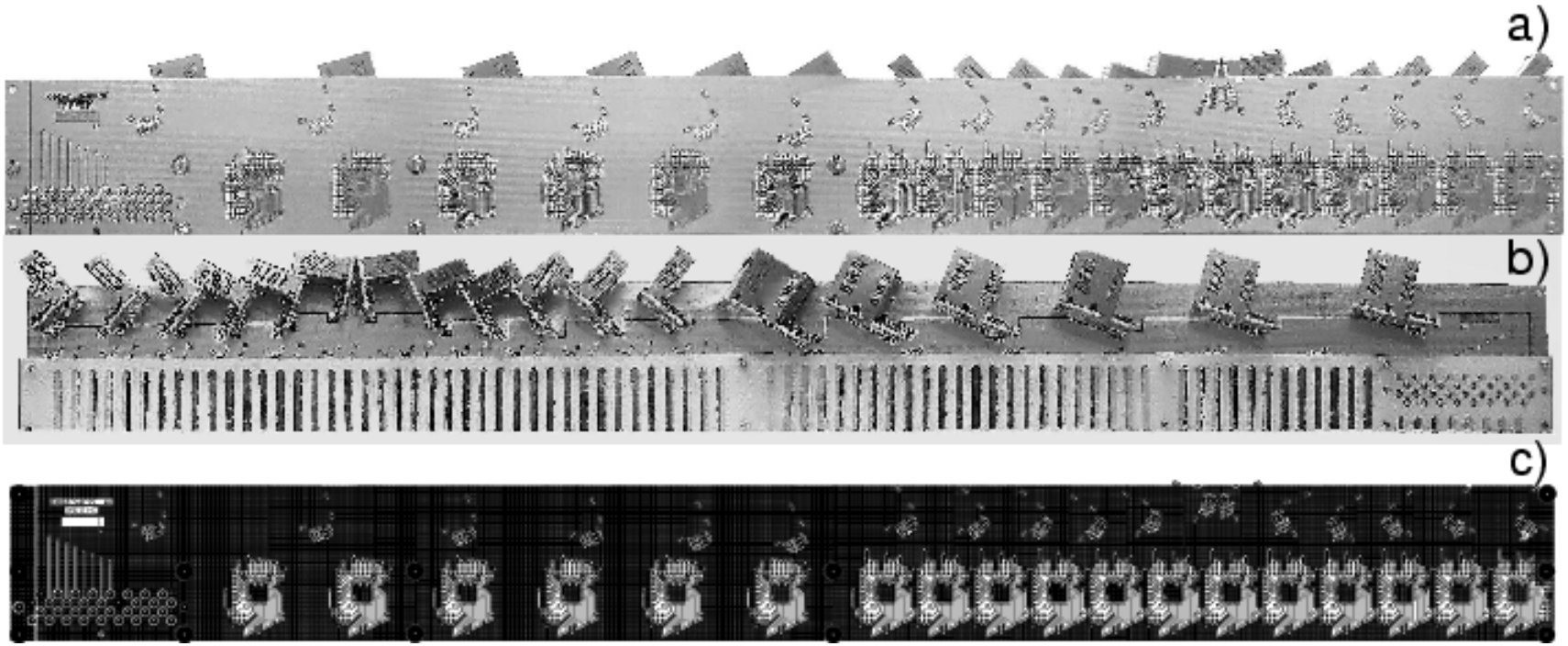








ASIC card in UHV



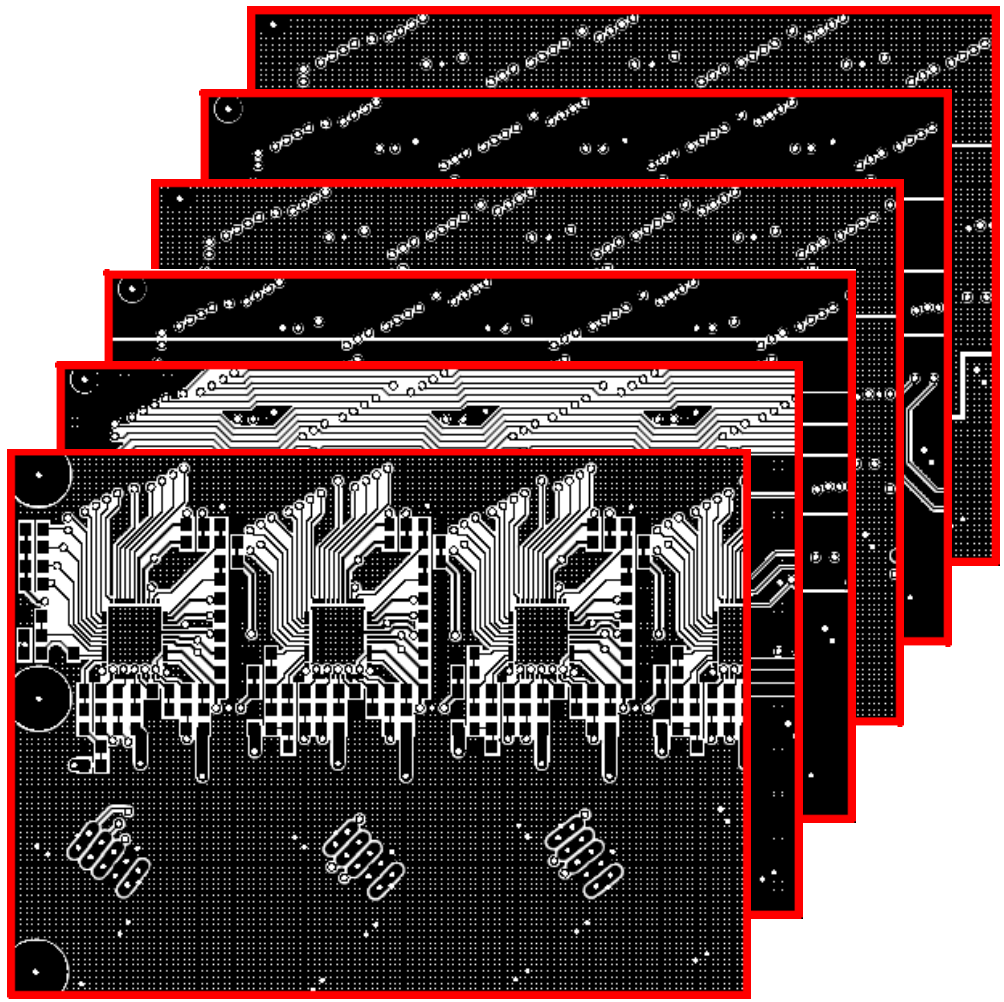
- **Area 450 × 45 mm**
- **Detector telescopes, integrated FEE, connectors, ext. components**
- **FR-4, EPO-TEX H20E**
- **Chip-on-board**
- **Multi-layer (6 layers) design**

ASIC card in UHV

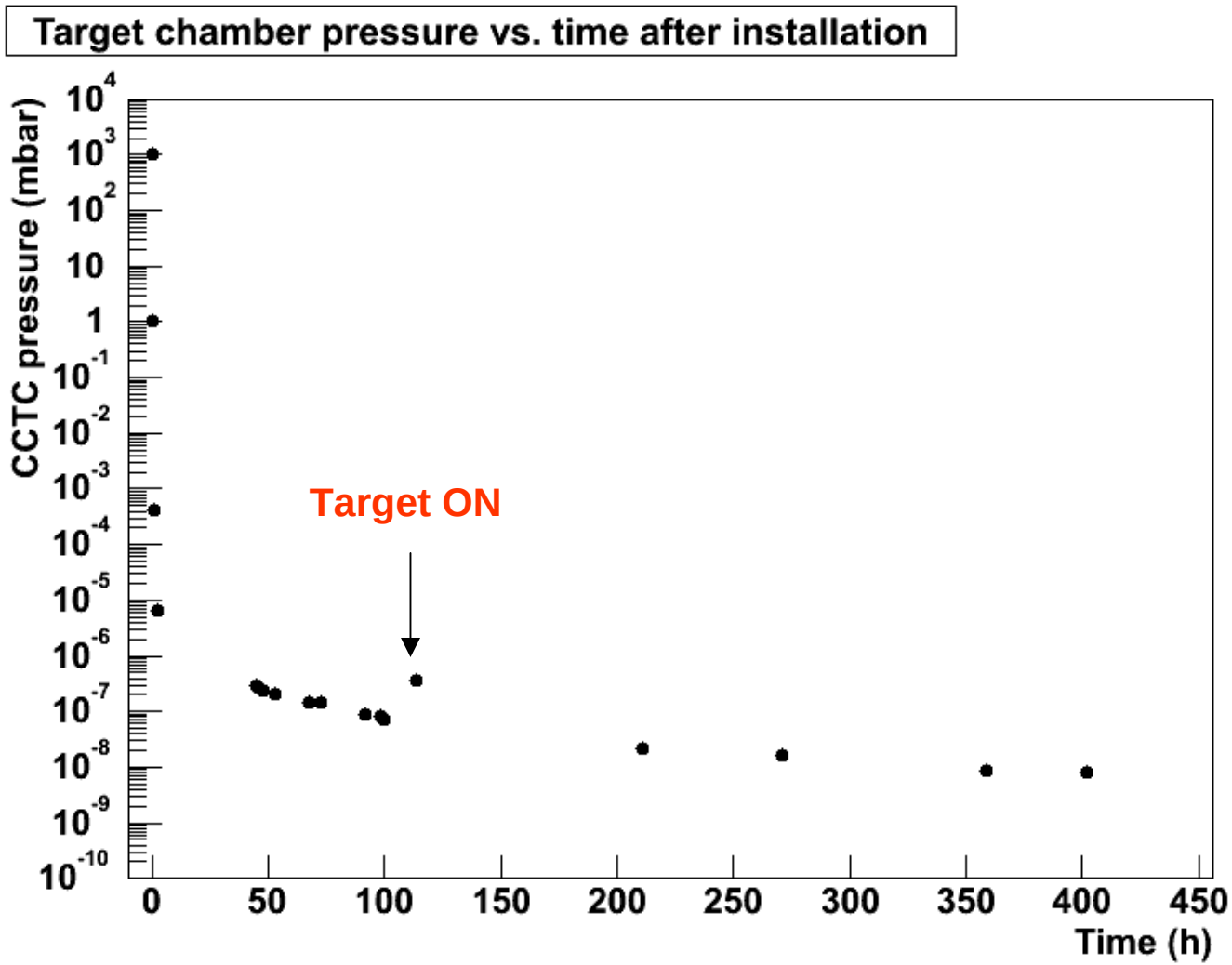
- **Large GMB dimentions + long signal/power lines → pickup, cross talk**
- **4 groups power lines**
- **Test lines**
- **Detector power lines**
- **Differential trigger signalling**
- **Private earth line for each detector**
- **Earth planes on circuit board**
- **Differential trigger signalling**

- **Chip-on-board techniques**
  → next step:
  - **chip-in-cavity**
  - **flip-chip ponding**

- **Simulations**



ASIC card in UHV



Practical experience

Process variations

- Channel to channel
- Chip-to chip
- Wafer to wafer

Intrinsic non-linearity

Amplitude-peaking time dependence

Dynamic calibration

- Programmable DAC test pulse generator
- Generate global calibration data-base that relates signal in channel to real units

Differential signalling

- Trigger signals
- Spectroscopic signals

Programming

- Chip ON/OFF
- Test inputs ON/OFF
- On-chip trigger logic

External components

- RC chip (biasing resistors)
- Integrate ext. elements

Noise reduction & on-chip cross-talk

- Chip design and process
- Bonding
- Simulations

Practical experience

Standard interface

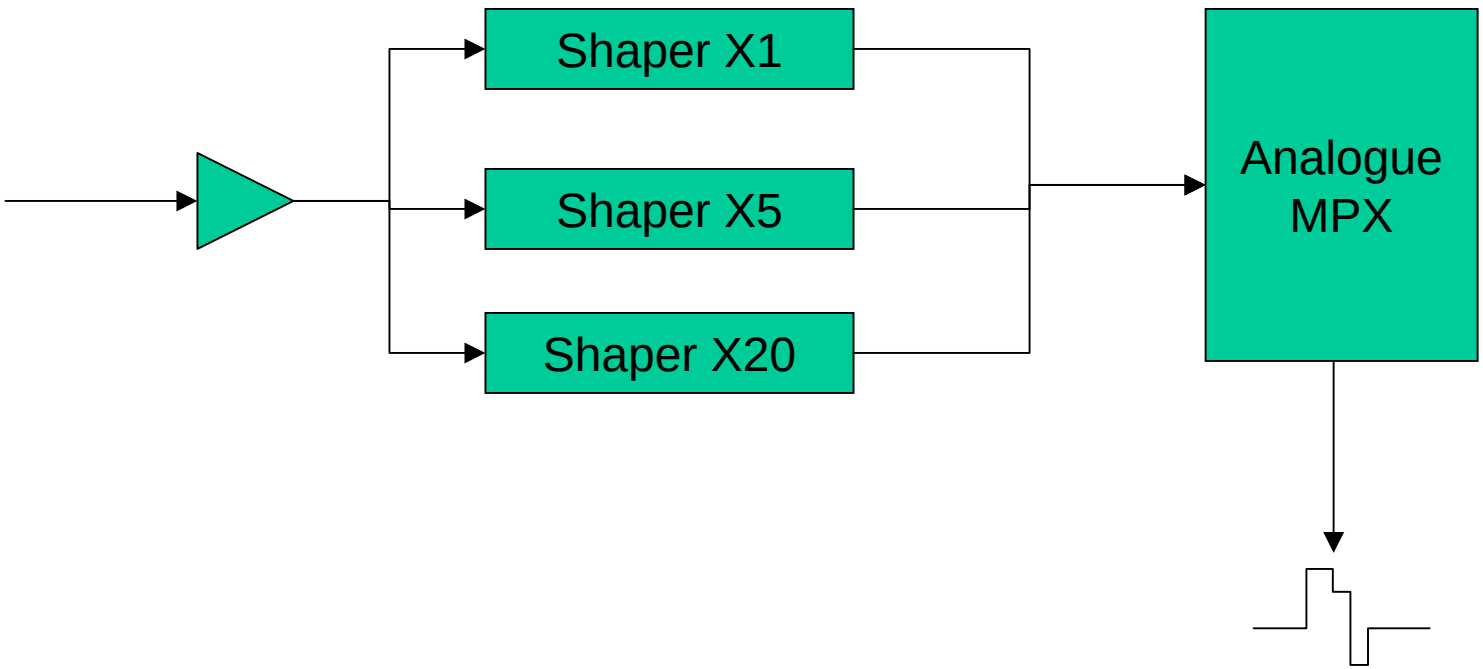
- Single wire
- Wireless (except power lines)
- USB 2.0 is standard (supports buses up to 32 bits wide)
- Easy to find standardized controller and transceivers chips for USB 2.0
- Advantage in UHV

	Standard	Bandwidth	Type
	USB 1.1	12 Mbps	Wire connection
→	USB 2.0	480 Mbps	Wire connection
→	WLAN 802.11a	54 Mbps	Wireless
	WLAN 802.11b	11 Mbps	Wireless
	Firewire	800 Mbps	Wire connection
	Bluetooth	1 Mbps	Wireless

Implementation of different gains

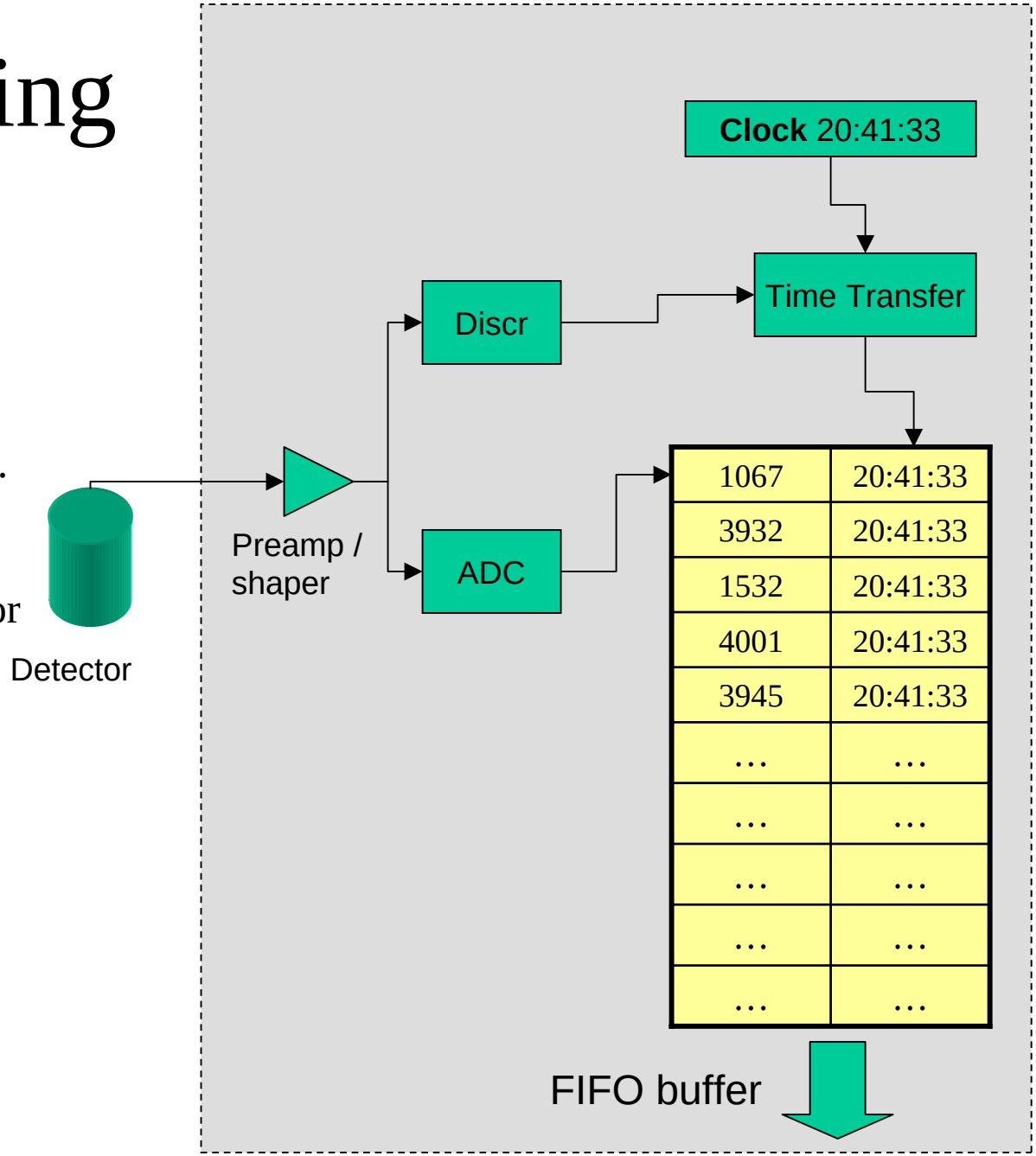
- **Golden rule** – never reject physically important information

- Not easily possible to change gain on chip – complex circuit needed
- Solution: Use standard fixed-gain modules with different gains and read out all signals.



Time-stamping

- Modern approach to time domain analysis of very high number of readout channels for coincidence and ToF data.
- Based on recording time stamp data with every detector event.



GPS time synchronisation

- GPS – Global Positioning System
- GPS provides global position and time services
  - Standard positioning service (SPS) ±170 ns
  - Precise positioning service (PPS) ±100 ns

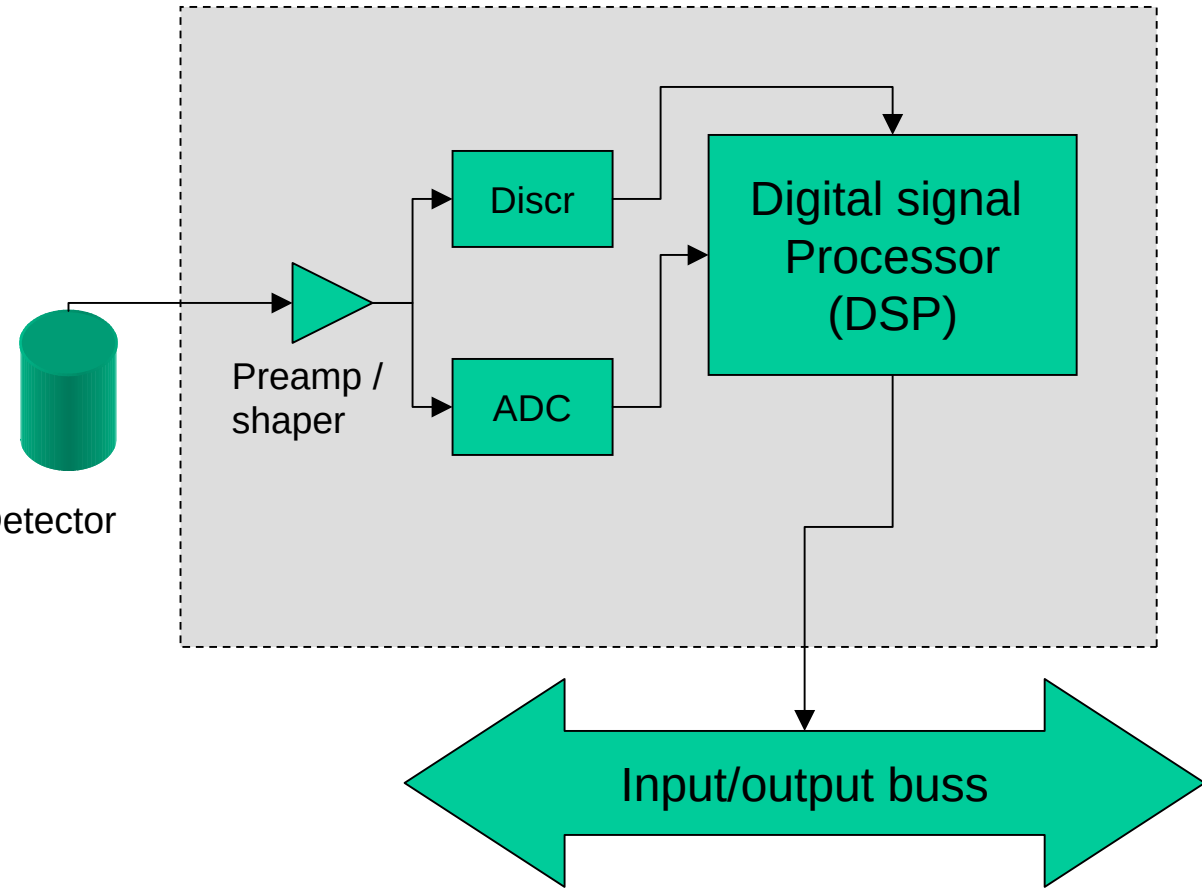
- Common mode time transfer using GPS
  - Time synchronisation within ± 5 ns over 2 000 km

- GPS time synchronisation could be integrated on the same chip as the readout electronics.

Idea's from Pete Jones & Harry Whitlow, JYFL

DSP approach

- Idea use high speed digital processor to extract energy, position and time information form each post.
- Possibility to correct for ballistic effects, plasma recombination and also extract *limited* position information
- Useful reduction of chip area as digital electronics is more compact than analogue electronics
- Extreme requirement on sampling ADC
- Noisy fast clock for DSP needed.



Input noise contributions

Flicker

$$ENC = \frac{2.71\left(C_{\det} + C_{in}\right)}{e}\sqrt{\frac{F_k}{2WL}}$$

Channel

$$ENC = \frac{2.71\left(C_{\det} + C_{in}\right)}{e}\sqrt{\frac{\Gamma kT}{3\tau_p g_m}}$$

Bulk

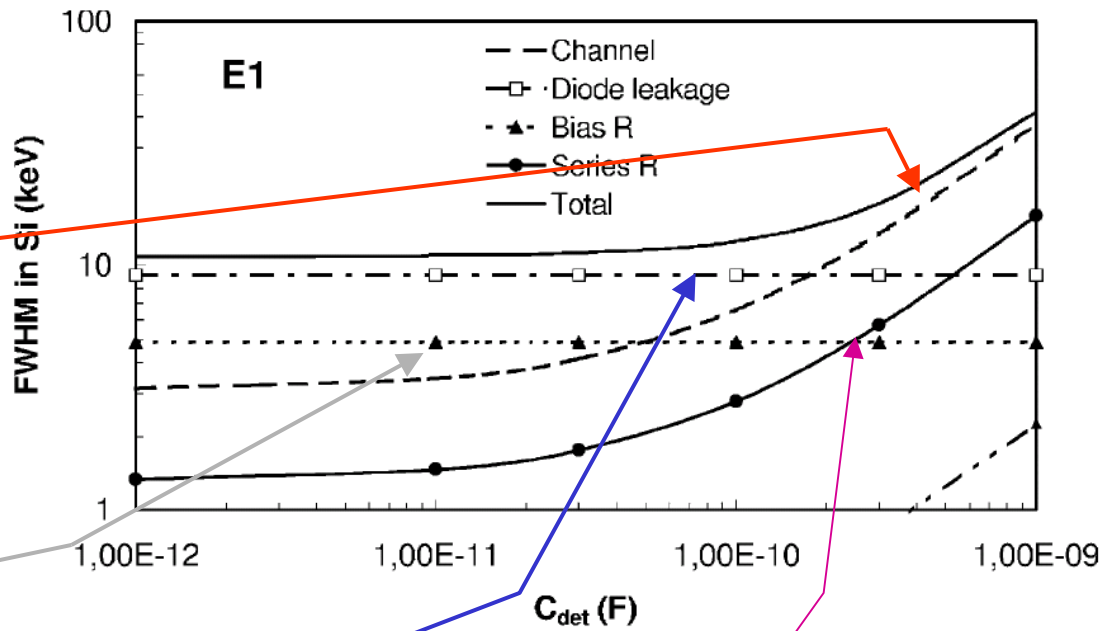
$$ENC = \frac{2.71\left(C_{\det} + C_{in}\right)}{e}\sqrt{\frac{R_{bulk}\eta^2 kT}{2\tau_p}}$$

Bias resistor noise

$$ENC = \frac{2.71}{e}\sqrt{\frac{\tau_p kT}{2R_p}}$$

Diode leakage

$$ENC = \frac{2.71}{e}\sqrt{\frac{eI_{\det}\tau_p}{4}}$$



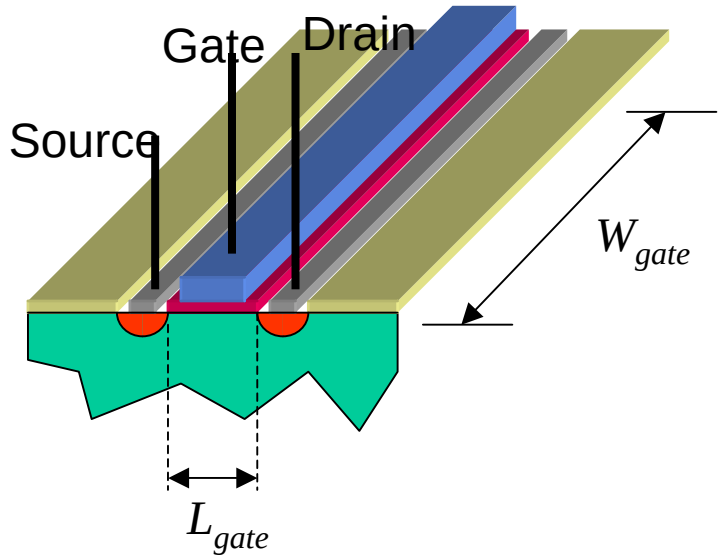
Series resistor

$$ENC = \frac{2.71\left(C_{\det} + C_{in}\right)}{e}\sqrt{\frac{R_{rseries} kT}{2\tau_p}}$$

Process gate width

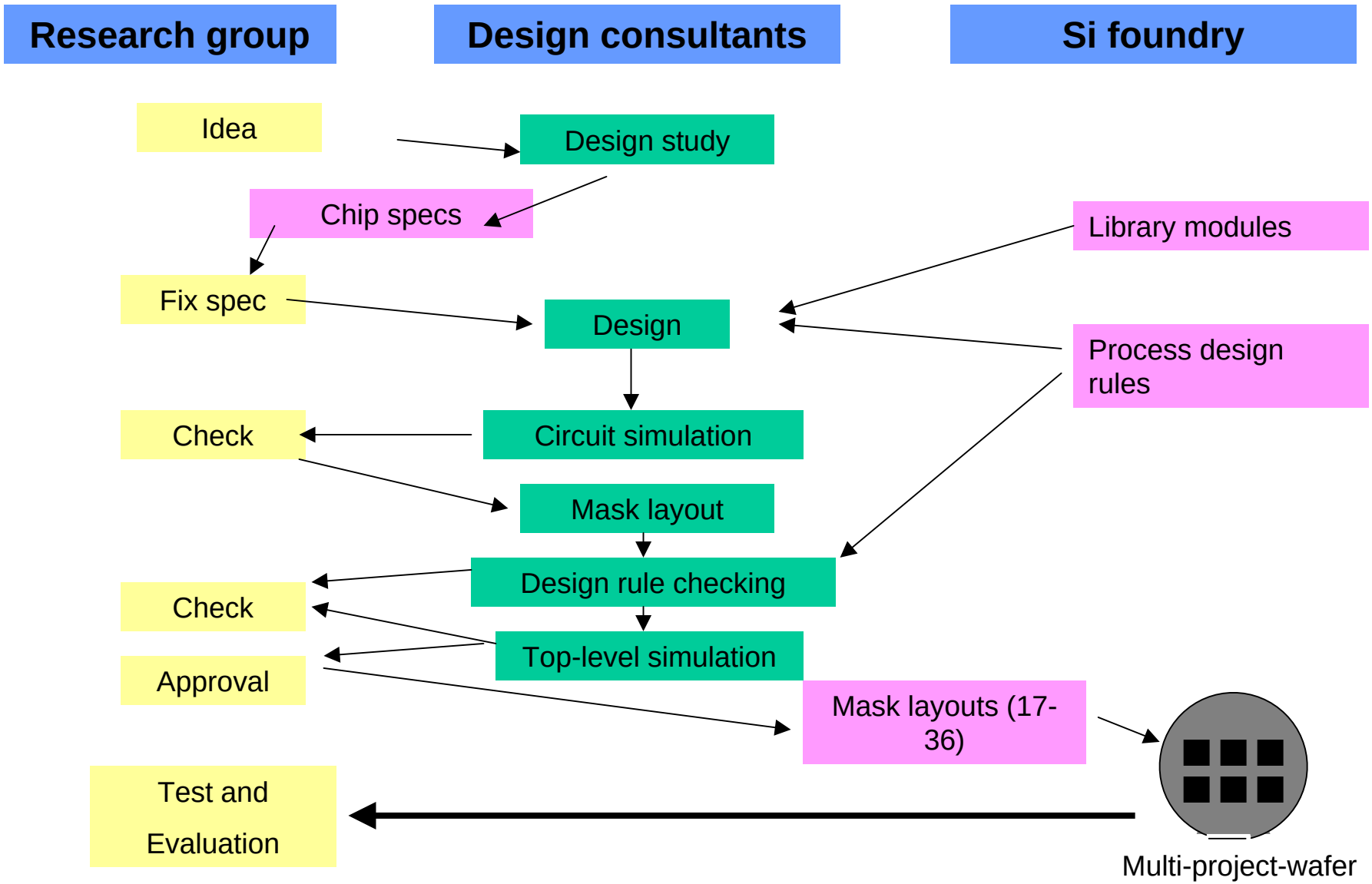
- If both channel length, *L*, and oxide thickness, t_{ox}, is scaled by $1/\kappa$ and we want to hold on to the criteria $C_{in} = C_{det}/3$
- The transconductance is increased by κ and noise by:

$$\sqrt{1/\kappa}$$



L_{gate}	**Relative noise**
0.8 µm (CHICSi Mk2 chip)	1
0.18 µm	0.47
90 nm	0.37

ASIC process



PICA
(Pulse Instrumentation Chip for analytical Applications)

Electronic configurations for most forms of pulse spectroscopy measurement are very closely similar →
Solution: integrate electronic readout system
(suited for a wide range of physical pulse spectroscopy measurements) into an ASIC chip

- **Standard interface**
  - **IEEE 801.b wireless or USB 2.0**
  - **Low power consumption**
  - **”Happy measurement” concept**
- **Significant user cost reduction**
  - **Drastically reduced energy cost**
    - **Energy cost for 1000 channels NIM: 350 000 SEK/yr: PICA 440 SEK/yr**
    - **Reduced floorspace**
  - **Eliminate bulky and expensive cable trunks**
  - **Mobile and battery operation**
    - **Remote monitoring**
- **No need for expensive software engineering**
  - **Simple upgrade**
  - **Simplified diagnostic**
  - **Standard software**
    - **e.g. LabView**

Our products

a. **Standard PICA chip.** This is a flexible readout chip for pulse processing electronics.
b. **Standard PICA units.** This is a packet solution on a board including standard chip + software + interface. It represents a radical new approach to pulse processing electronics by providing a standard chip that is capable of a wide range of measurements and provides a low-cost *standard* interface to PCs for data collection.
c. **Development of special chips** for high volume special applications based on adoption of the circuit design modules for the PICA chip to tailor them for special applications.

Summary and outlook (for ASIC design)

- Use a professional design consultant
- Select the process carefully – many are only available for a few years.
- **Never, ever modify a process.** Use a standard process with the function already included.
- Use standard modules for amplifiers, gates, DAC's, ADC's, counters, interface circuits. No need to re-invent the wheel.
- Make complex functions by combining many standard modules
- Include test probe pads where possible – in case things go wrong.
- Assume process variations are large.
- **Simulate.**