TECHNISCHE UNIVERSITÄT
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# A Multi Gigabit Clock and Data Recovery Testchip fabricated in 0.18µm CMOS

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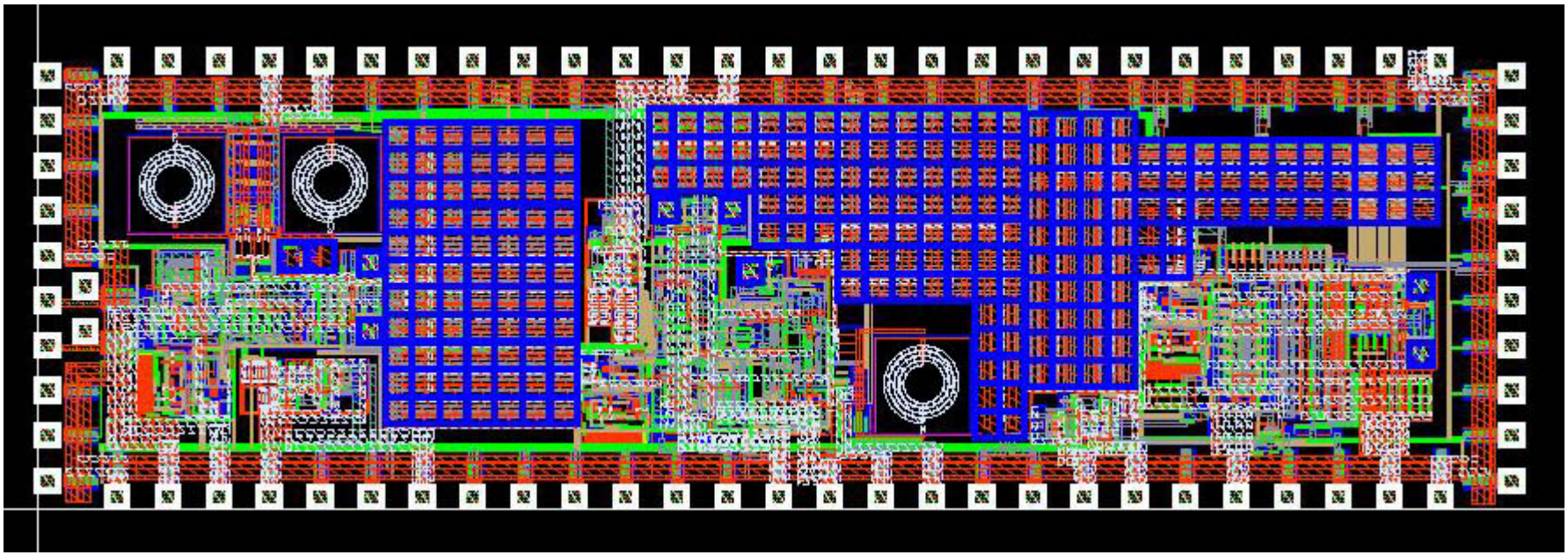
## Introduction

• In standard SerDes system, each transceiver has its own local reference clock.
• If clock is distributed through serial data port, clock and data recovery (CDR) circuit has to operate without local reference clock.
• The recovered clock must have sufficient jitter performance to be used as reference clock for local components such as ADC or serializer.
• The conventional half-rate-clock CDR using ring-based oscillator, as using in OASE, do not have sufficient jitter performance.
• Therefore, the feasibilities of low jitter CDR using LC-based oscillator and the improved $1/4^{th}$-rate-clock CDR using ring-based oscillator are investigated.

**Clock Data Recovery (CDR) Testchip**

Technology : UMC 0.18 µm CMOS with RF options

Chip Area : 1525 µm x 4960 µm



CDR-1

- with Quadrature-phase LC-VCO
- full-rate-clock architecture
- current-mode-logic style
- quadricorrelator frequency detector

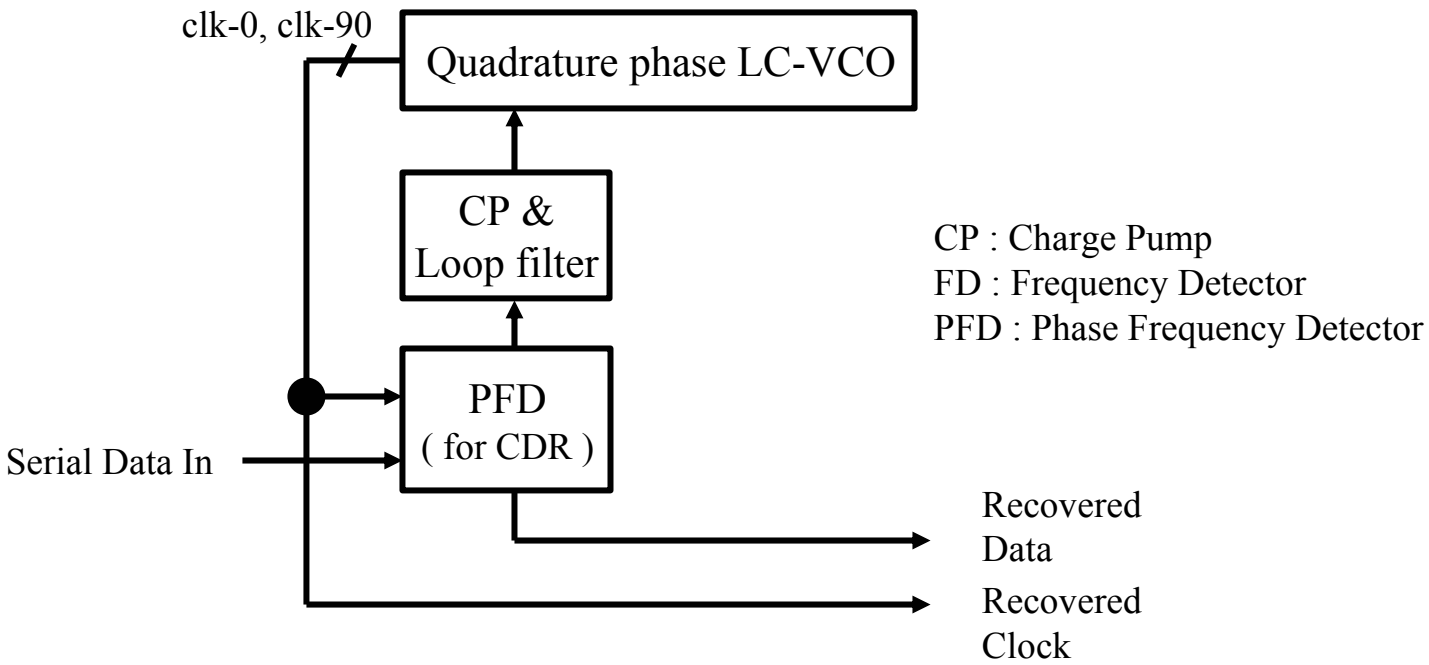
CDR-2

- with LC-VCO and clock delay unit for f-detector
- full-rate-clock architecture
- current-mode-logic
- quadricorrelator frequency detector

CDR-3 with 1:4 DEMUX

- with 8-phase ring oscillator
- $1/4^{th}$ -rate-clock architecture
- low power CMOS logic style
- parallel architecture quadricorrelator frequency detector

# Test structure CDR-1 “CDR full-rate Quadricorrelator FD Structure”



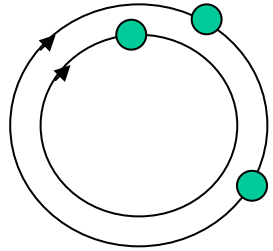

- CDR can operate without local reference clock.
- Quadricorrelator frequency detector can provides information of frequency difference between VCO clock and serial data steam.
- CDR with FD can have low loop bandwidth and wide pull-in range.

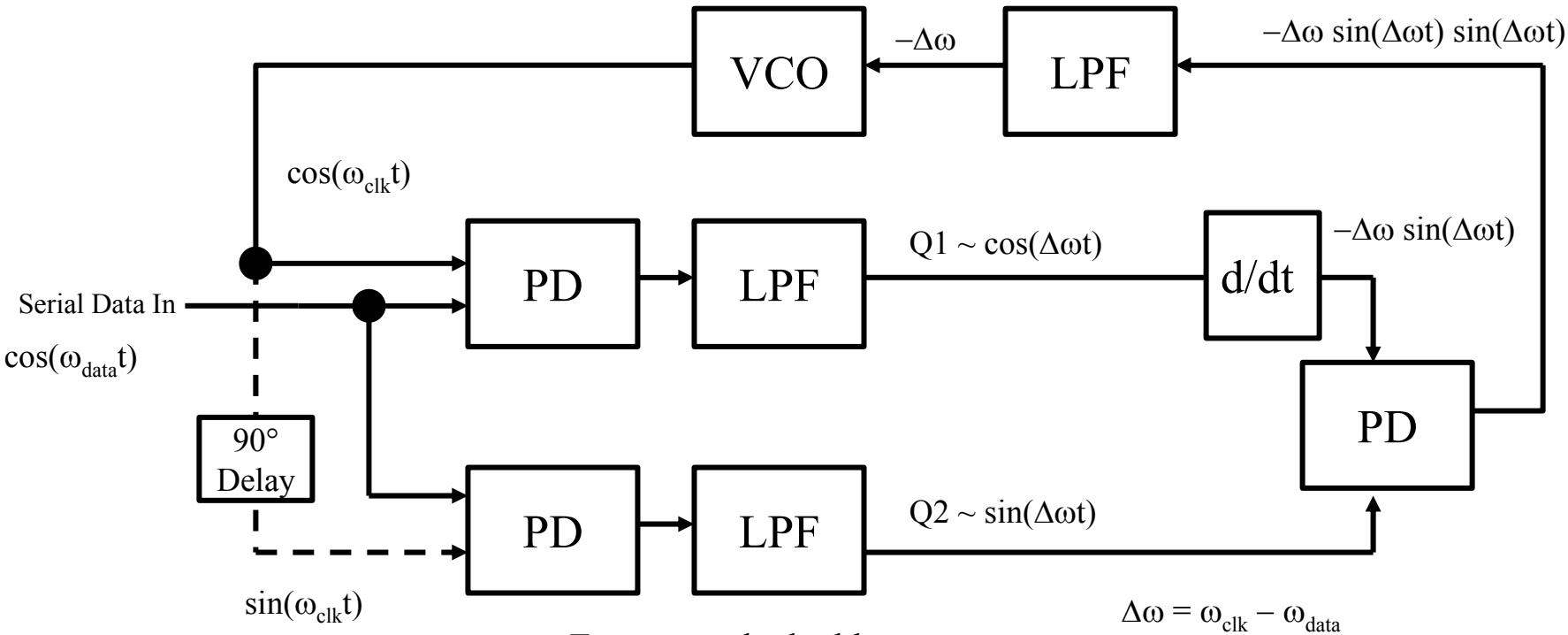
# Principle of quadricorrelator frequency detector

- consists of 2 sets of phase detector with different clock phases
- Q1 and Q2 show the frequency difference.
- Phase difference of Q1 and Q2 shows the sign of frequency difference.

Ex. If $\Delta\omega$ is positive Q1 leads Q2

If $\Delta\omega$ is negative Q2 leads Q1 because $\sin(-\Delta\omega t) = -\sin(\Delta\omega t)$

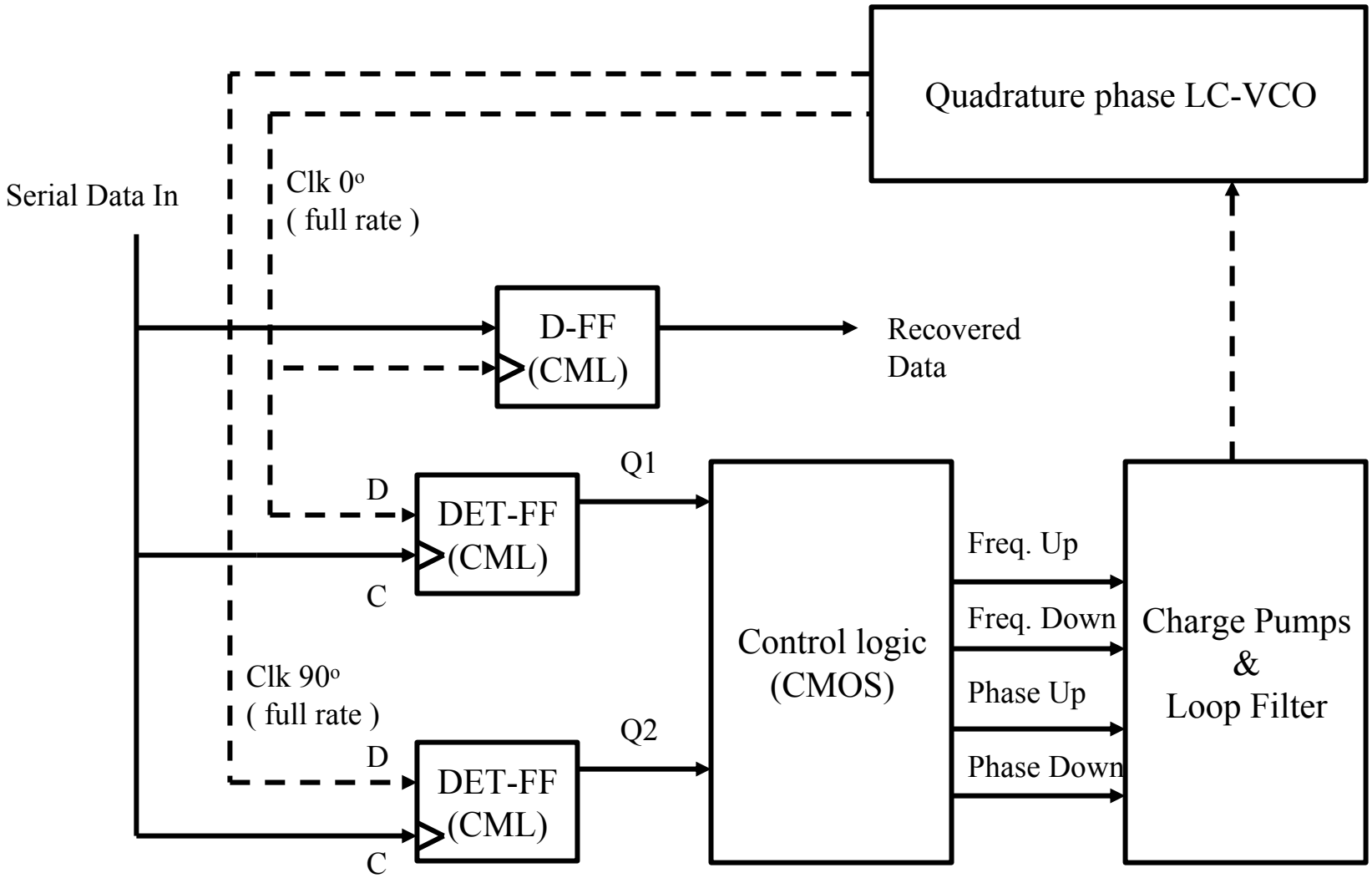




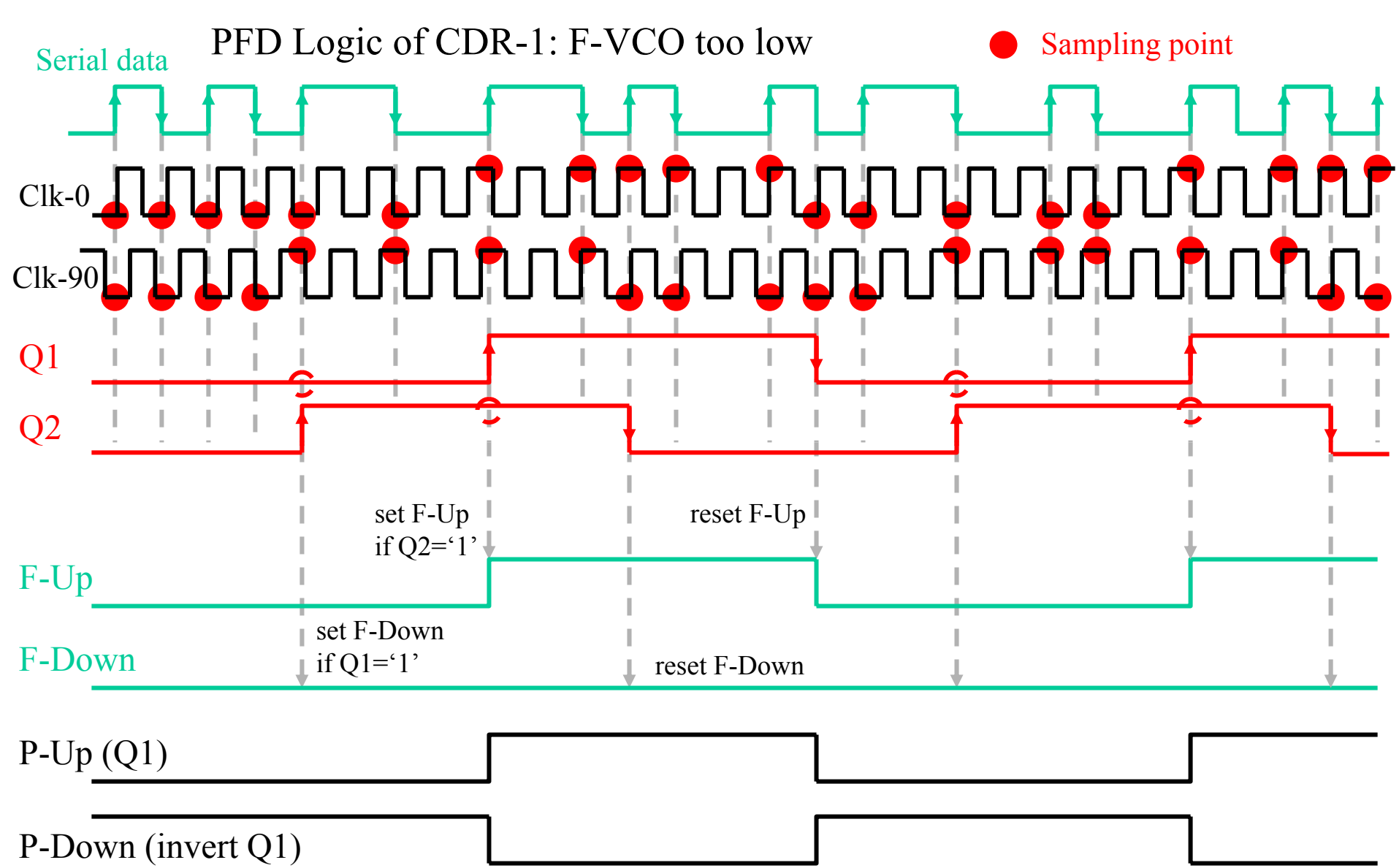

Frequency-locked loop

PD : Phase Detector
LPF : Low-passed Filter

# CDR using digital quadricorrelator frequency detector

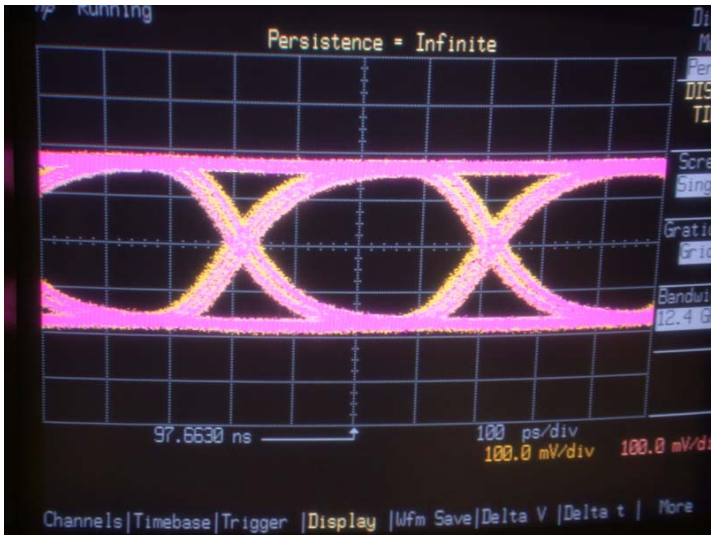



DET FF : Double-edge-triggered Flipflop

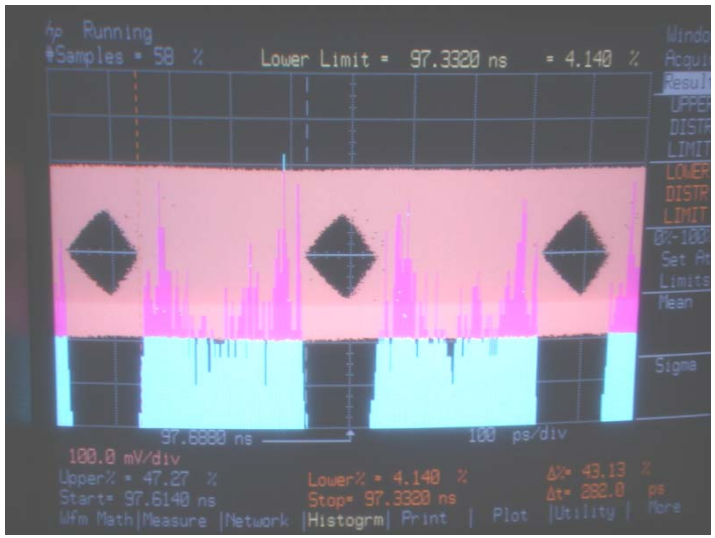



- Both edges of serial data sampling clk-0 and clk-90 to generate Q1 and Q2.
- Q1 and Q2 are used to generate F-Up, F-Down, P-Up and P-Down.

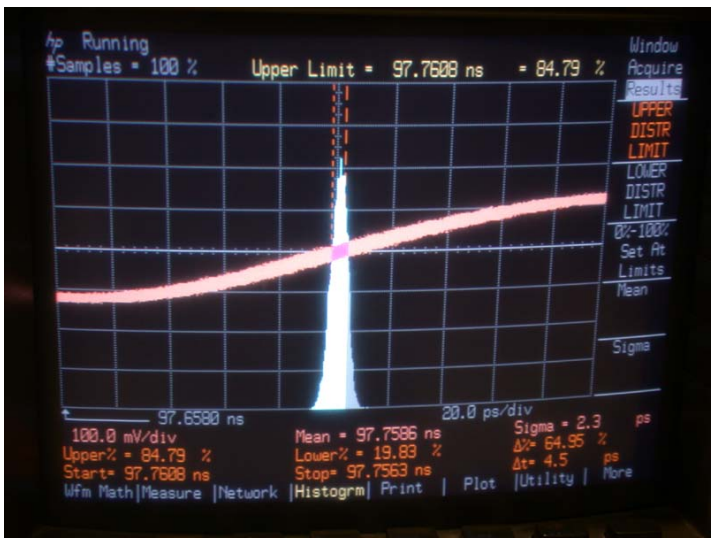
# Measurement results : CDR-1



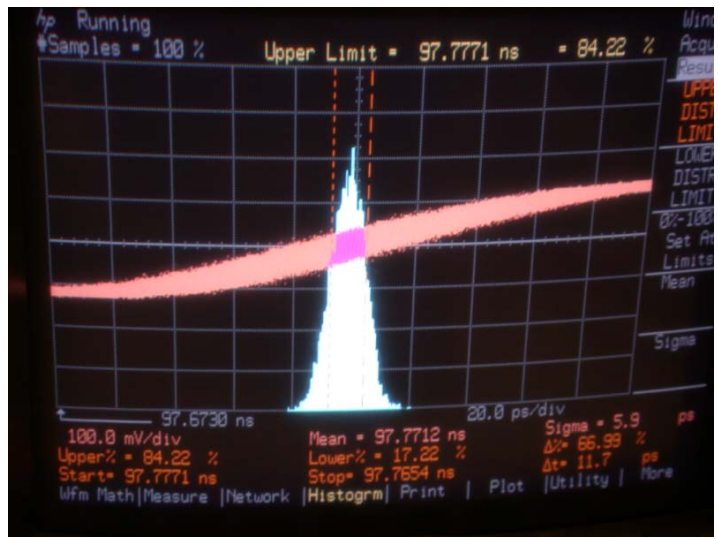

a) Incoming serial data in, 2.5 Gbps, PRBS $2^7$-1




c) Incoming serial data in, 2.5 Gbps, jitter 280 ps,p-p (0.7UI) at 10MHz. modulation

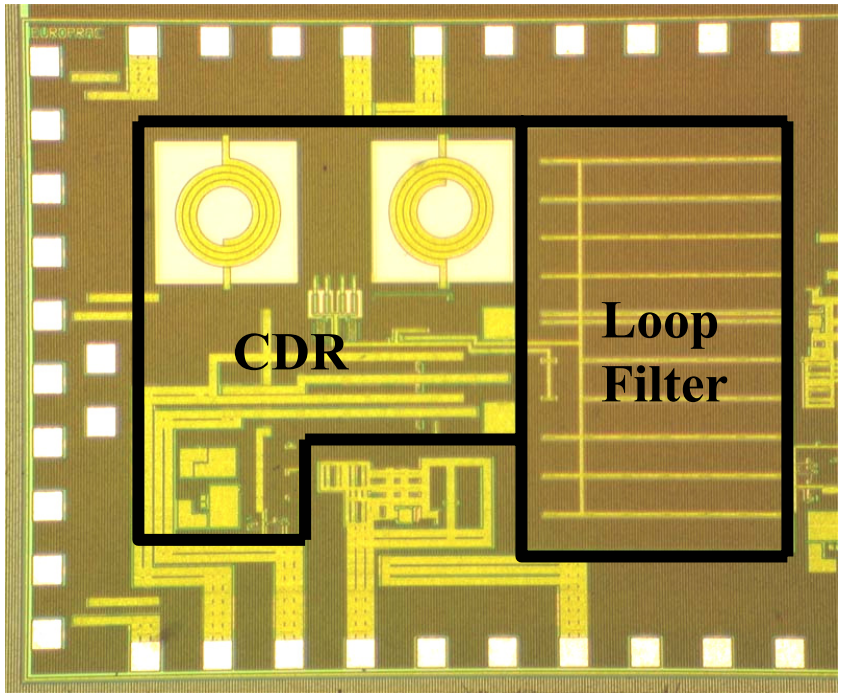



b) Jitter histogram of the recovered clock, 2.5 GHz., jitter 2.3 ps, rms




d) Jitter histogram of the recovered clock, 2.5 GHz., jitter 5.9 ps, rms

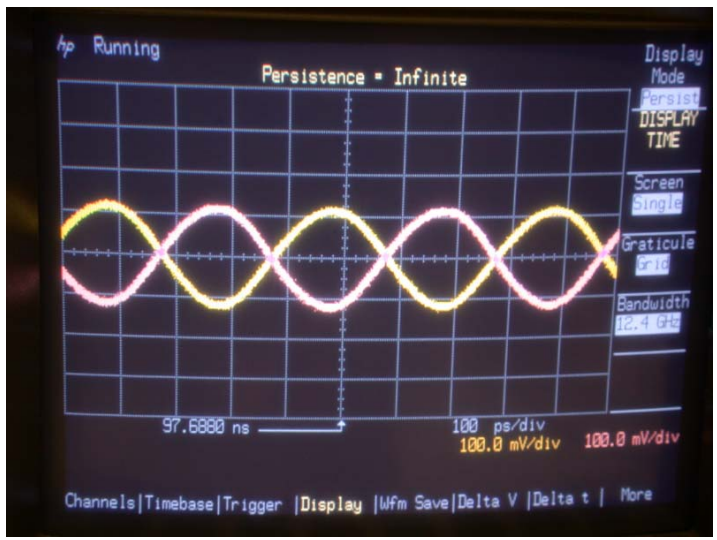
# Measurement results : CDR-1




Die Photograph

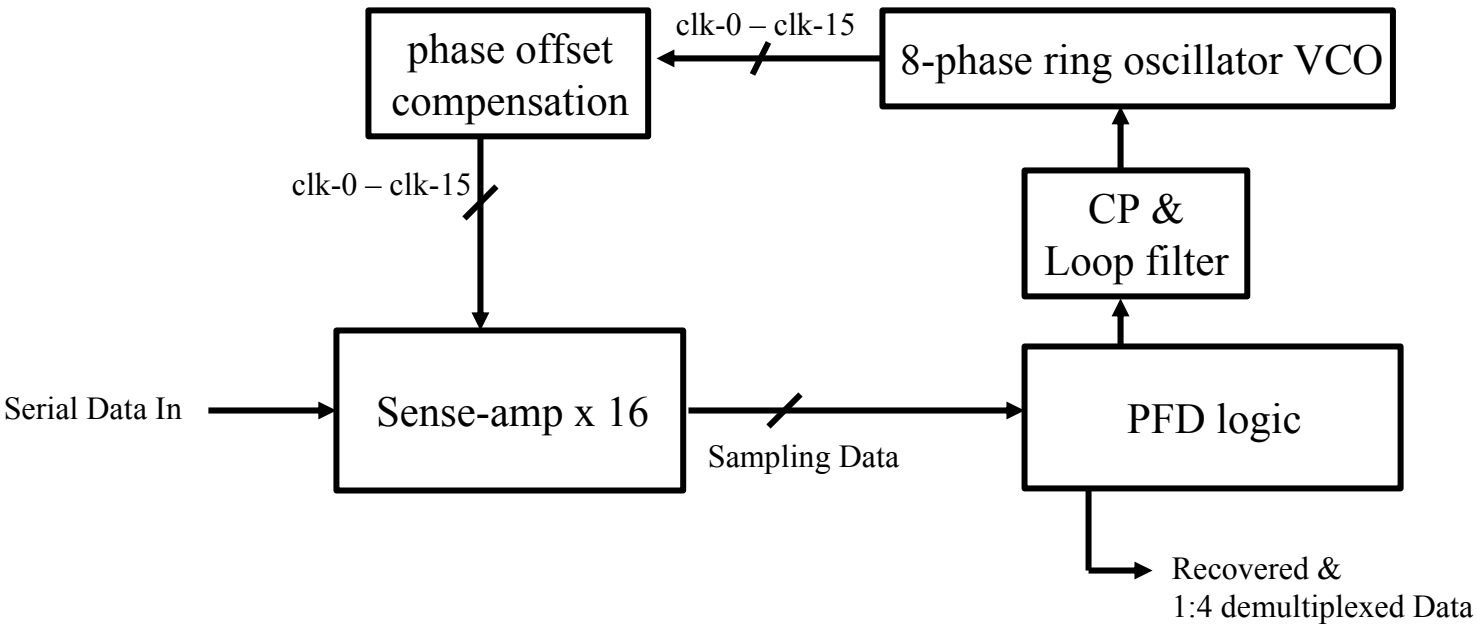
- Technology 0.18µm CMOS
- Active area
  - CDR 0.71 $mm^2$
  - Loop Filter 0.69 $mm^2$
- Power consumption 140 mW at 1.8 Vdd
- Data rate 2.41 - 2.72 Gbps
- Loop bandwidth 1.3 MHz.
- Pull-in range > 100 MHz.
- Jitter Performance

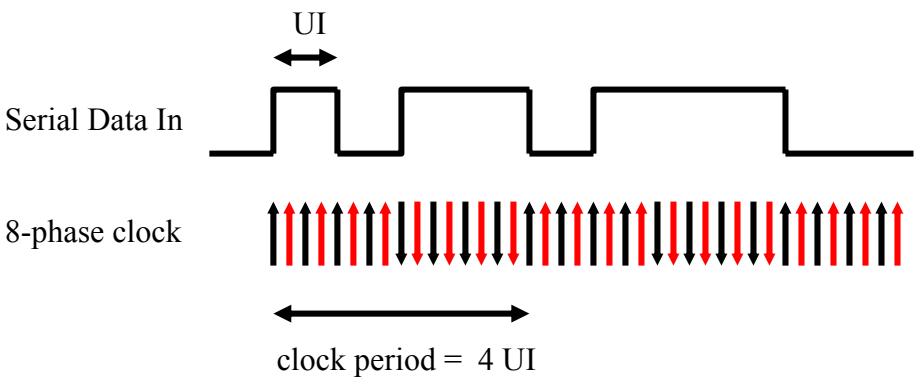
| Input Data | Output clock |
|---|---|
| ▪ 2.5 Gbps, PRBS $2^7$-1 | 2.3 ps, rms |
| ▪ 2.5 Gbps, jitter 280 ps, p-p (0.7UI), modulation at 10 MHz. | 5.9 ps, rms |

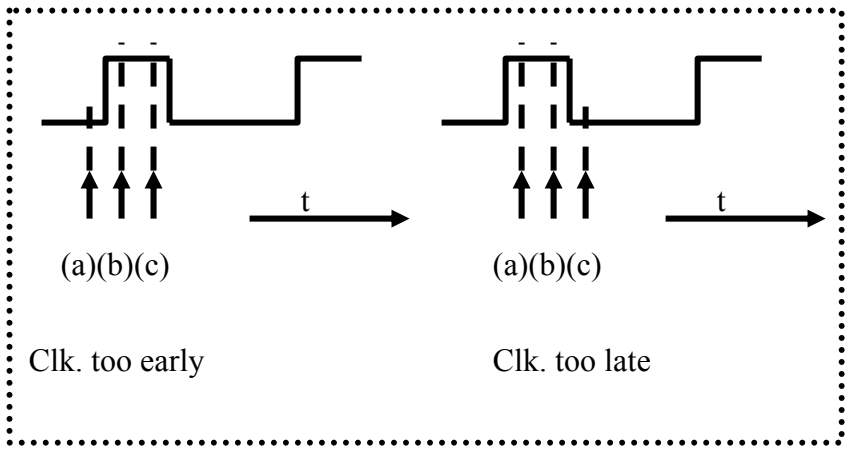



Recovered clock, 2.5 GHz.

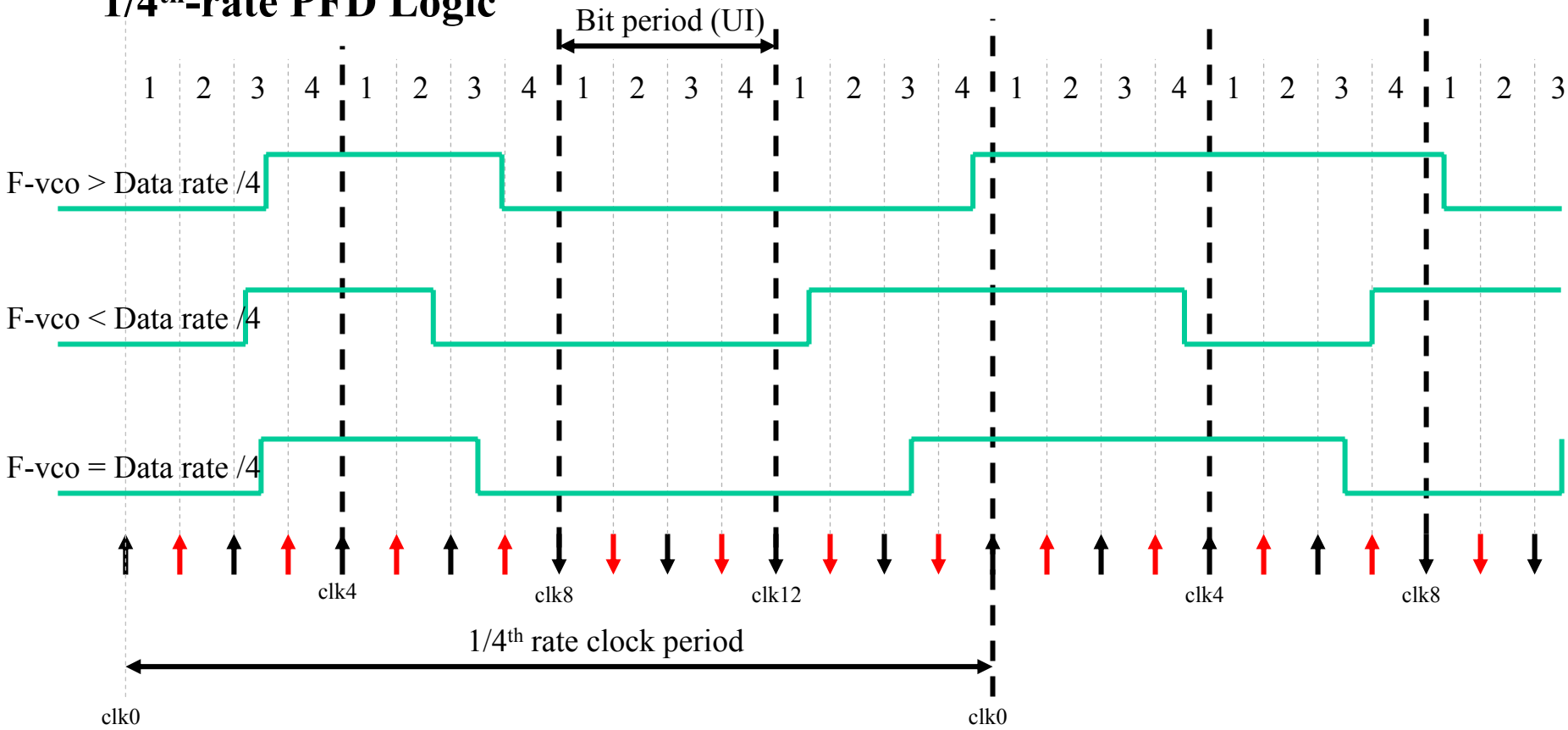
# Test structure CDR-3 "CDR using 1/4th-rate Quadricorrelator FD Structure"



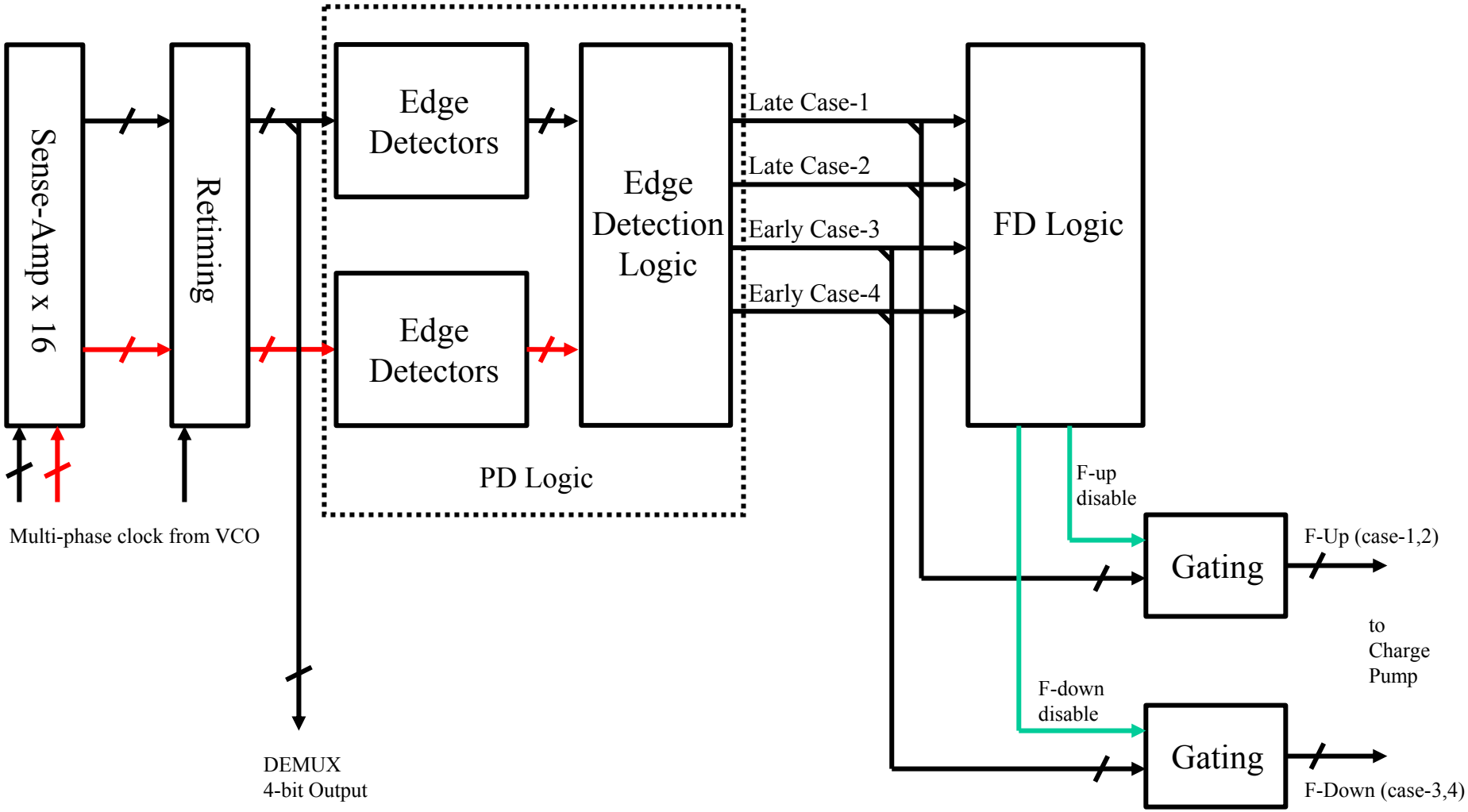



# 1/4th-rate PFD Logic

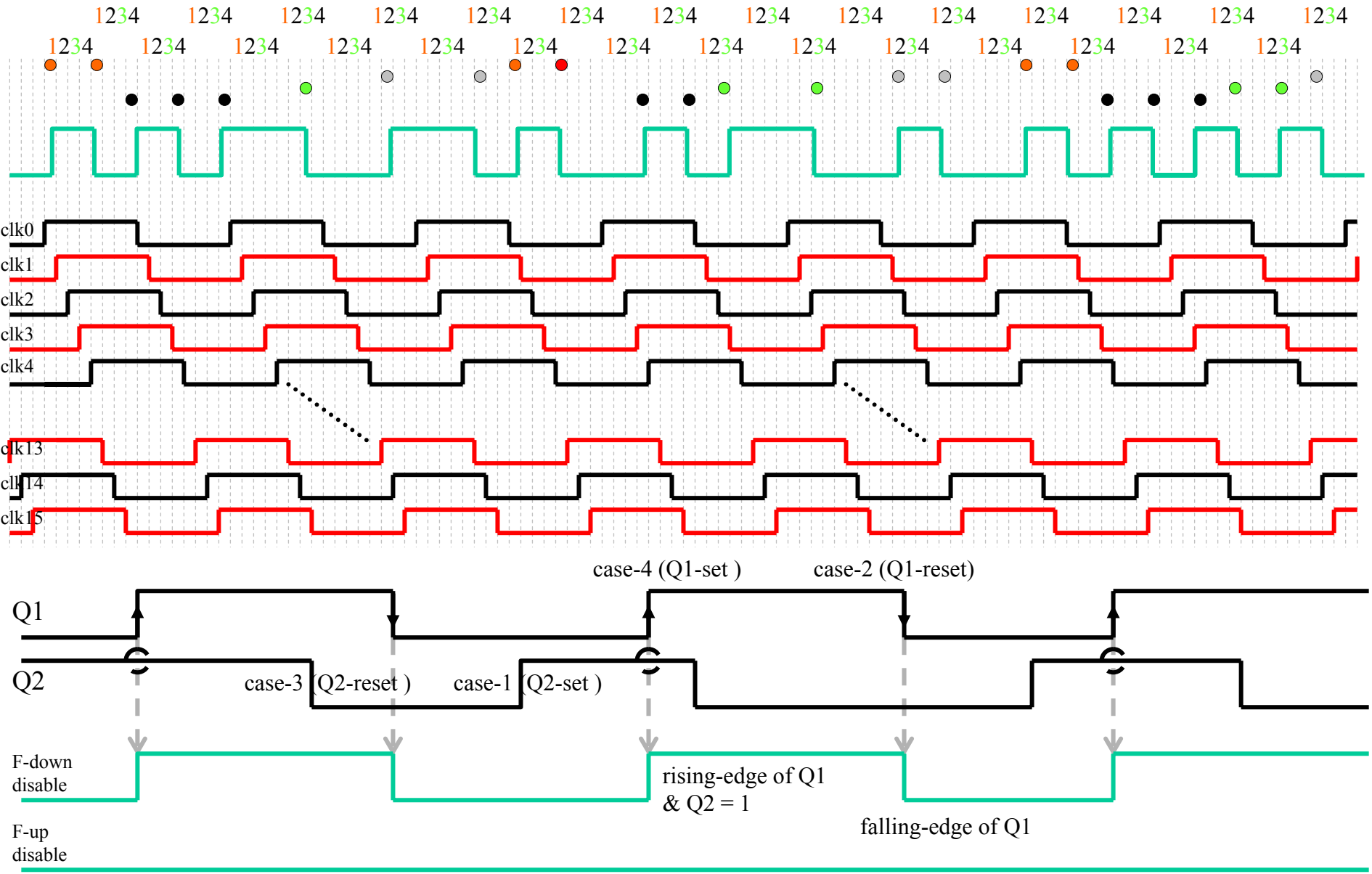



- F-VCO > Data rate /4, data transitions rotate from case-1 -> case-2 -> case-3 -> case-4.
- F-VCO < Data rate /4, data transitions rotate from case-1 -> case-4 -> case-3 -> case-2.
- In lock condition, clk-0 sampling at the middle of data-eye, edges of data are in case-2 or case-3.
    - PD generate “late” signal (f-up) for case-1 and case-2.
    - PD generate “early” signal (f-down) for case-3 and case-4.

# 1/4th-rate PFD Block Diagram

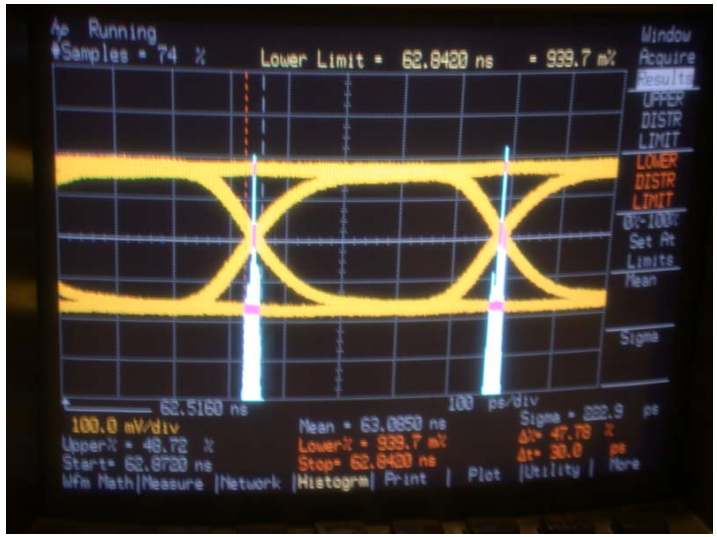


# FD Logic of CDR-3: F-VCO too low

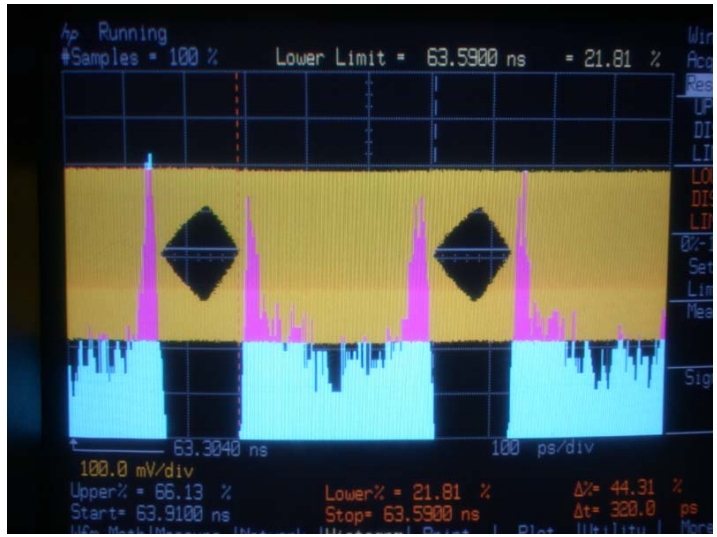


# Measurement results : CDR-3

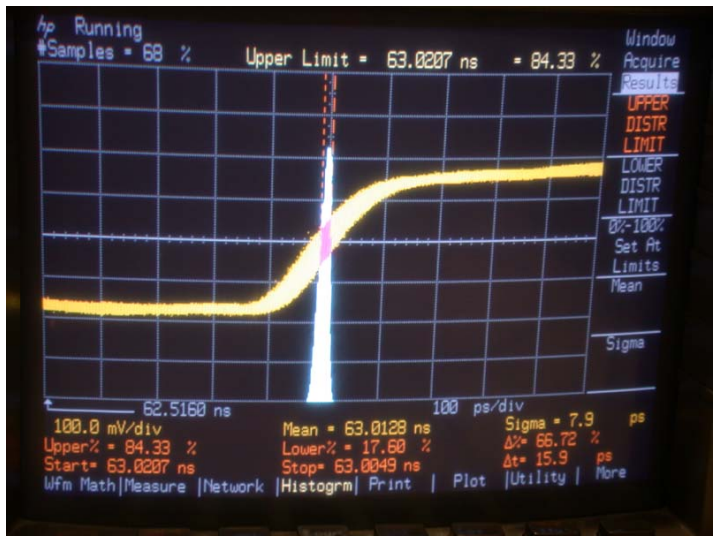
: Jitter Histogram at Incoming Serial Data 2.25 Gbps



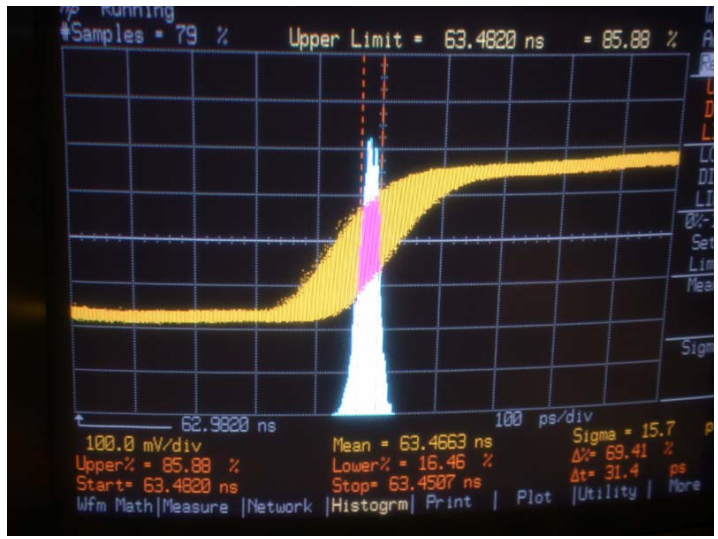

a) Incoming serial data in, jitter 6.6 ps, rms




c) Incoming serial data in, jitter,p-p 311ps (0.7 UI) at 10MHz.

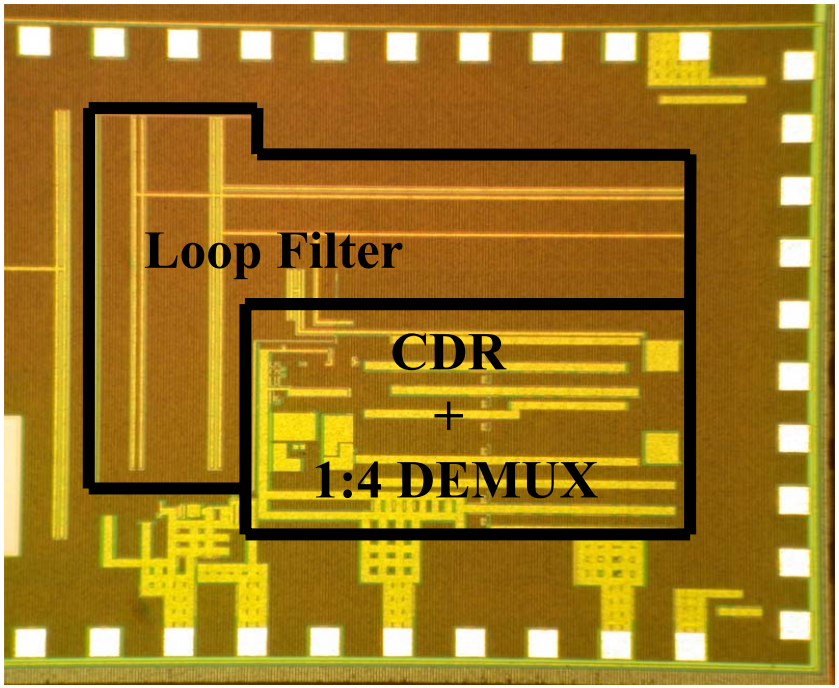



b) Corresponding recovered clock, jitter 7.9 ps, rms




d) Corresponding recovered clock, 15.7 ps, rms

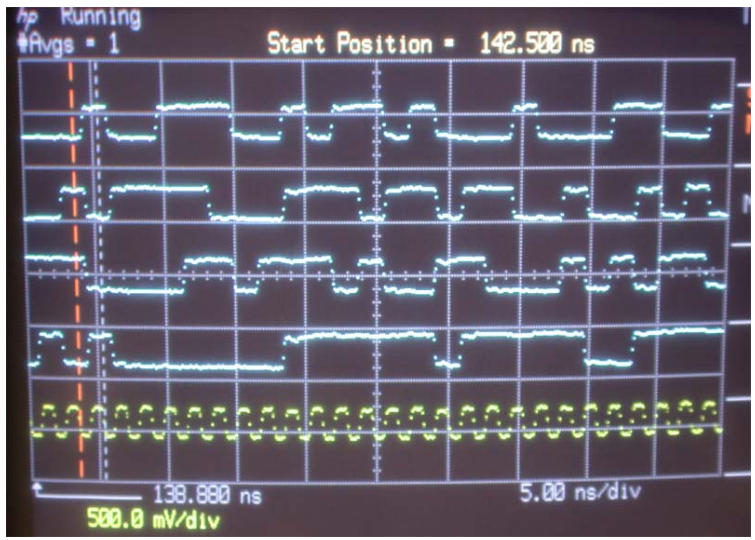
# Measurement results : CDR-3




Die Photograph

- Technology 0.18µm CMOS
- Active area
  - CDR + DEMUX 0.70 $mm^2$
  - Loop Filter 0.63 $mm^2$
- Power consumption 100 mW at 1.8 Vdd
- Data rate 1 - 2.27 Gbps
- Loop bandwidth 1MHz.
- Pull-in range > 100 MHz.
- jitter Performance

| Input Data | Output clock |
|---|---|
| ▪ 2.25 Gbps, PRBS $2^7$-1 | 7.9 ps, rms |
| ▪ 2.25 Gbps, jitter 311 ps, p-p (0.7UI), modulation at 10 MHz. | 15.7 ps, rms |



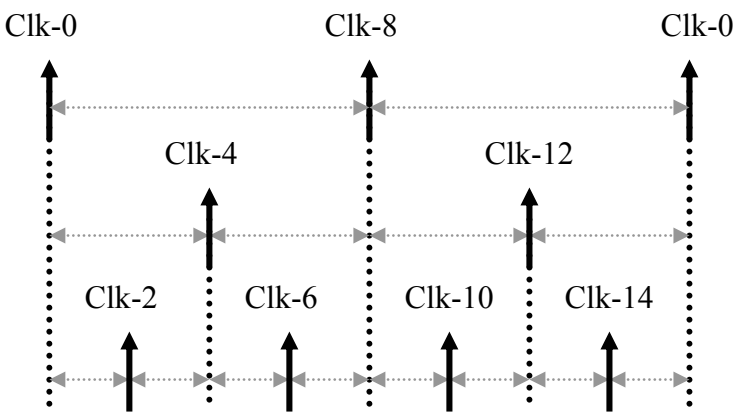

Deserializer Outputs at 562.5 MHz. (2.25 Gbps)

# Conclusions

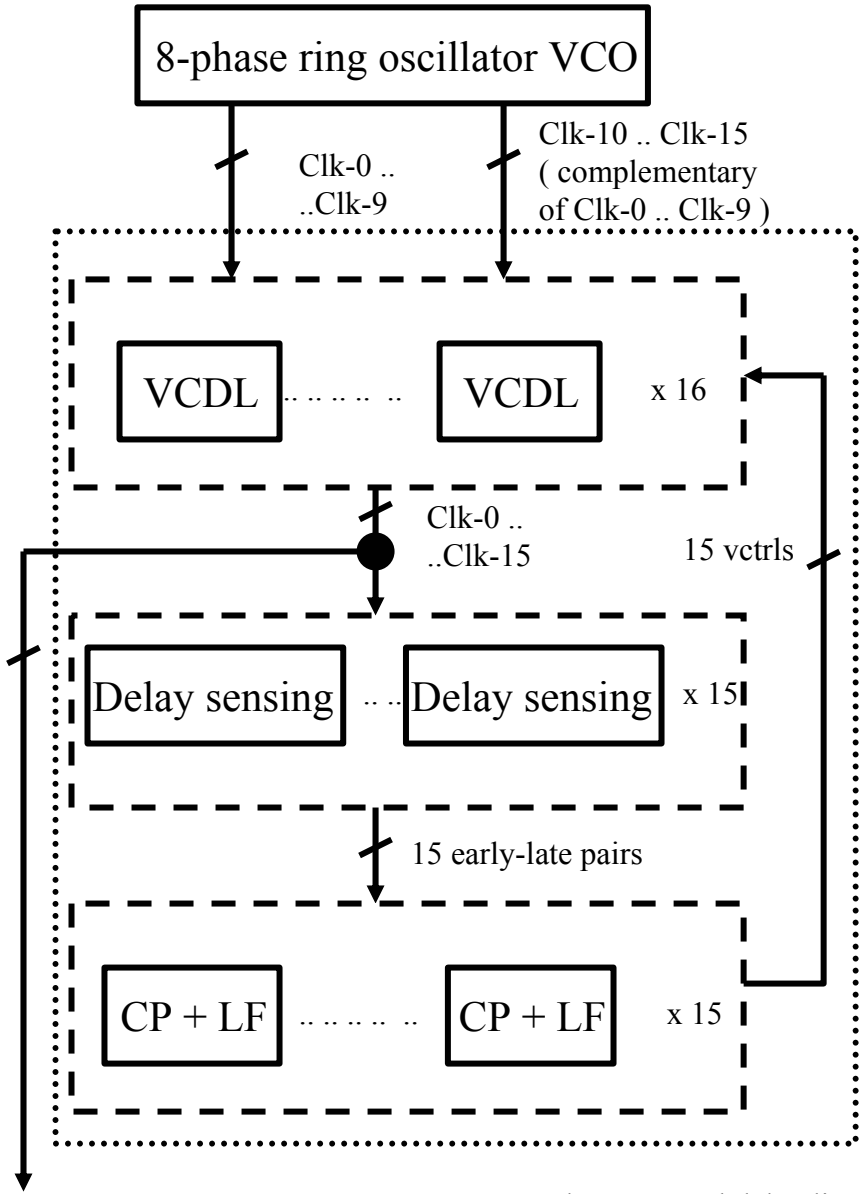
- CDR with Frequency Detector
  - can operate without the need for a local reference clock.
  - low jitter operation and wide pull-in range can be achieved.
- Full-rate CDR architecture,
  - suitable for LC-VCO, very low jitter.
  - phase frequency detector is implemented in CML.
- 1/4$^{th}$-rate CDR architecture,
  - lower operation frequency, suitable for ring-based oscillator.
  - all logic units can be implemented by CMOS logic, low power.
  - intrinsic 1- to - 4 DEMUX.
  - phase offsets of VCO can be reduced by layout techniques and skew calibration scheme.

- The tested CDRs implemented on 0.18μm CMOS Technology has low jitter operation.

# Skew Calibration Scheme




Phase control hierarchy




VCDL = voltage control delay line

Ref: Lin Wu, William C. Black Jr., A Low Jitter Skew-Calibrated Multi-Phase Clock Generator for Time-Interleaved Applications, ISSCC 2001, pp396 – 397.