State of the Art of CMOS Sensors for Charged Particle Tracking : On Pixel Signal Processing and On Chip Readout Architectures.

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On behalf of

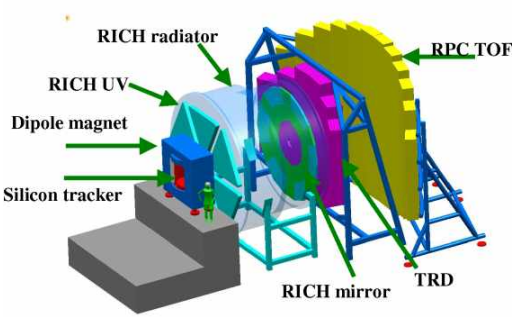
(and DAPNIA / SACLAY / for the MIMOSA-8 prototype)

Outline

- **Vertex detector requirements**
- **The operation principle of CMOS-sensors**
- **Fast readout architectures**
  - Development guide lines
  - Pixel layouts including CDS
  - Recent results
- **Recent results on radiation tolerance**
- **Conclusion and outlooks**

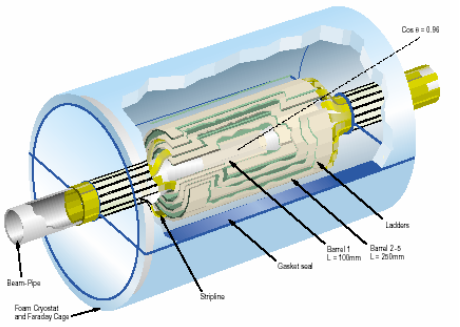
Vertex detector requirements

CMOS sensors are developped for several futur vertex detectors :



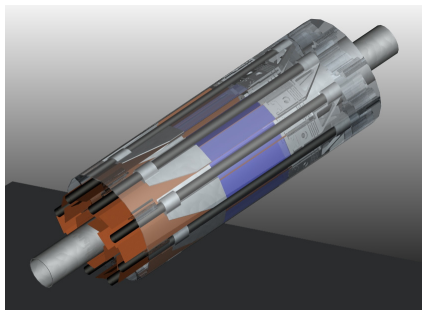
CBM ~2015

- Radiation dose : O(10) MRad/cm^2/year
- Granularity : ~30 μm
- Readout speed : <10 μs



International Linear Collider ~2015

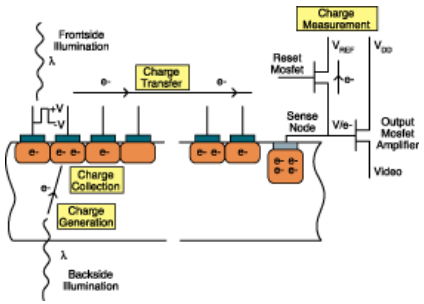
- Radiation dose : <100 kRad/cm^2/year
- Granularity : ~20 μm
- Readout speed : 25 μs

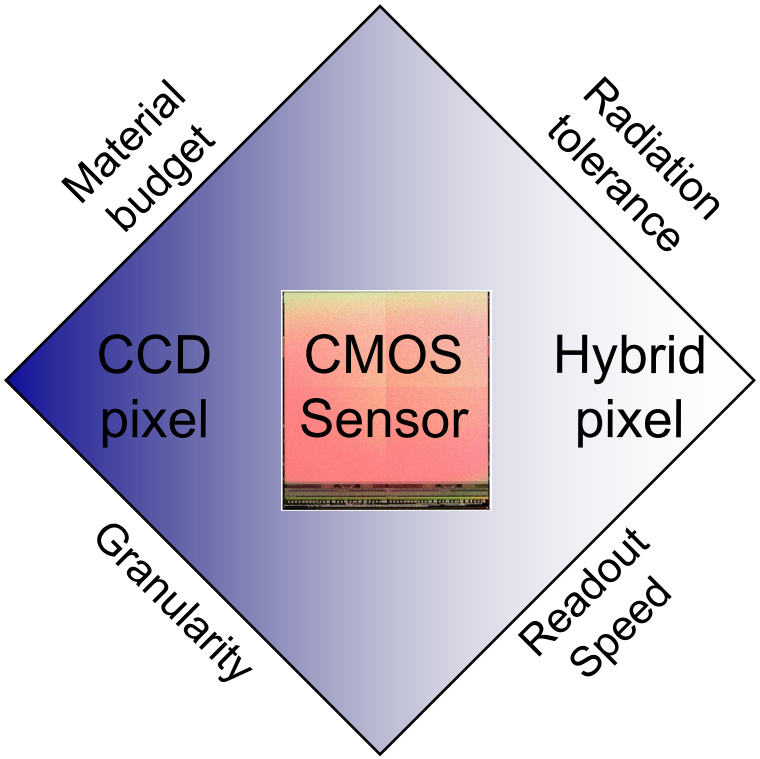


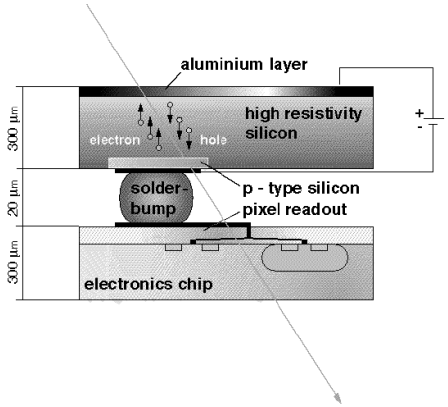
STAR Upgrade ~2011

- Radiation dose : <100 kRad/cm^2/year
- Granularity : ~30 μm
- Integration time : <200 μs

CMOS sensor advantages for vertexing

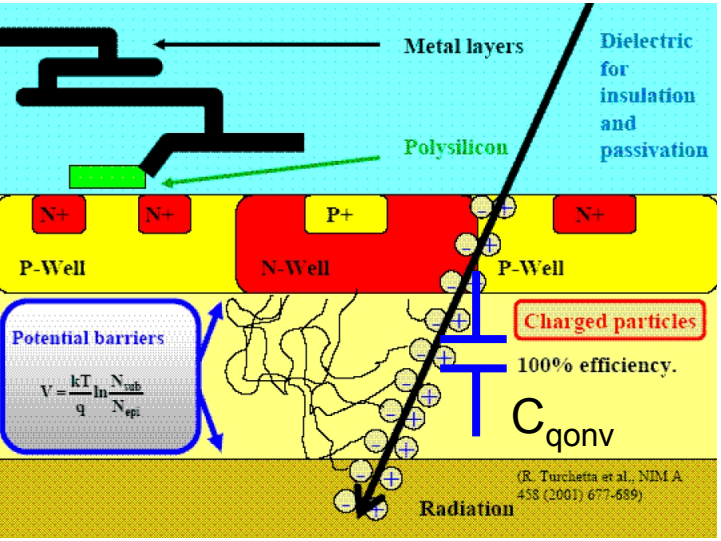


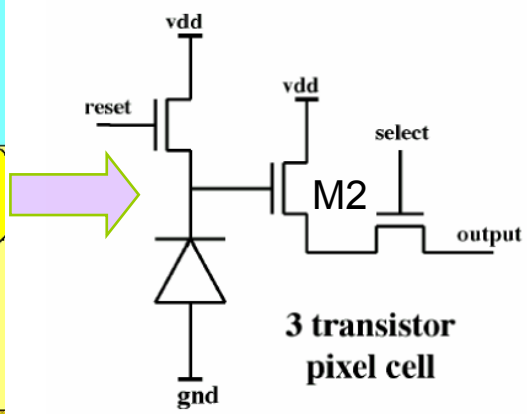


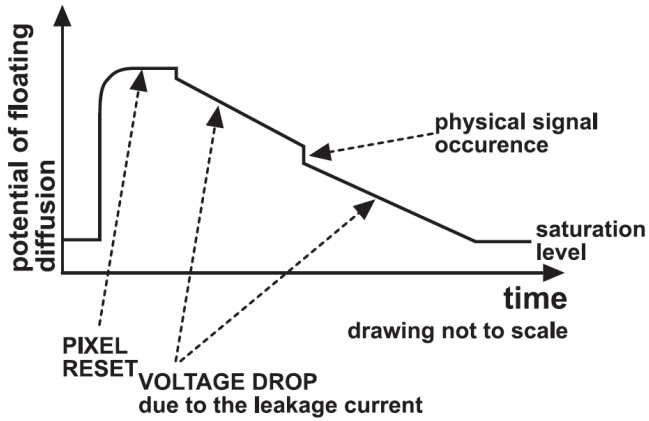


- **Excellent m.i.p. detection performances (120 GeV π^- at CERN – SPS) :**
  - > 99% m.i.p. detection efficiency, (ENC ~10 e-, S/N = 15-30)
  - High single point resolution : 1.5~2 µm
  - Radiation tolerance : ~10^{12} neq/cm^2 & several MRad
  - Material budget (thin sensitive volume : ~ 10µm) : 50 µm thickness achieved with reticle size sensors (1Mpix, around 4cm^2)

Principle of operation of CMOS sensors







$$G_{q\to v,sf} = \frac{g_{m,\,M2}}{g_{m,\,M2} + g_{m,\,M2}} \cdot \frac{1}{q \cdot C_{qonv}}$$

$$G_{q\to V}\left[\mu V / e^{-}\right]$$

- Simple 3 transistors structure established for many applications
- Thin ~undepleted epitaxial layer = active volume (~10 µm), liberated Charge ~80e-/µm/m.i.p.
- Charge collected by deep n-well/p-epi diode (~10µV/e- process dependent)
- Only NMOS T. can be integrated inside pixels
- Charges collected through thermal diffusion with collection time : up to ~100ns
- Signal delivered contains : Fixed Pattern Noise, KT/C Noise and electronic noise (thermal, 1/f, shot)

Fast readout general arguments

Readout today:

- Serial analog mode
- External 12-bit ADC
- Cluster finding and discrimination on PC
- Efficient but very slow

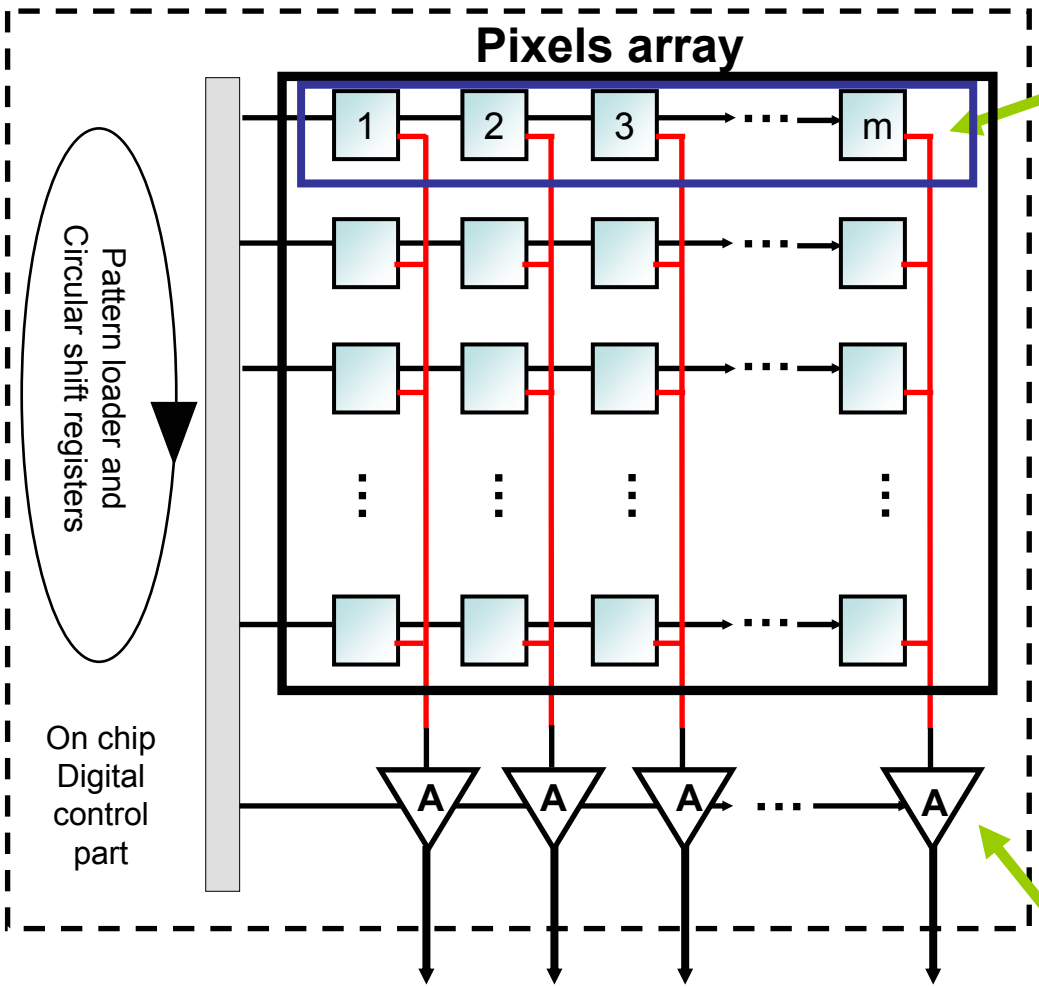
Proposed readout mode for CBM:

- Massive column parallel readout

Consequences:

- Parallel readout produces ~10^9 analog samples /s/cm²
- Transfer to external ADCs is not possible
- Discrimination and data sparsification has to be done on the chip itself.

CMOS sensor architecture



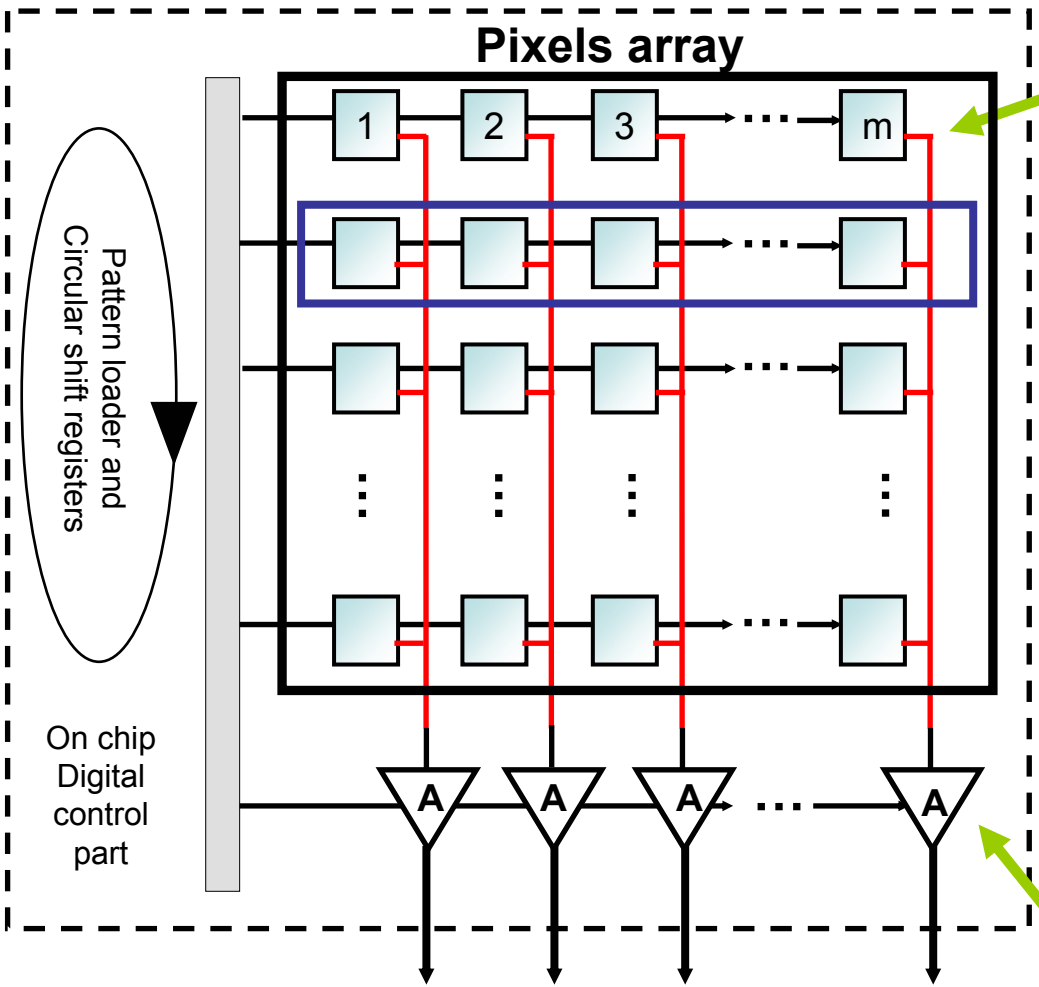
pixel

- 1 common readout line per column
- Circular readout of each row
- Power consumption

  Goal : <1mW per column

On chip signal processing : amplifier, ADC

CMOS sensor architecture



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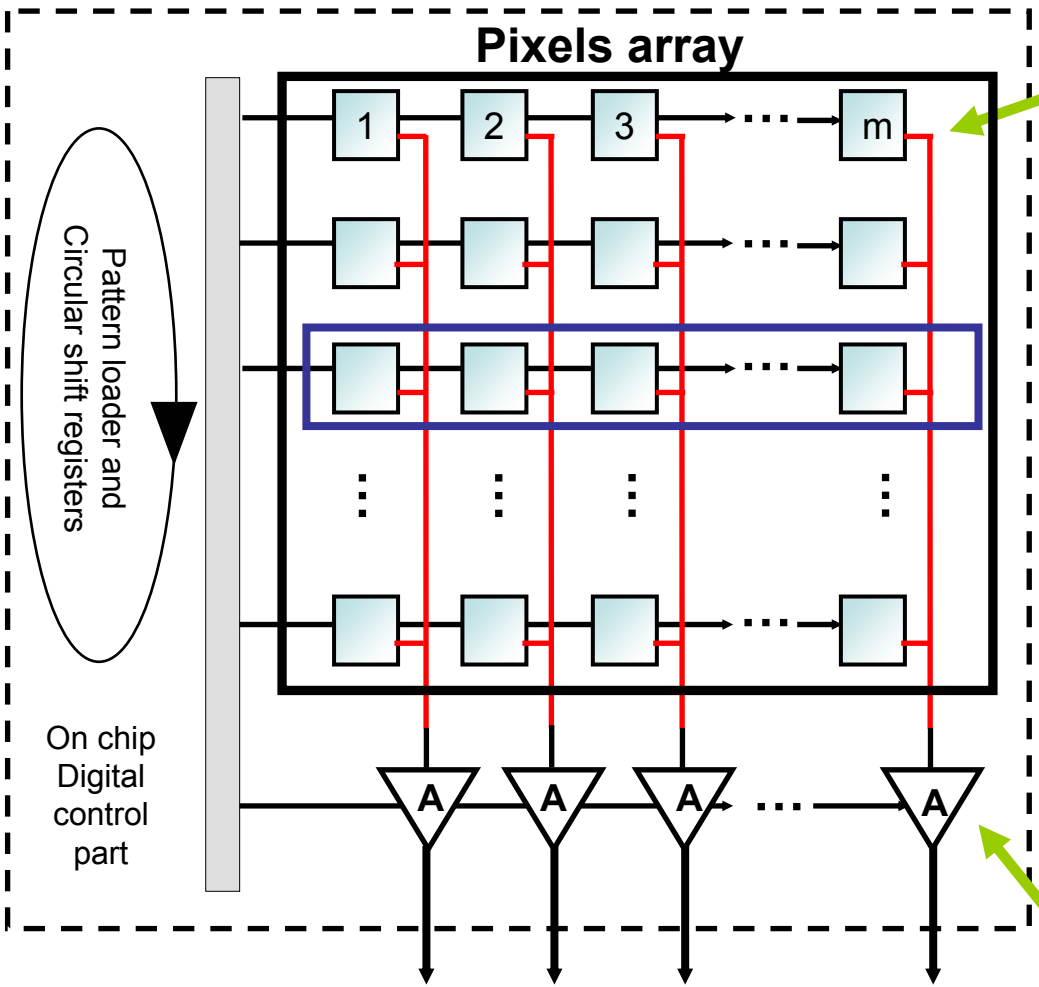
CMOS sensor architecture



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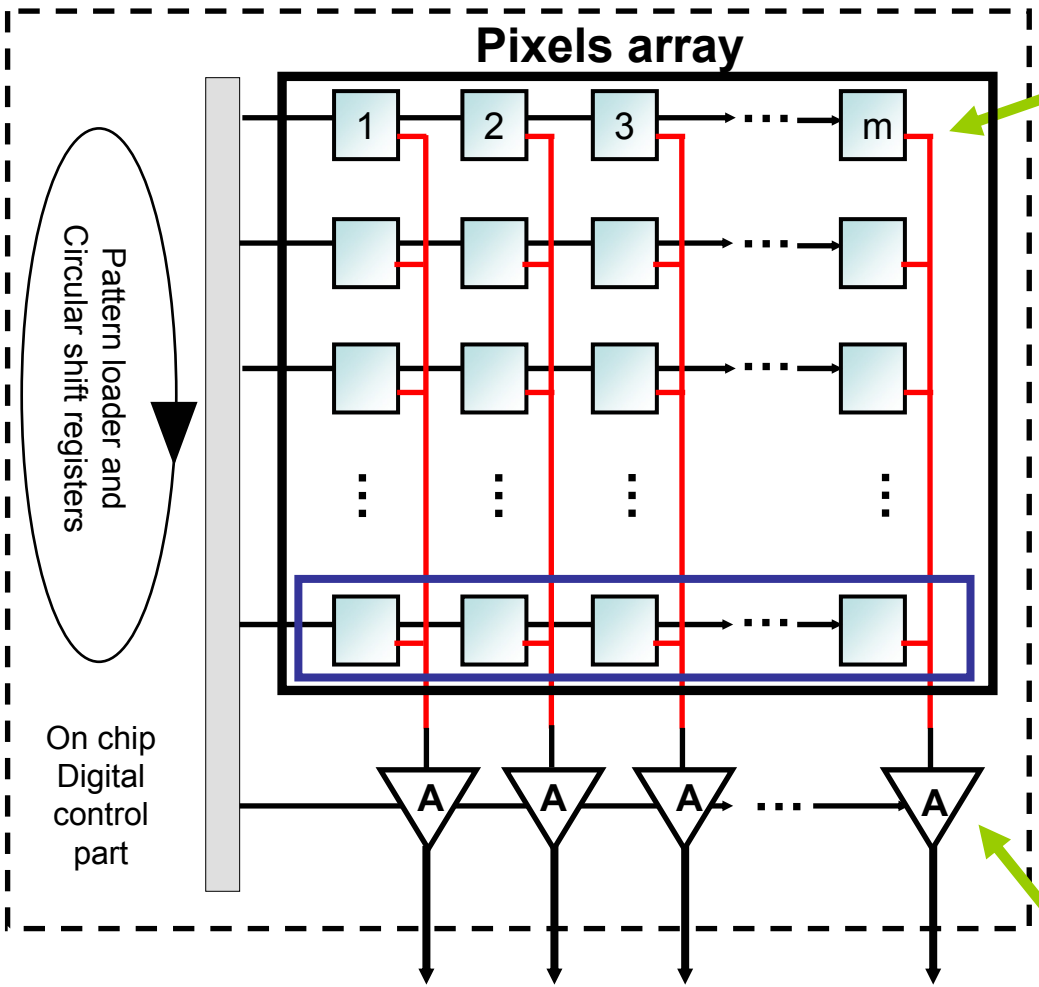


pixel

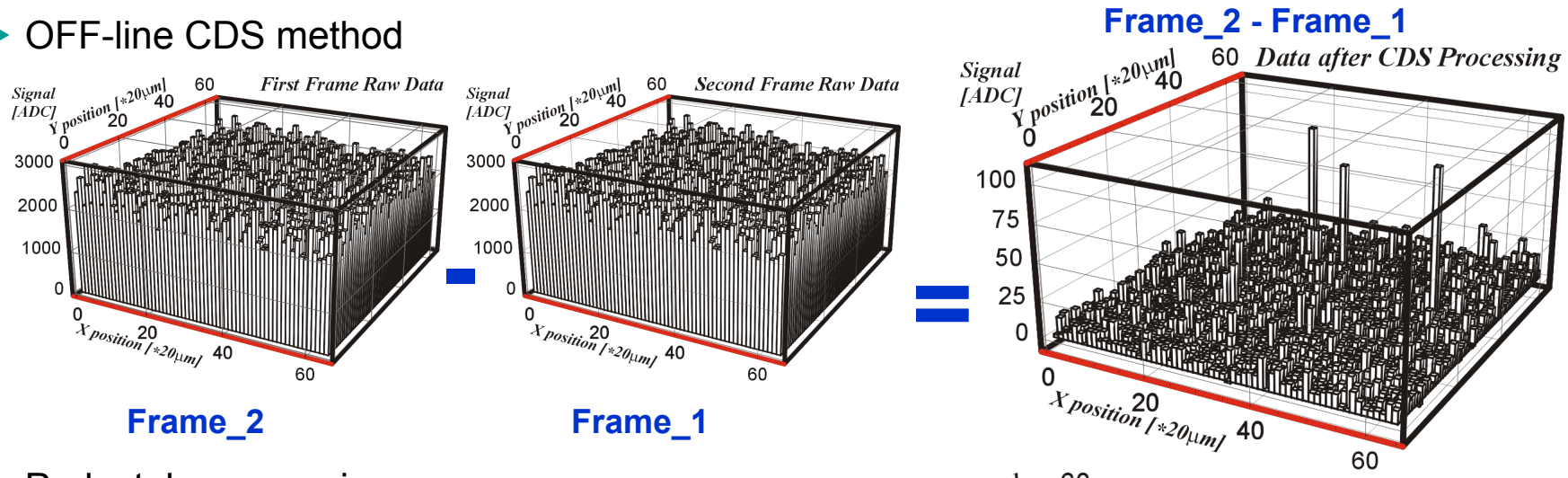
- 1 common readout line per column
- Circular readout of each row
- Power consumption

  Goal : <1mW per column

On chip signal processing : amplifier, ADC

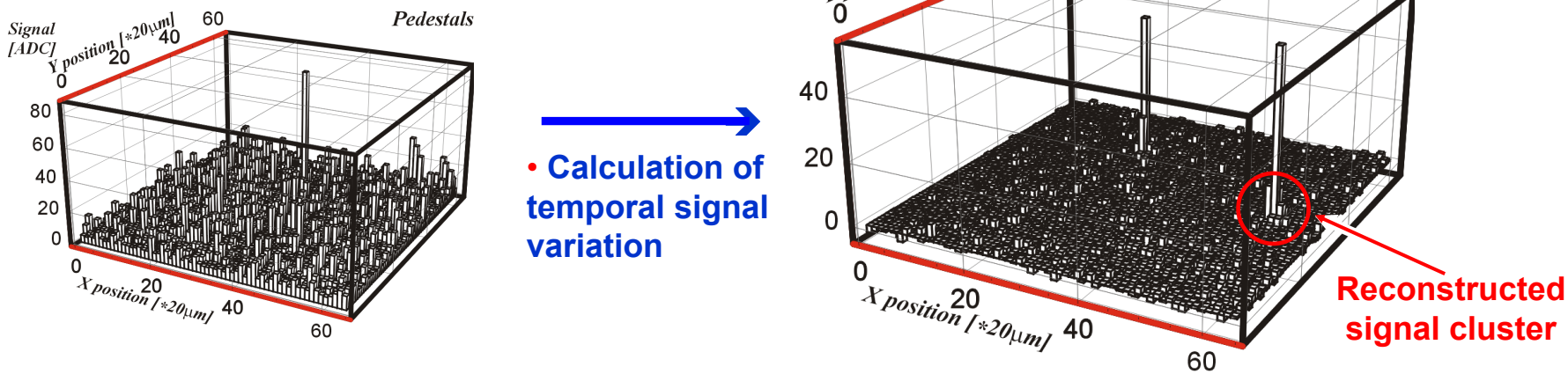
CDS and pedestal correction (so far on PC)

- OFF-line CDS method



- Pedestal suppression

CDS pedestals=integrated leakage current



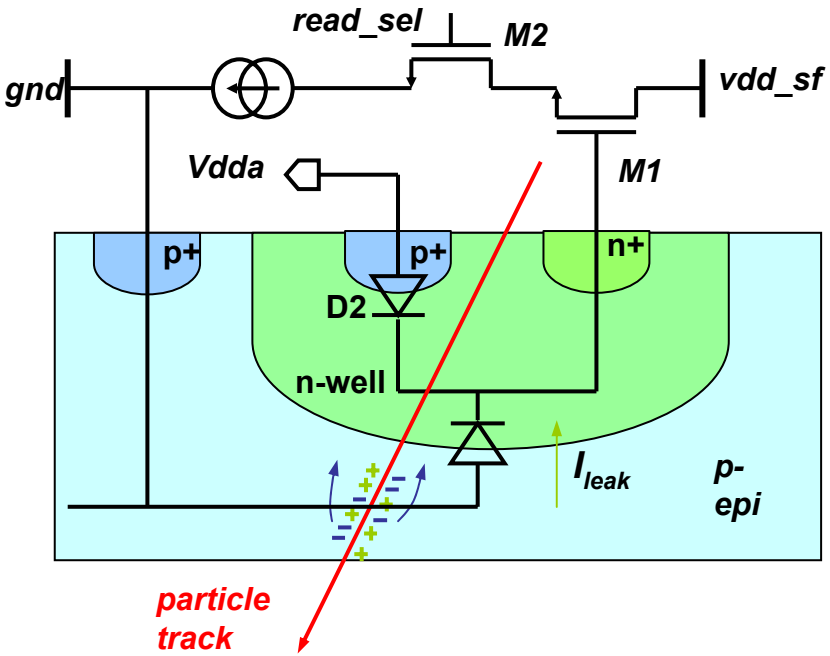
- GOAL : **integrate this signal processing in the sensor**

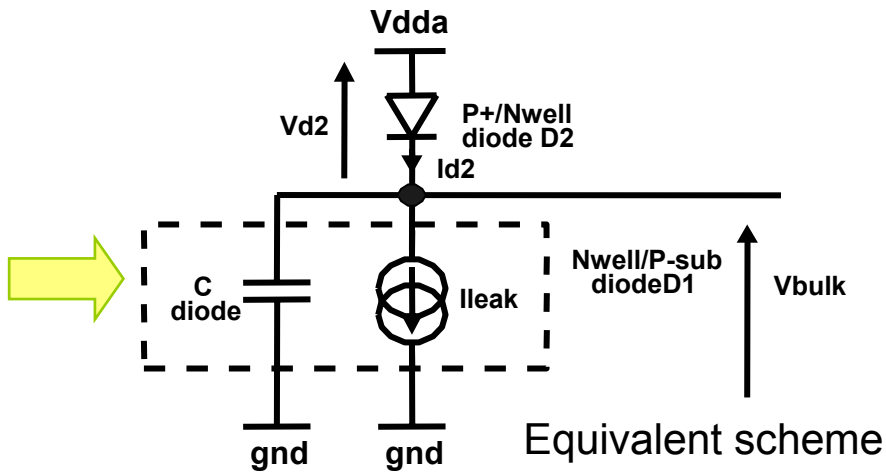
Fast readout general arguments

Requirements for on chip data sparsification:

- **Discrimination has to be done by one discriminator (or ADC) per column.**
- **Advanced signal processing has to be done inside the pixel**
  - Leakage current compensation
  - CDS processing (needs additional amplification)
  - Pedestal correction
- **High pixel to pixel uniformity is required**
  - Compensate production tolerances of CMOS

Self bias pixel (pixel with leakage current compensation)



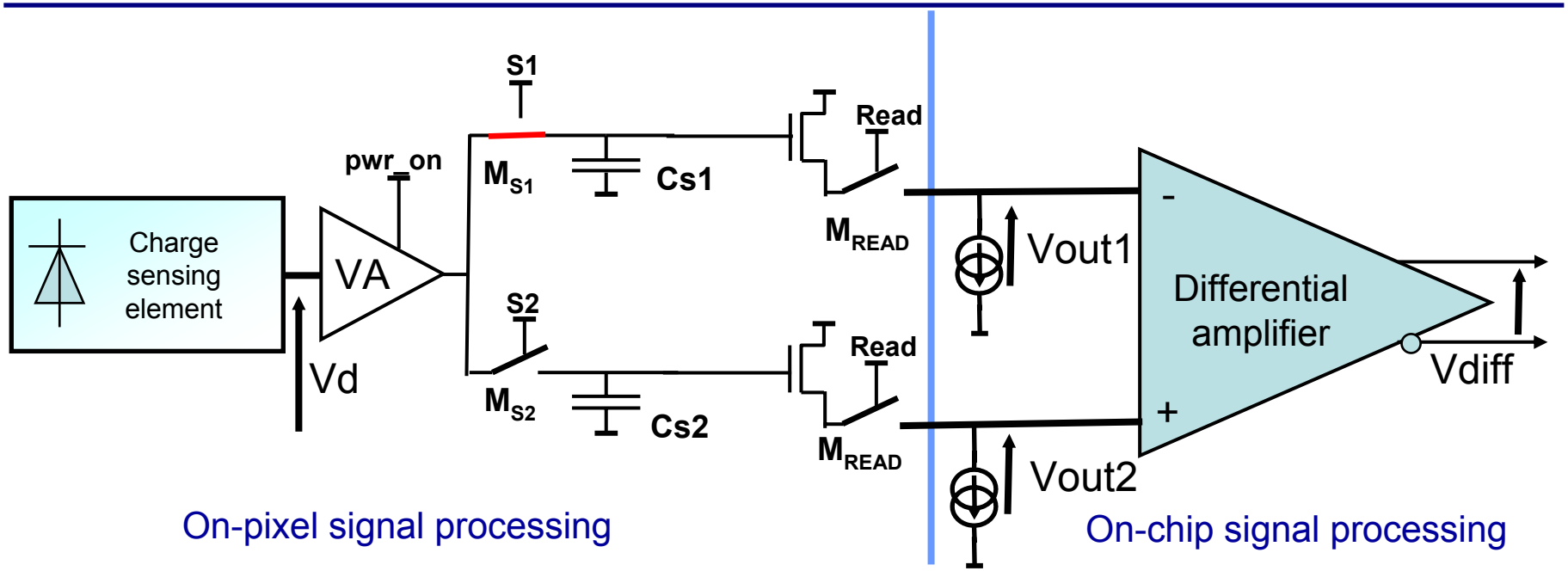


$$Ileak = Id2 = Is \cdot \left[\left(\exp\left(\frac{Vd2}{ut} \right) \right) - 1 \right]$$

$$Vbulk_{(DC)} = Vdda - Vt \cdot \ln\left(\frac{Ileak + Is}{Is} \right)$$

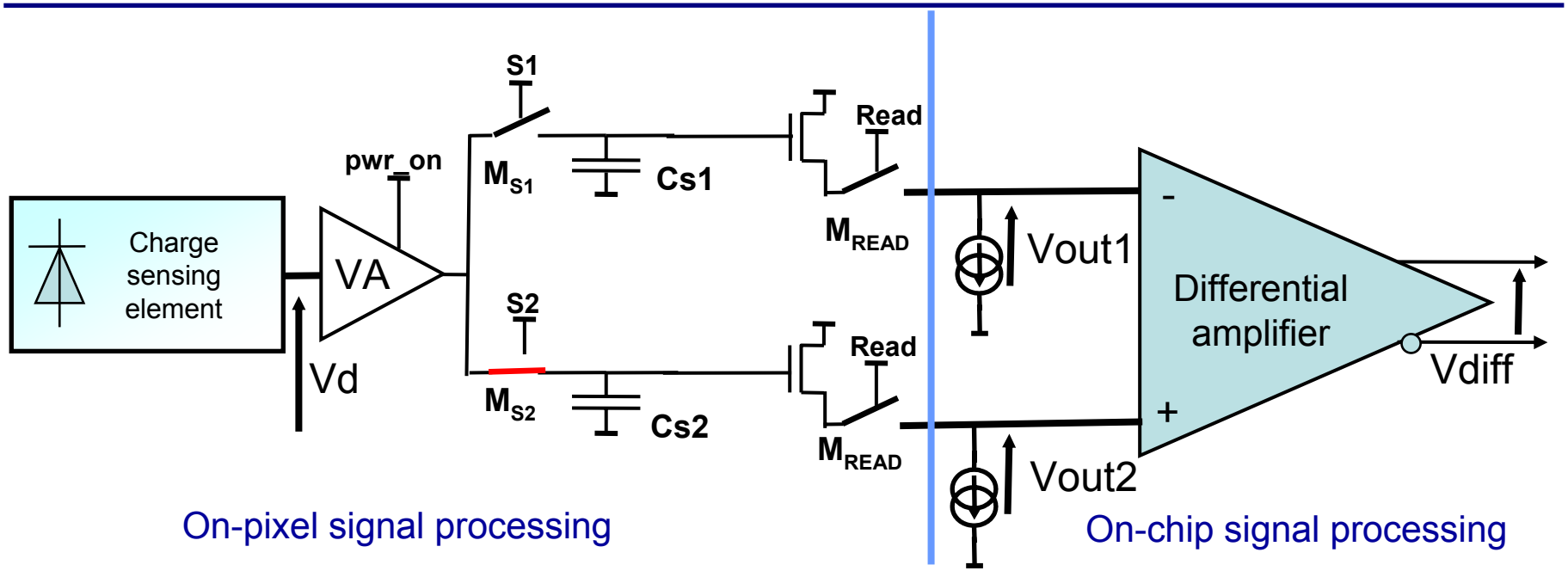
- Preserve charge integration : ~10μV/e-
- Self-reverse bias of charge collecting diode
- In darkness, the diodes D2 conveys only a small value leakage current, thus it represents very high value resistance (10^9-10^{12} Ohm)
- Recovering time after a hit : 50 - 100 ms
- Excellent performance : noise ~10 e-

On-pixel double sample processing



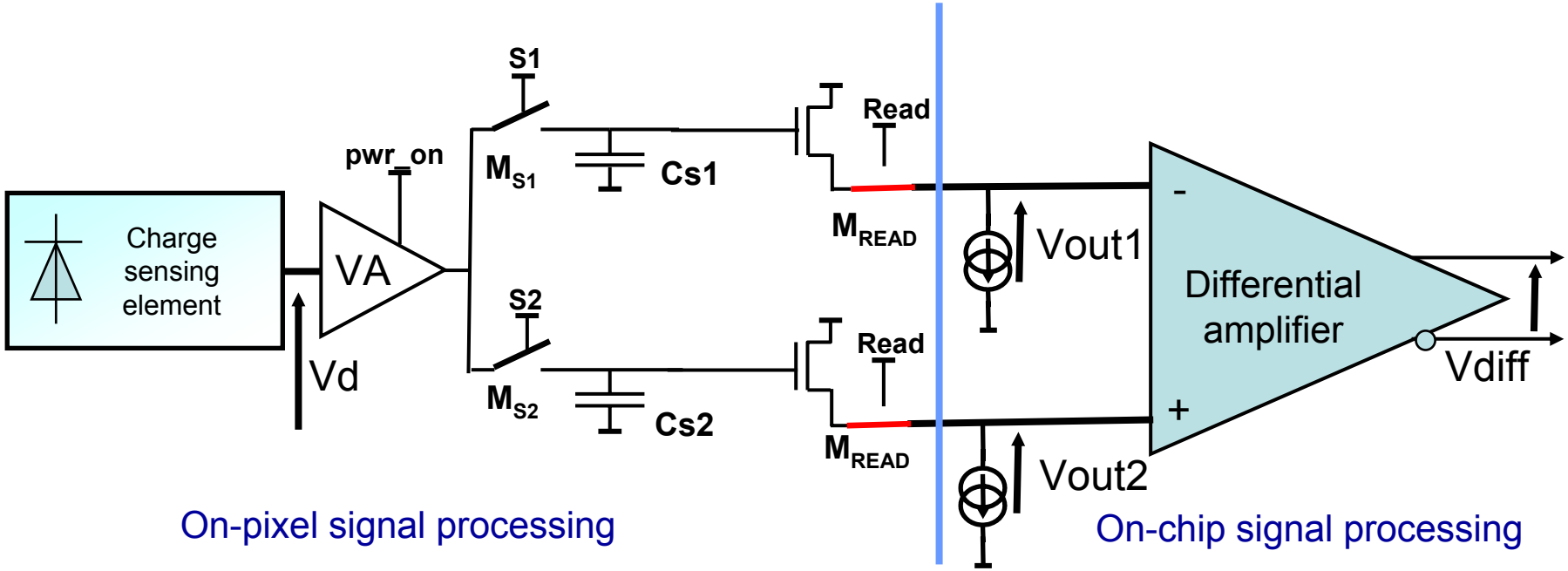
- Step 1 : transistor M_{S1} is closed, store charges information on Cs1

On-pixel double sample processing



- Step 1 : transistor M_{S1} is closed, store charges information on Cs1
- Step 2 : transistor M_{S2} is closed, store charges information on Cs2

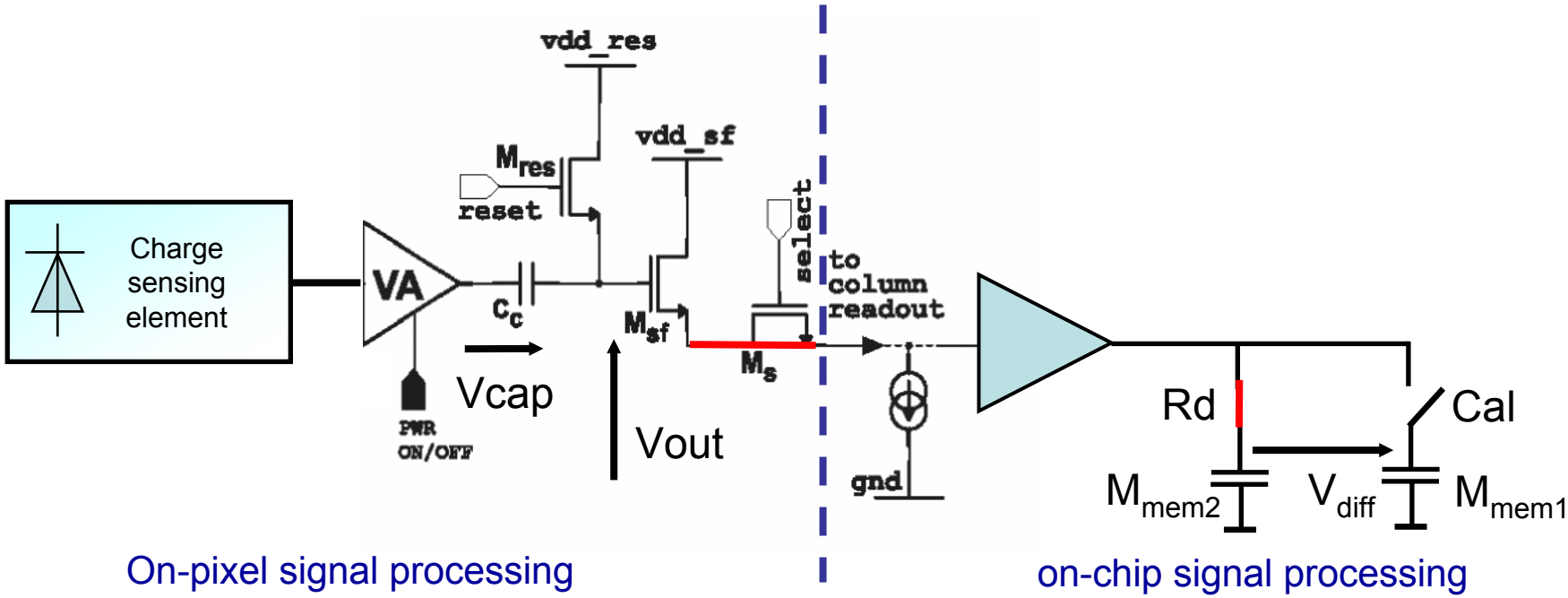
On-pixel double sample processing



- Step 1 : transistor M_{S1} is closed, store charges information on Cs1
- Step 2 : transistor M_{S2} is closed, store charges information on Cs2
- Step 3 : transistors M_{READ} are closed, readout voltage (Vout1) and (Vout2), the subtraction realized by differential amplifier => DS, Vdiff = Vout2 - Vout1
- Results : pixel is working but ~ 5mV residual offset after “CDS” as compared to 35 mV signal. High symmetry is required =>difficult due to production tolerances.

Next trial : clamping (MIMOSA8) in collaboration with DAPNIA / Saclay

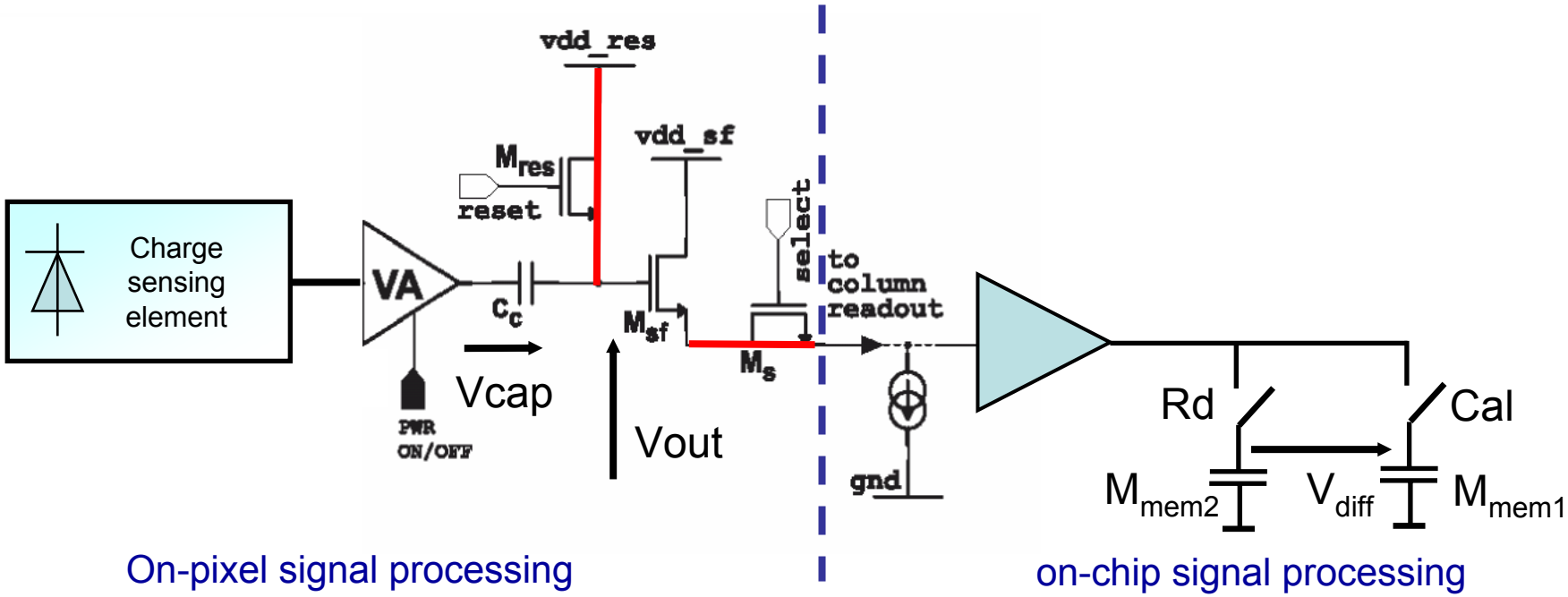
After integration time : A signal is stored in the charge sensing element



- **1st step**
  - Readout the signal and store it to the RD-memory cell

Next trial : clamping (MIMOSA8) in collaboration with DAPNIA / Saclay

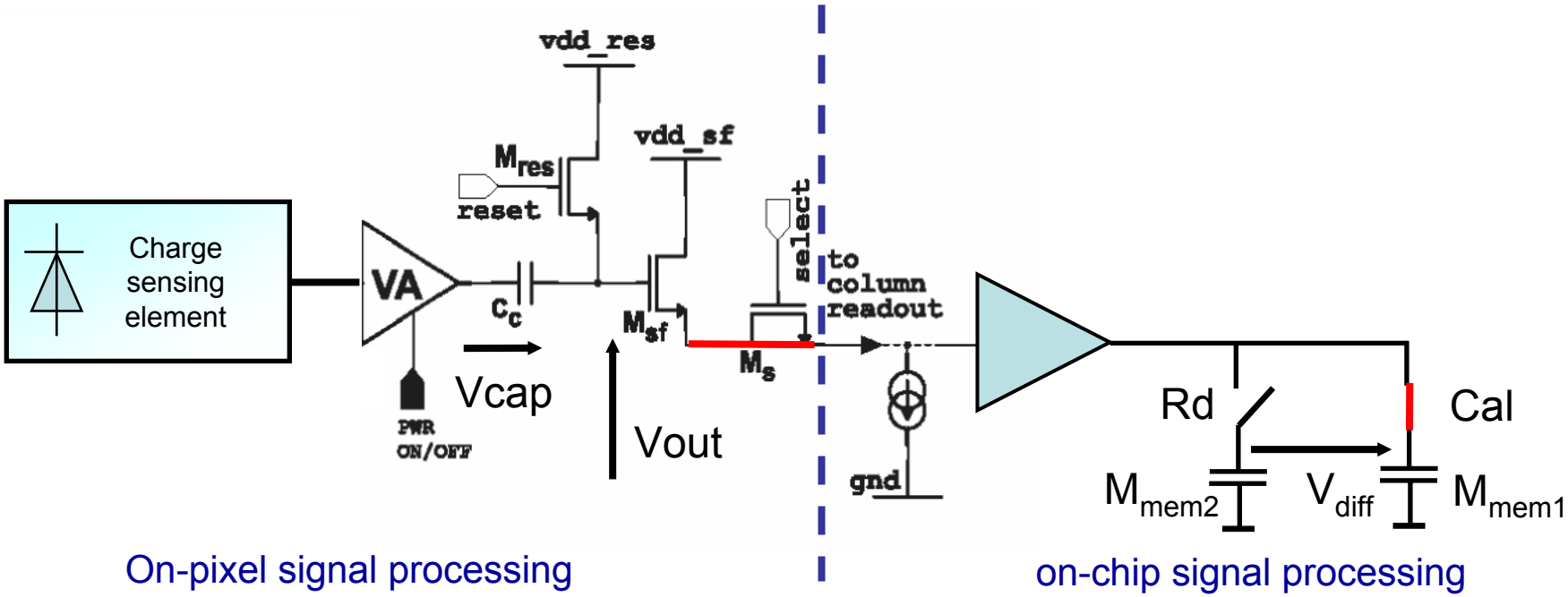
Problem now: How to get the reference for CDS



- **2sd step**
  - Reset the clamping structure

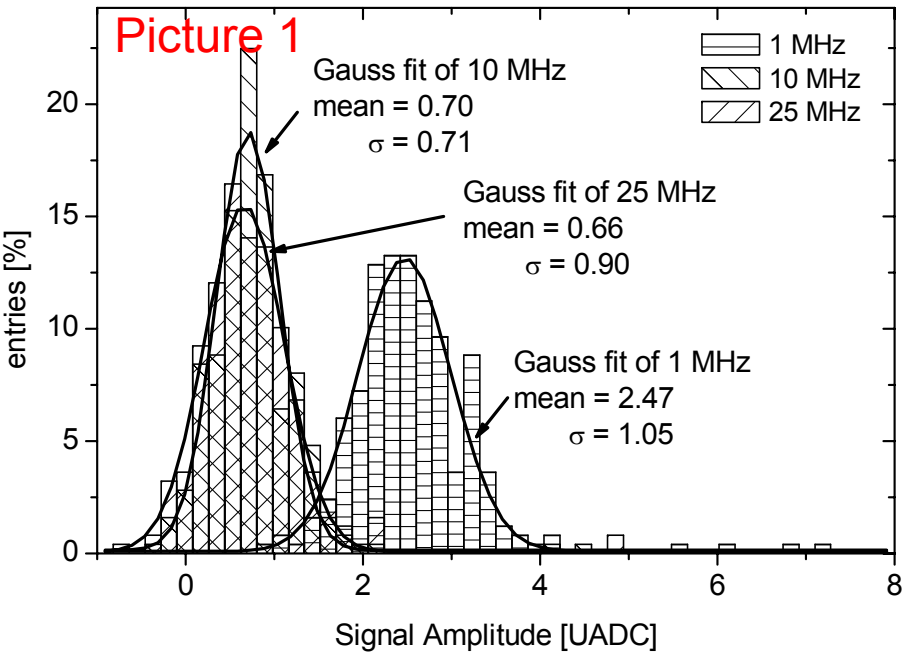
Next trial : clamping (MIMOSA8) in collaboration with DAPNIA / Saclay

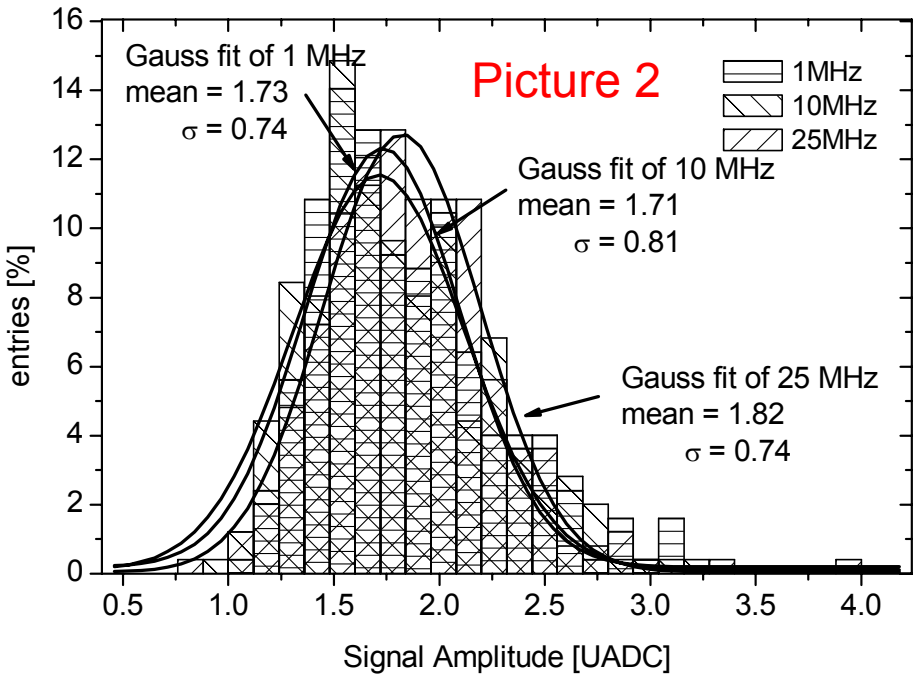
Problem now: How to get the reference for CDS



- **3rd step**
  - Readout the value after reset as a reference
- **4th step**
  - Subtract Cal and Rd to perform CDS.

Next trial : clamping (MIMOSA8) in collaboration with DAPNIA / Saclay



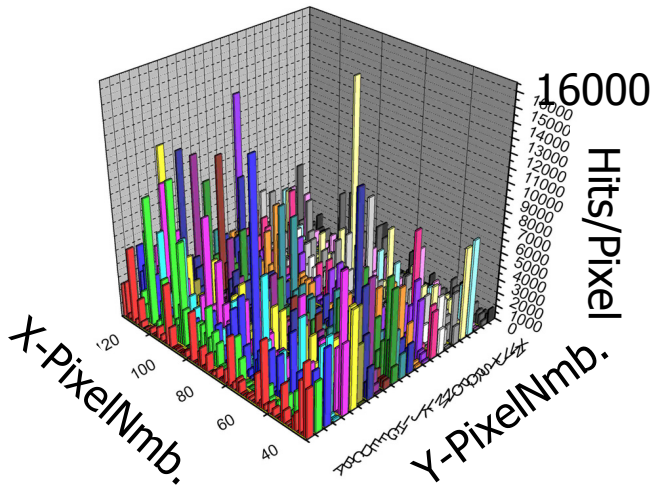


- **Picture 1 (FPN : pixel-to-pixel dispersion) :**
  - For a low frequency readout speed the offset is around 2.5 ADC counts (1.25 mV rms).
  - For a high frequency readout speed the offset is around 0.7 ADC counts (0.35 mV rms).
- **Picture 2 (temporal Noise) :**
  - Noise distribution of the MIMOSA 8 chip is 1.82 ADC count (0.9 mV rms), (ENC : ~20 e -).
- **Prototype test results** : <1mV residual offset, similar to signal noise level

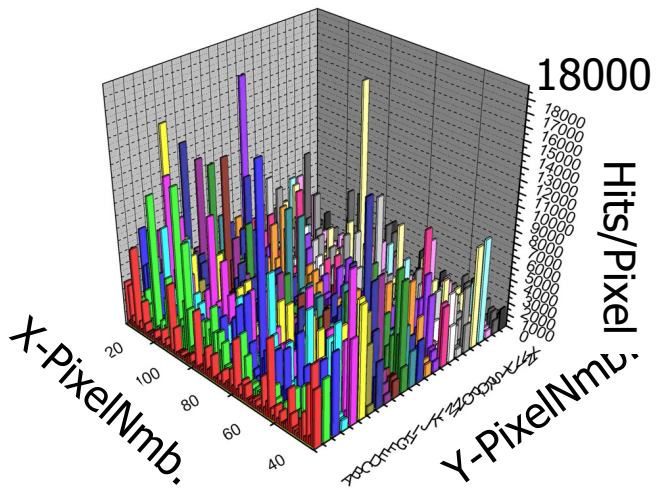
Testing the integrated discriminator (MIMOSA8)

100kEvents

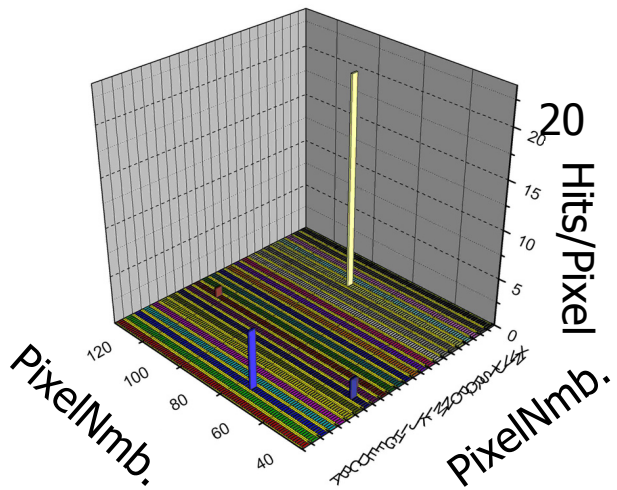
Without ^{55}Fe source

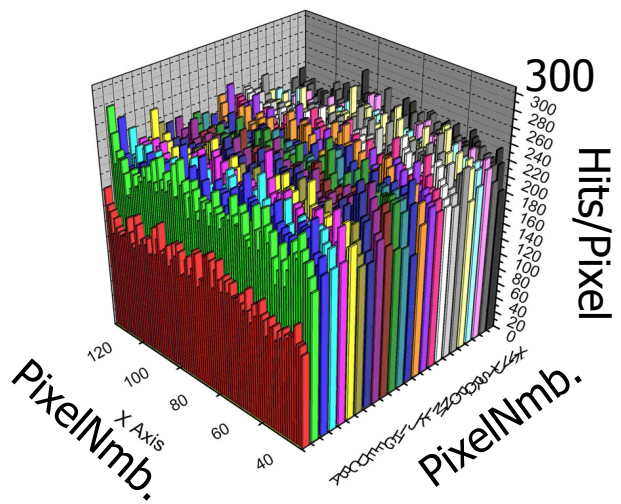


With ^{55}Fe source



V_{th}=5mV



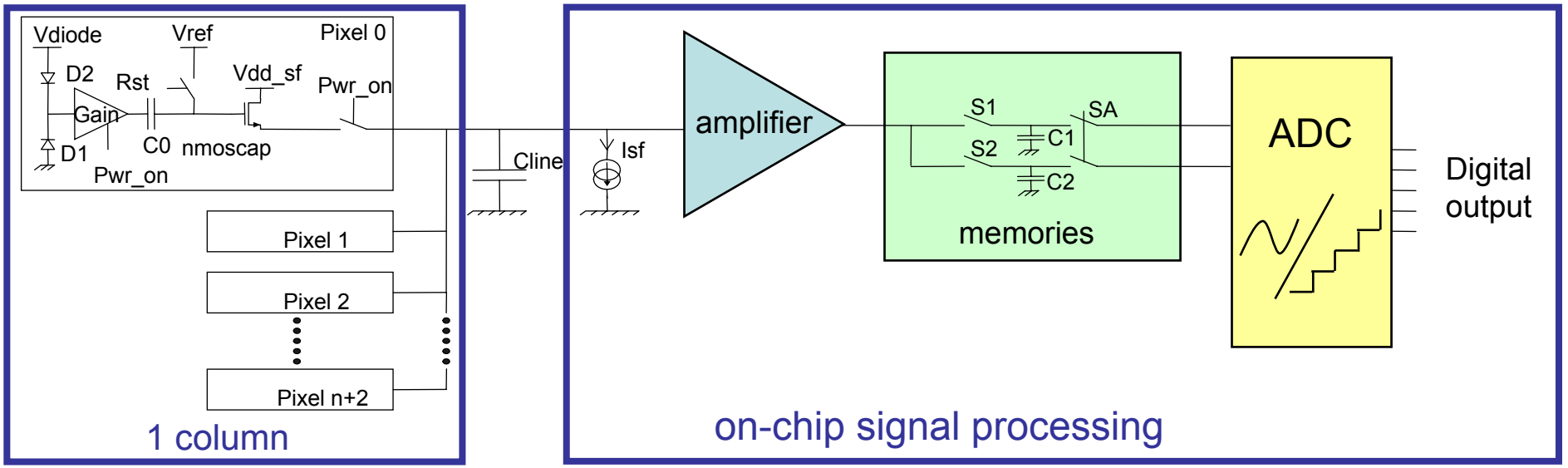


V_{th}=10mV

Testing the chip MIMOSA8

- **Beam tests : 5 Gev electron beam at DESY**
- **Measures :**
  - temperature : -20°C => 20°C
  - Discriminator threshold : 3.5, 4, 5, 6, 7, 8, 20 mV
  - Frequency : 40 Mhz, readout time : 50µs
- **Off line analysis (very preliminary results) :**
  - Detection efficiency up to 99 %
  - ENC : < 20 electrons

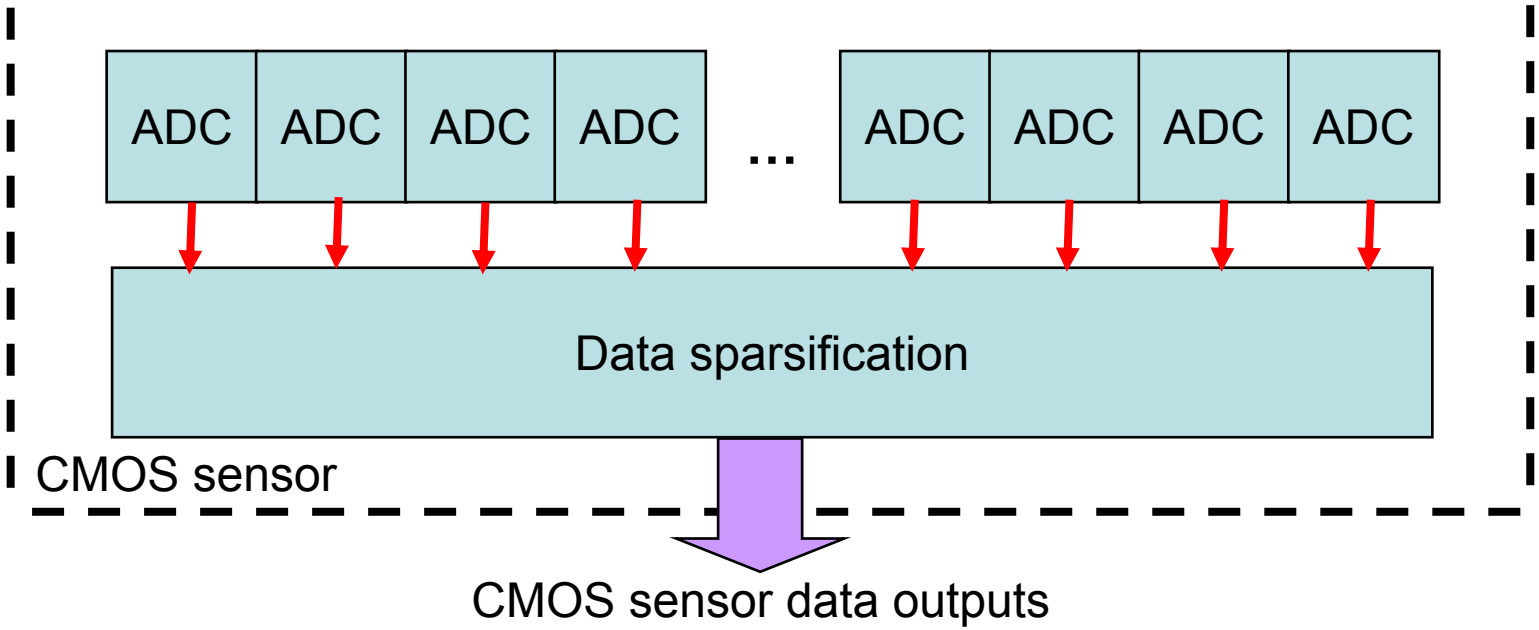
On-chip signal processing : ADC



- Fast, low power, compact layout ADC :
  - 3~5 bits digital outputs
  - conversion time : <100ns
  - input single ended or differential input
  - <0.5mW consumption
  - pitch of the ADC limited to 20μm

- Various ADC architectures under study :
  - Flash ADC (LPC, Clermont Ferrand)
  - Pipeline ADC (LPSC, Grenoble)
  - Wilkinson ADC (IReS, Strasbourg)
  - Successive approximation ADC (IReS, Strasbourg) (DAPNIA, Saclay)

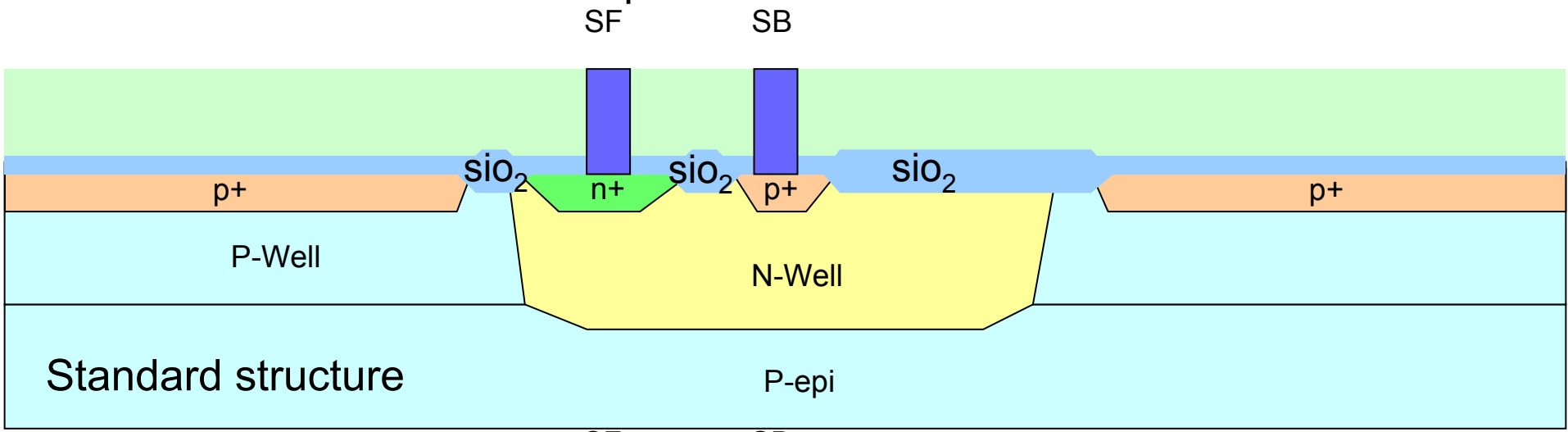
On-chip signal processing : Digital processing

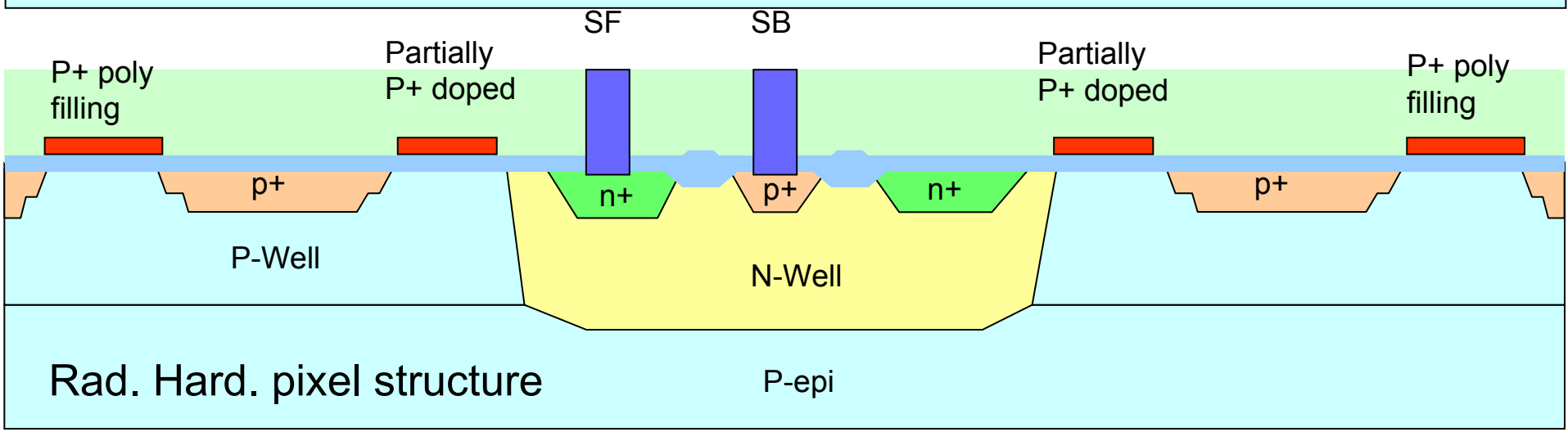


- Raw data flow O(10^2) Gbit / sec / chip
- Data compression by integrated spasification µcircuits
- A reduction factor of 10 - 100 is needed : challenge !

CMOS sensor radiation tolerance results

- Radiation tolerance tests performed at for several radiation doses



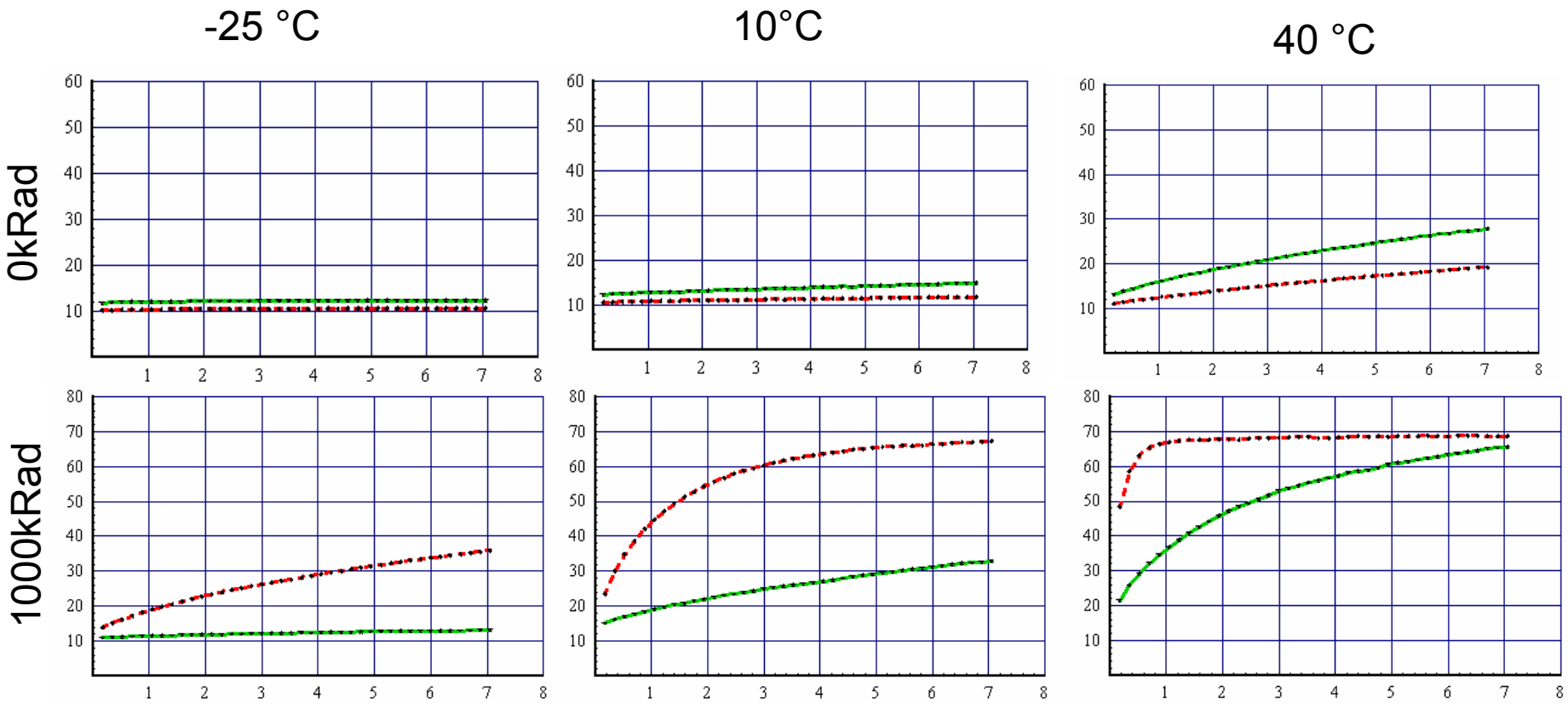


CMOS sensor ionising radiation tolerance results

Standard Pixel versus radiation hard Pixel as a function of :

- X-ray (10 Kev) irradiation : 0 => 1 MRad
- Temperature : -25 °C => 40°C
- Tinteg : 200µs => 7 ms

x: Time in ms, y: Noise in electrons



Conclusion and outlook

- **Outcome of achieved R&D :**
  - CMOS Sensor is an attractive technology for future vertex detectors
  - envisaged for CBM, ILC, STAR Upgrade (and BELLE)
  - viable pixel architectures including “CDS” obtained
  - Fast column parallel architecture with integrated discriminator / col. tested on beam
- **Present R&D issues :**
  - design of ADC architectures
  - exploration of fabrication processes with feature size < 0.25 μm, …..
  - improving radiation tolerance
- **Other R&D topics :**
  - thinning < 50 μm