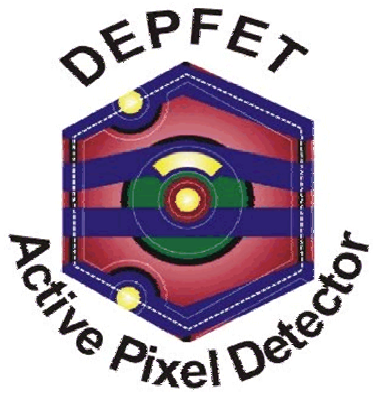
Front-End Electronics for DEPFET Sensors



Peter Fischer for the DEPFET collaboration

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Preface

- The DEPFET collaboration (Munch, Bonn, Mannheim, others joining) is presently developing devices and systems for **ILC** and **Xray satellite missions** (XEUS and others).

- There is no involvement in FAIR experiments so far.

- This talk describes the main features of DEPFETs for the detection of ionizing particles so that a possible benefit for the FAIR experiments can be evaluated.

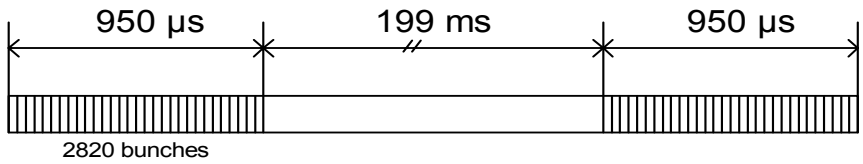
- Xray detection with DEPFETs (an important application) is not treated here.

Talk Outline

- ILC requirements & possible geometry of ILC DEPFET layer
- The DEPFET working principle
- Sensor design & technology
- Thinning technology
- Readout, chips and the ILC prototype system
- Measurements on ILC structures:
  - -Noise, clear efficiency
  - -Matrix: Lab results
  - -Matrix: Test beam results
- Summary

Requirements for ILC innermost Tracker Layer

- Time structure: one train of **2820 crossings** in **~1 ms** every **~200ms**

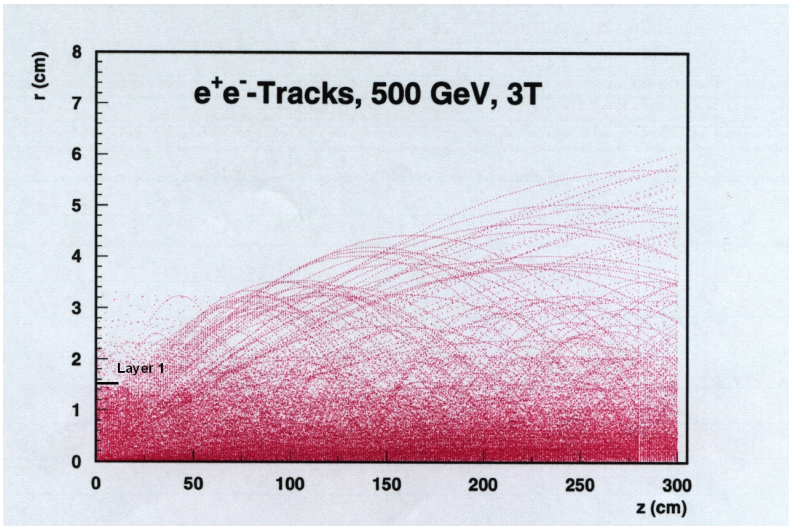


- Hit density: For a 10 cm long cylinder at **r=15 mm** (A=10500 mm²):
  ~ 370 tracks / crossing
  ~ 0.035 tracks / mm² / crossing
  ~ **100 tracks / mm² / train**

  much less if r > 15 mm (~ 1/7 for r=27 mm)

- Row readout rate: some 10 MHz

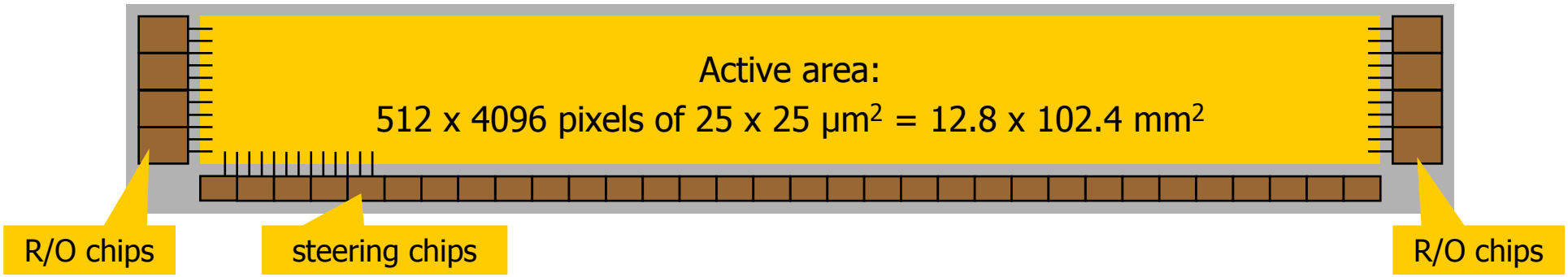
- Resolution: **few µm** ($\Rightarrow$ pixel size $\leq$ 25 x 25 µm²)
- Radiation tolerance $\geq$ **200 krad** (for 5 years operation)
- Radiation length very small: **~0.1% X_0** per layer



(simulation from C. Büsser, DESY)

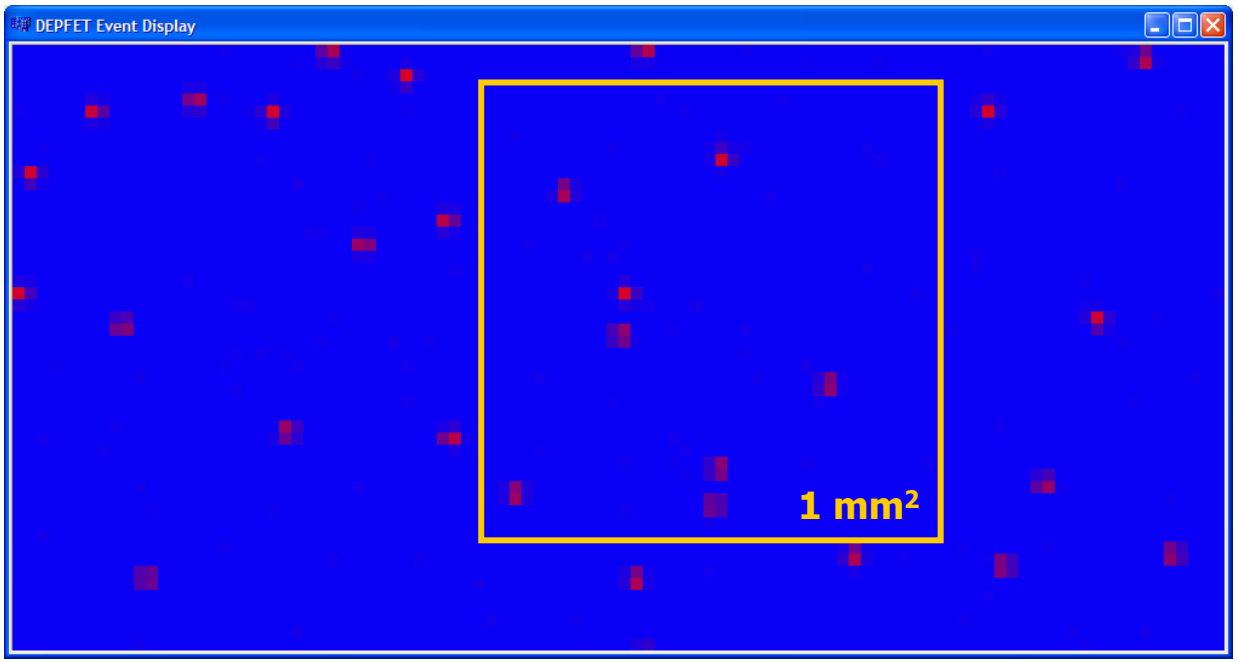
ILC DEPFET Module (Layer 1)

- Modules have active area ~**13 x 100 mm²**
- They are read out on **both sides**.

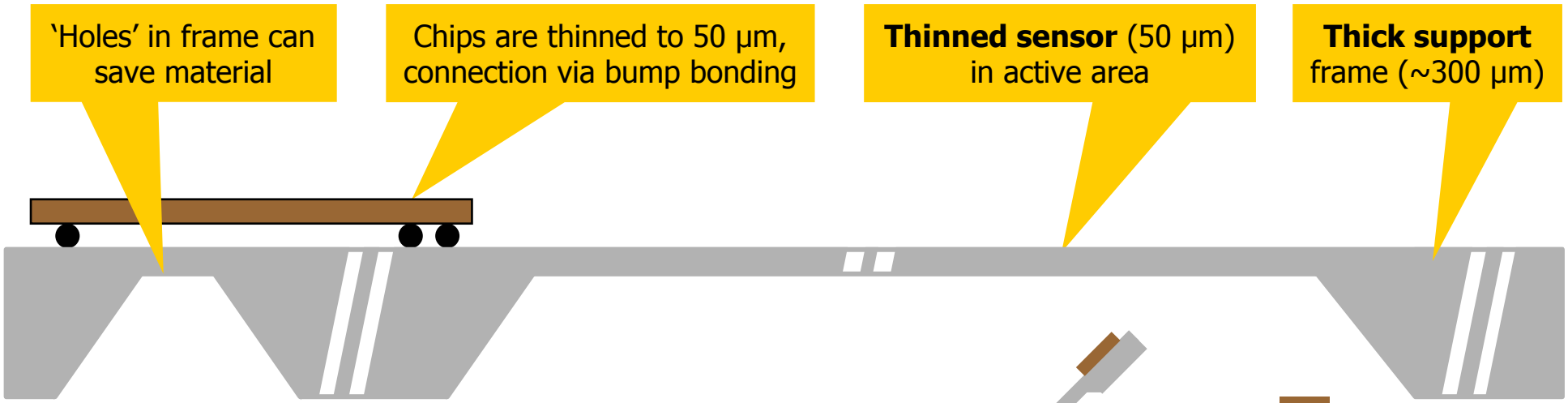


- Occupancy simulation:
  - Assume signal width of 10µm
  - Read **10 frames** per train
    i.e. 10 x 2048 rows in 1ms
    or one row in 50ns (**20MHz**)
  - Expect ~10 tracks / mm² / event

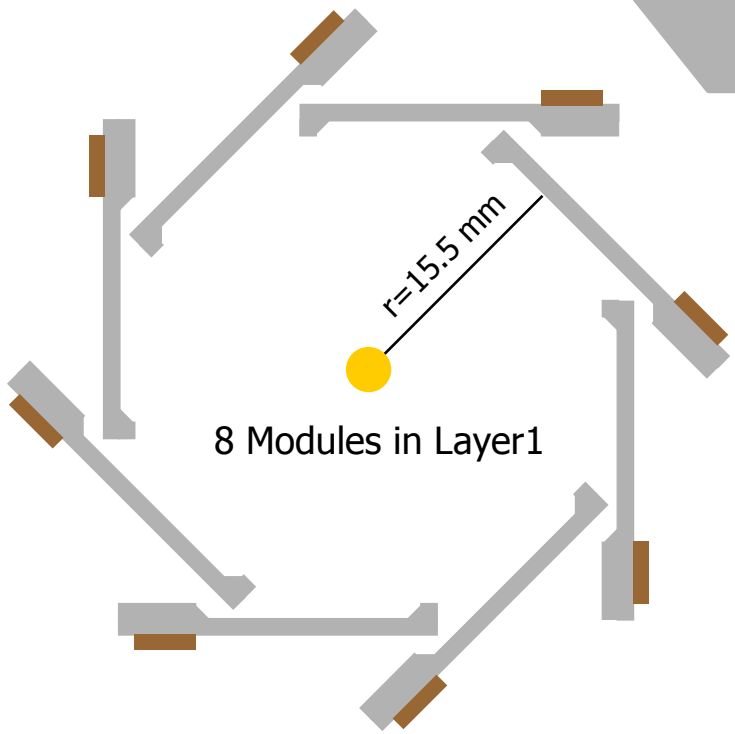
- Pattern recognition should not be a problem!



Possible Geometry of Layer 1



Cross section of a module

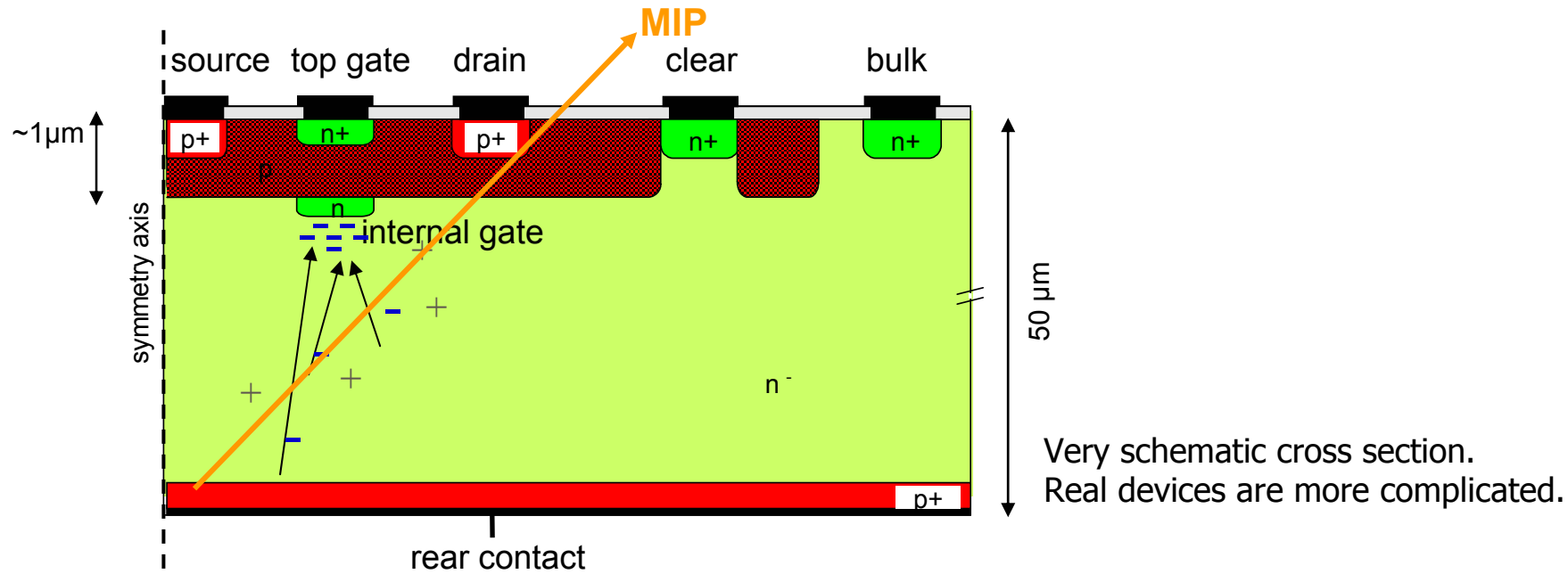


Estimation of material budget:

- pixel area: 13x100 mm^2, 50µm: 0.05% X_0
- steering chips: 2x100 mm^2, 50µm: 0.01% X_0
- frame w. holes: 4x100 mm^2, 50% of 300µm: 0.05% X_0
- total: **0.11% X_0**

DEPFET Principle of Operation

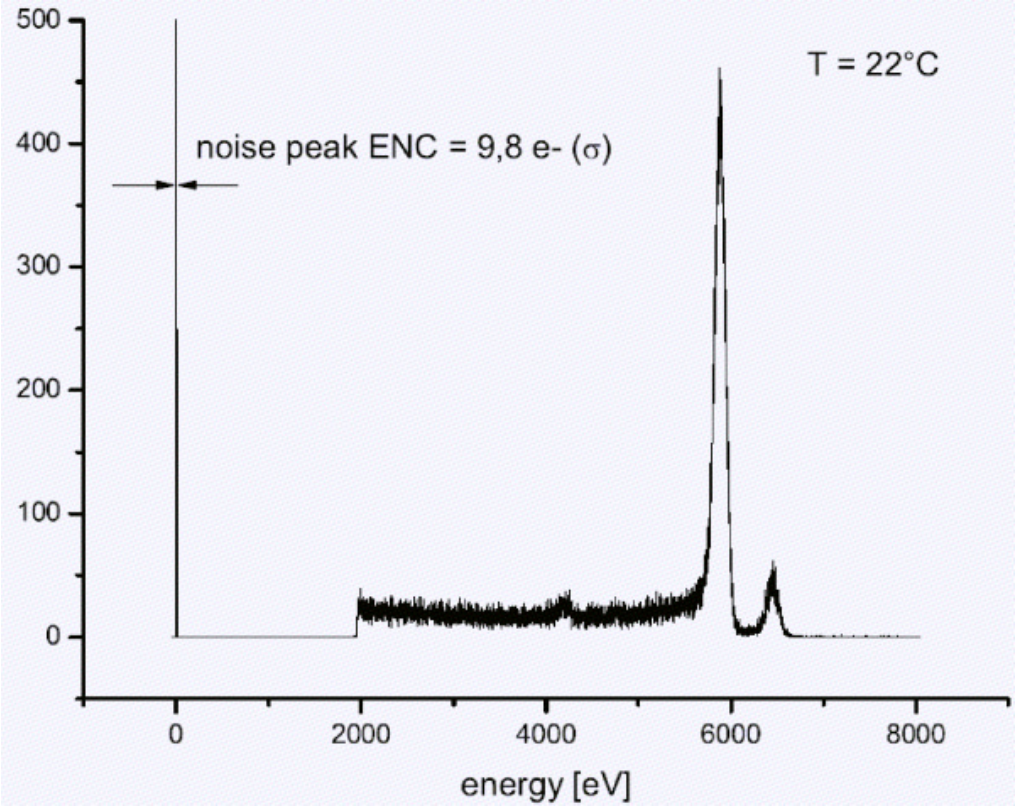
- A **potential minimum for electrons** is created under the channel by **sideward depletion**
- A **p-FET** transistor is integrated in every pixel
- Electrons are collected in the „internal gate" and **modulate the transistor current**
- Signal charge is removed via a clear contact
- Readout can be at the source ('voltage signal') or at the drain ('current signal') – **ILC uses drain readout**



- **Advantages:**
  - **Fast** signal collection in **fully depleted** bulk
  - **Low noise** due to small capacitance and first amplification
  - Transistor can be **switched off** by external gate – charge collection is then still active !

Noise in ILC DEPFET Pixels

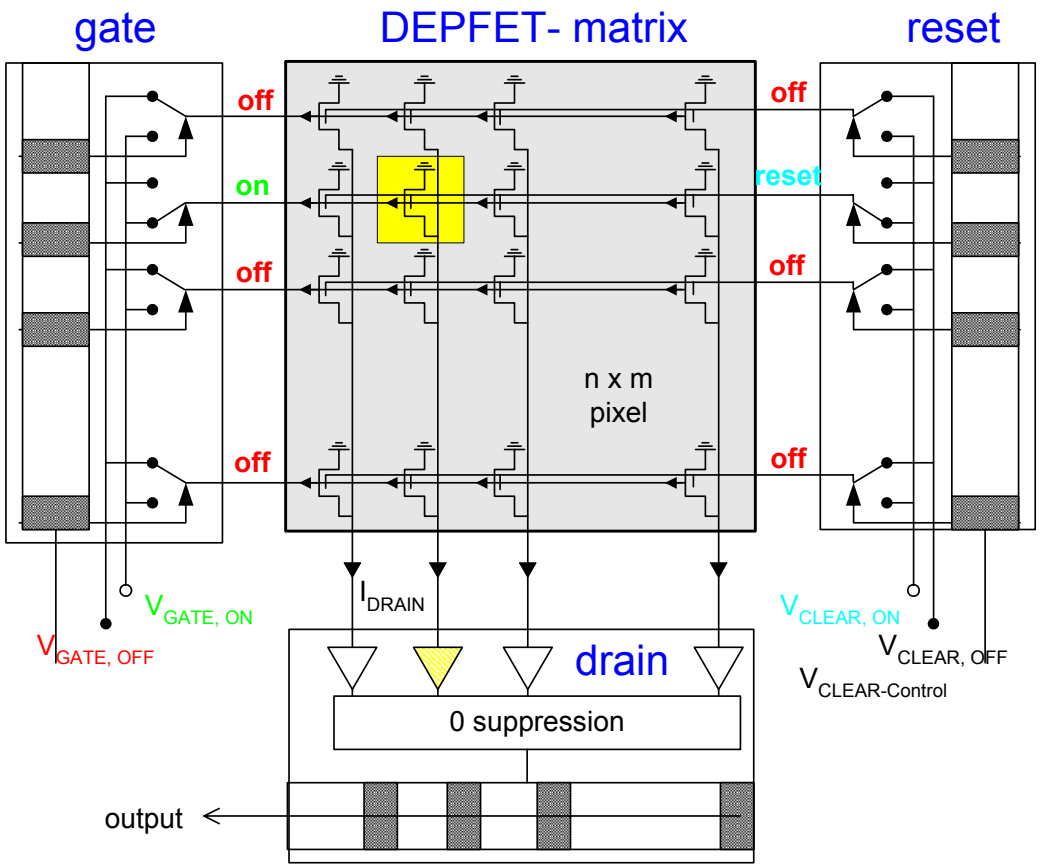
- ^{55}Fe spectrum with ILC structure taken at room temperature with 10µs shaping time:



- Noise peak: 10e$^-$
- Best DEPFET result (large XEUS structure, cold, slow): 2.2e$^-$
- **DEPFETs regularly provide noise below 10e$^-$** @ room temperature (for single devices with slow shaping)!

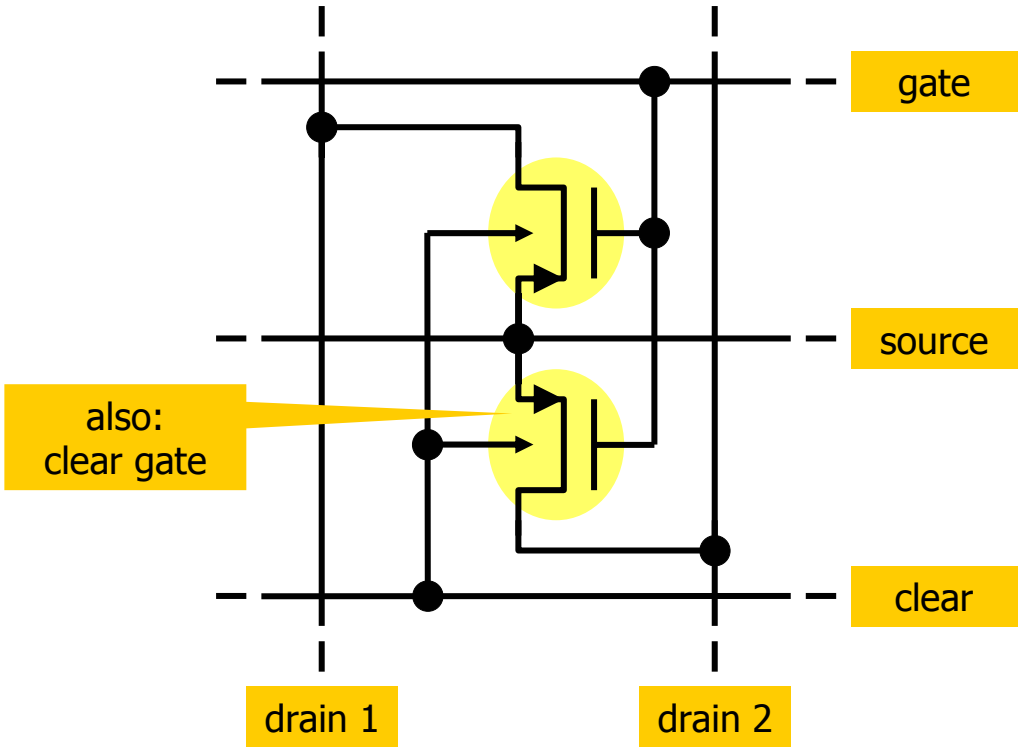
Matrix Operation

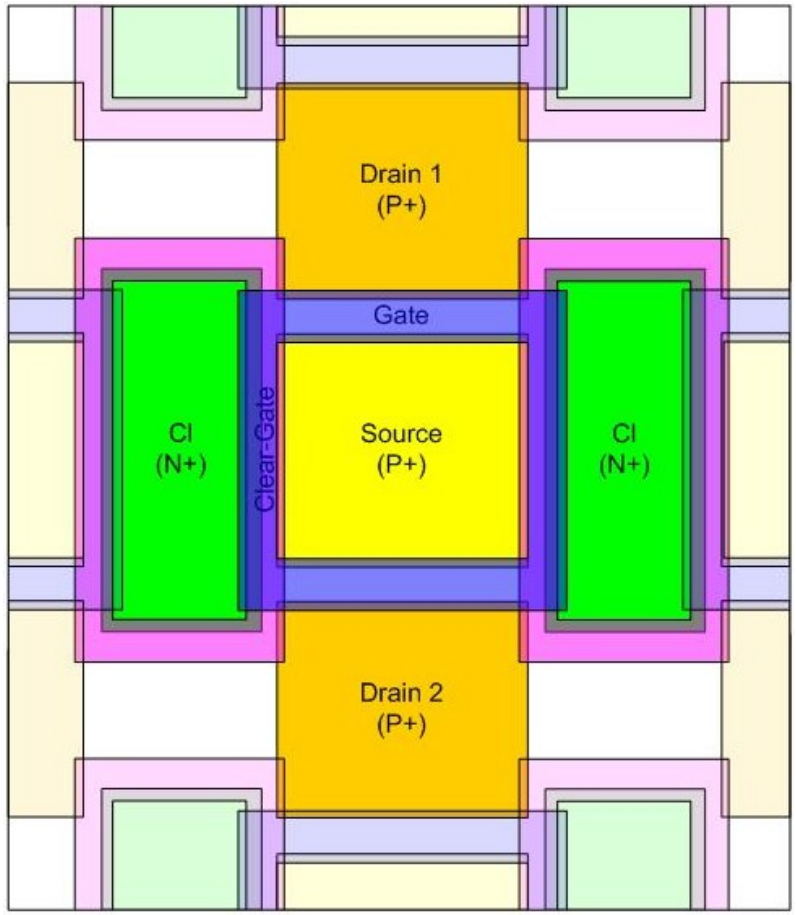
- Connect **gates and clears horizontally** to select / clear single rows. Apply voltages with SWITCHER chips.
- Connect **drains (or sources) vertically** and amplify current (or voltage): CURO (CAMEX) chip
- Charge is not shifted!
- Readout sequence: Enable row – read current (I_{sig} + I_{ped}) – clear – subtract current (I_{ped}) – move to next row



Sensor Design: MOS Devices

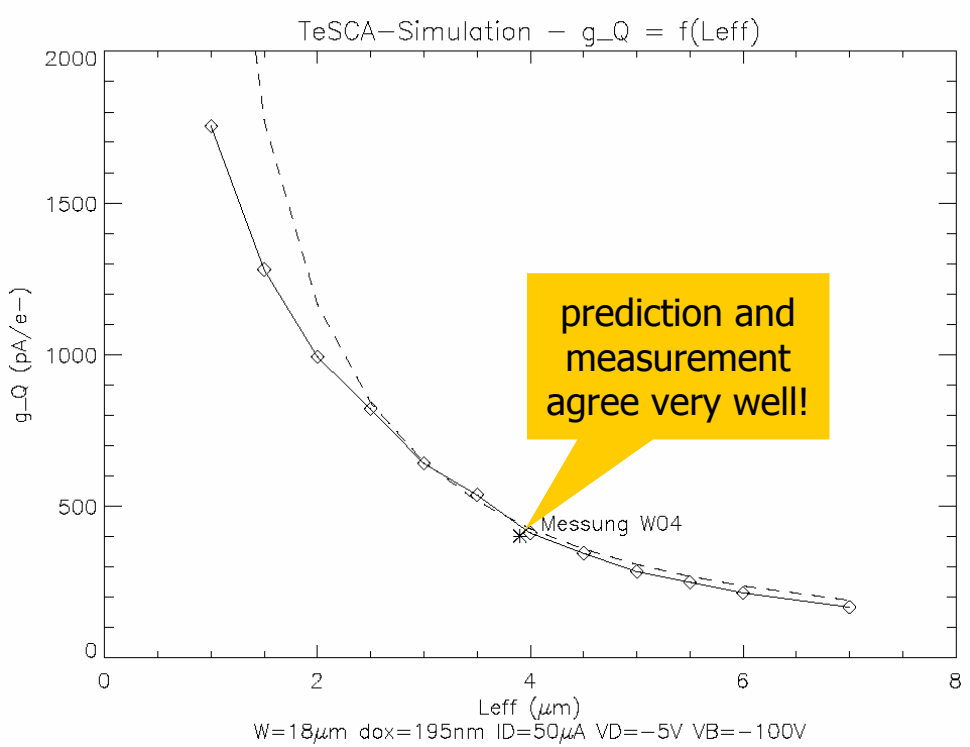
- Advantages of IGFET devices (earlier DEPFETs were JFETs)
  - smaller device variations (required for large sensors)
  - smaller pixels (linear transistors possible)
  - issue: radiation tolerance of gate oxide ?
- Increased amplification (now ~1nA / e^-)
- Fast and complete clear (using clear gate)
- Compact double pixel cell



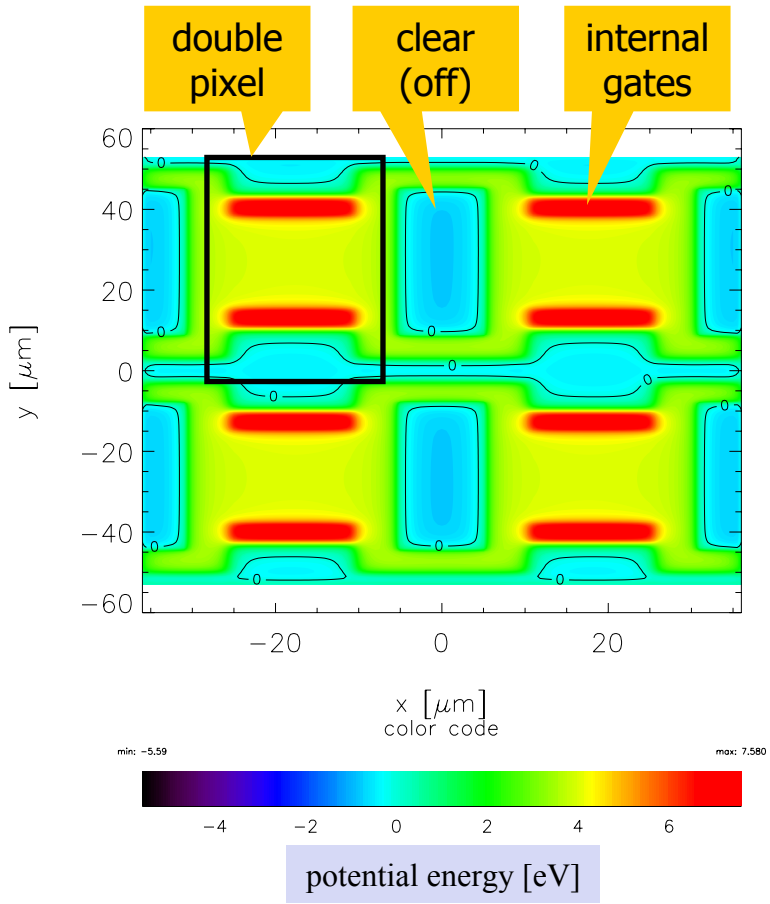


Sensor Simulations

- HLL uses 3D-Simulator (Poseidon) for complicated structures
- Device behavior can be predicted accurately.
  Important for successful new designs!



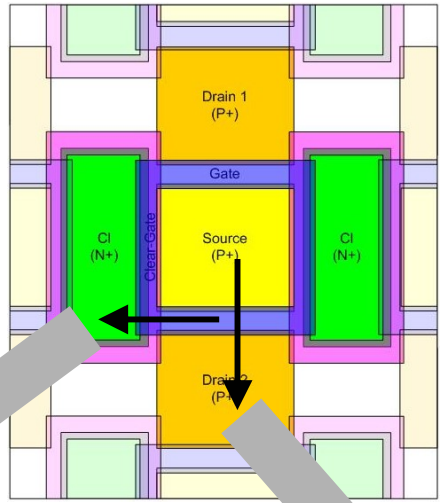
charge gain g_q for varying gate length

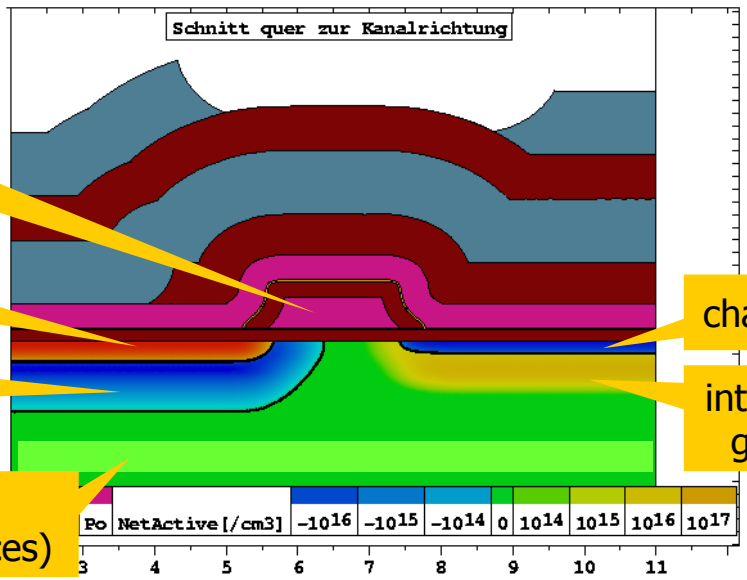


Potential distribution in 1µm depth in charge collection mode

Device Cross Sections

- Added **'clear gate'** to lower the clear barrier.
  Clocked and **static** operation possible
- Added a deep **high-E** n-implantation in some devices to lower clear voltages (clear channel is moved into bulk)





clear gate (Poly)

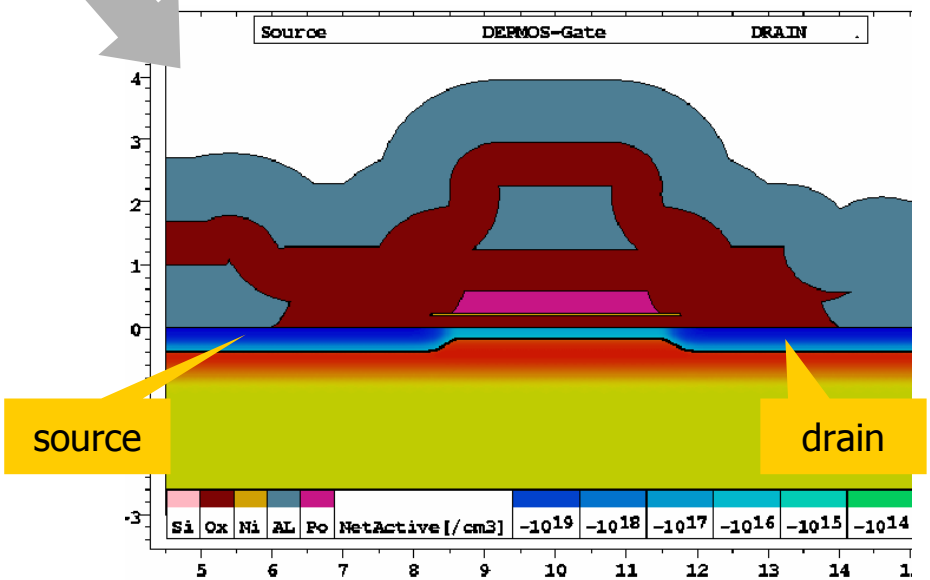
clear (n^+)

p-well

high-E (some devices)

channel

internal gate

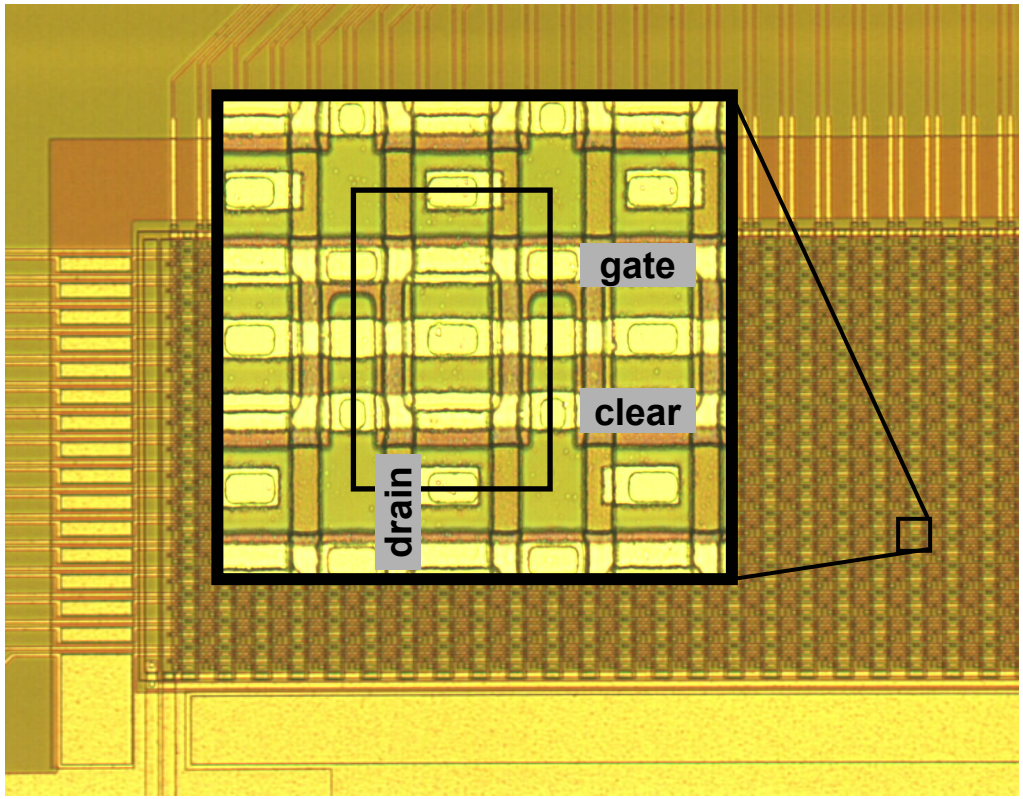


source

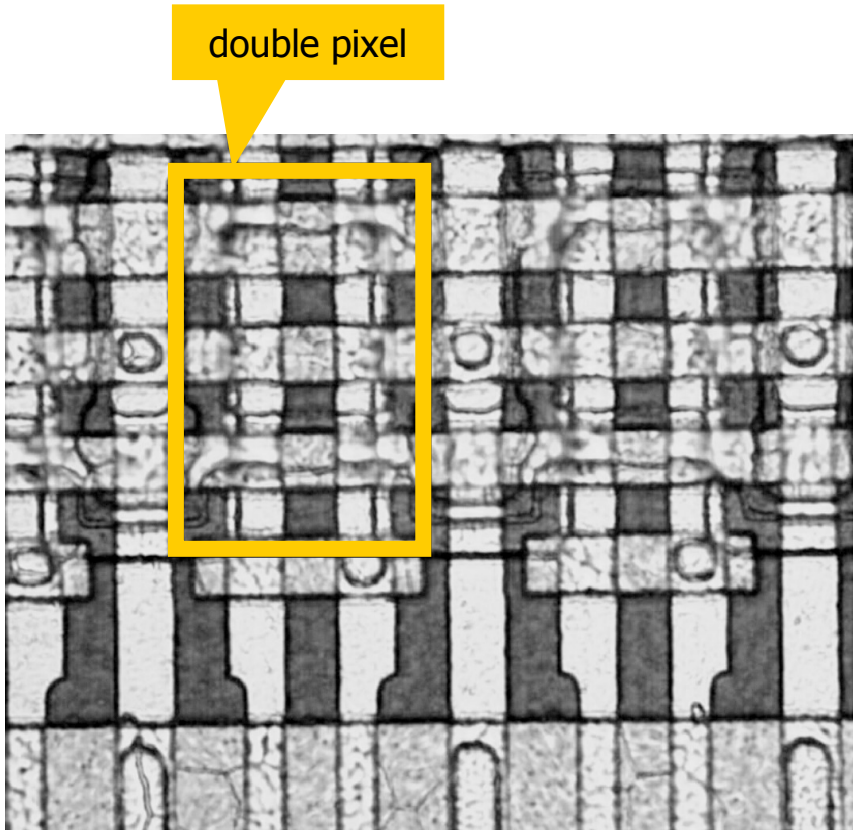
drain

Sensor Fabrication Technology

- A sensor-compatible technology with **2 poly and 2 metal layers** has been developed at HLL
- These are required for large matrix designs



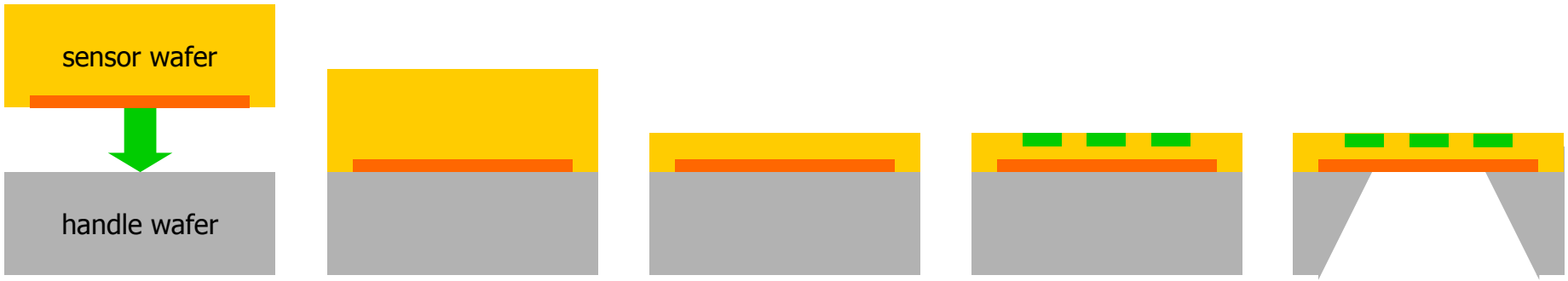
16x128 test matrix, double pixel cell 33 x 47 μm²



double metal matrix

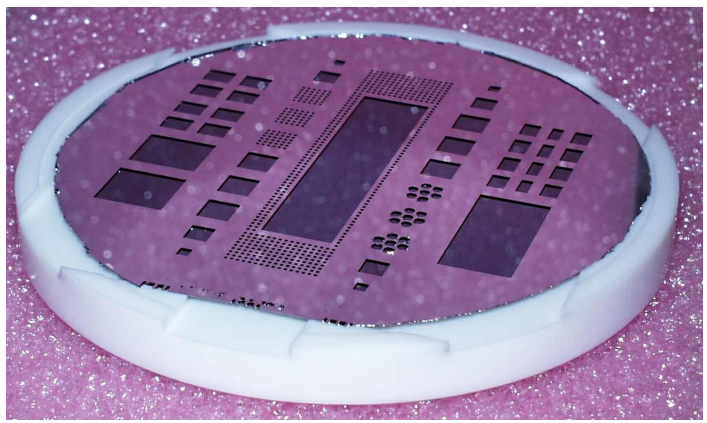
Making thin Sensors

- A novel technology to produce detectors with **thin active area** has been developed and prototyped



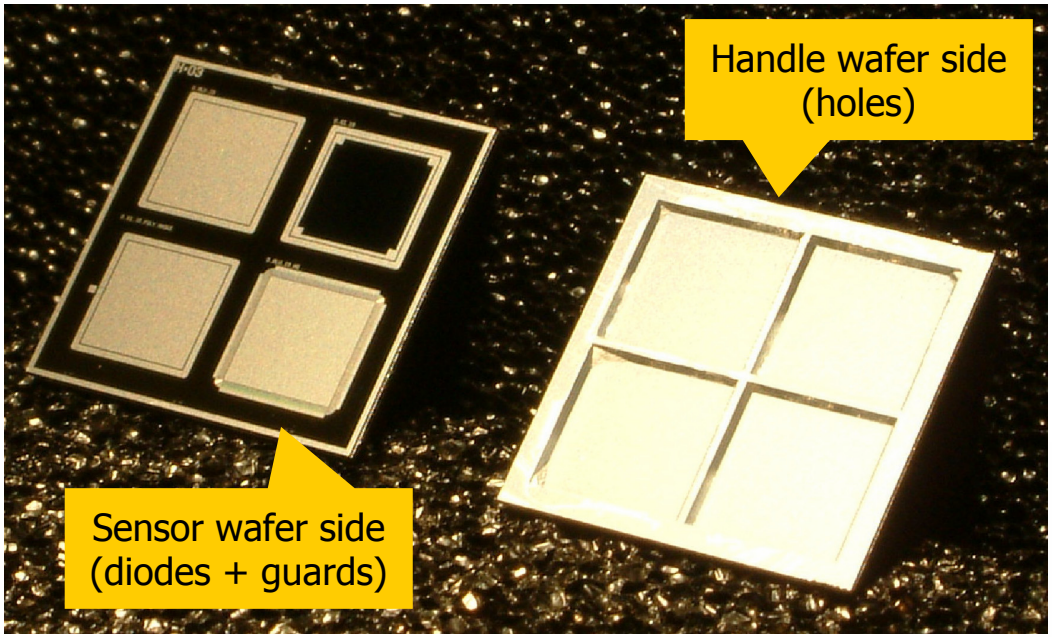
1. implant backside on sensor wafer
2. bond wafers with SiO_2 in between
3. thin sensor side to desired thickness.
4. process DEPFETs on top side
5. etch backside up to oxide/implant

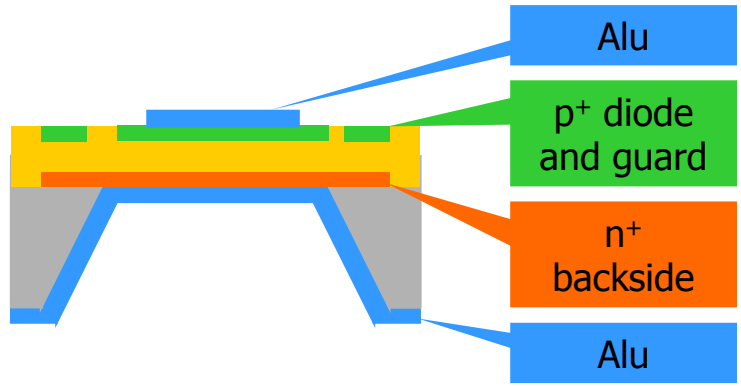
first 'dummy' samples:
50µm silicon with 350µm frame

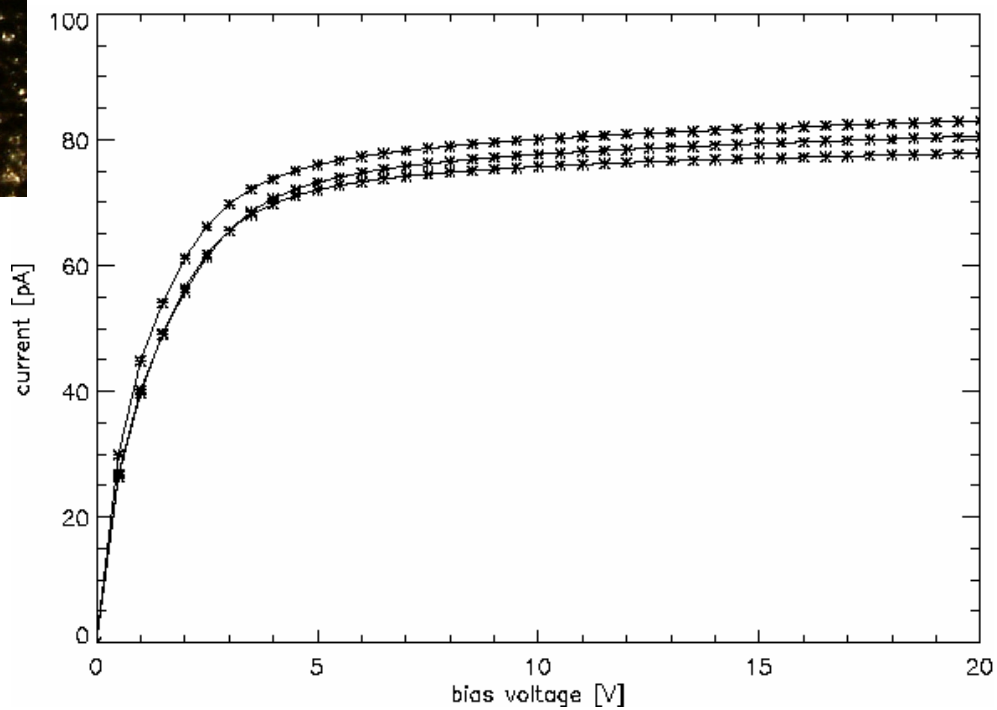


thinned diode structures:
leakage current: <1nA /cm^2

Quality of Thin Diodes is very good

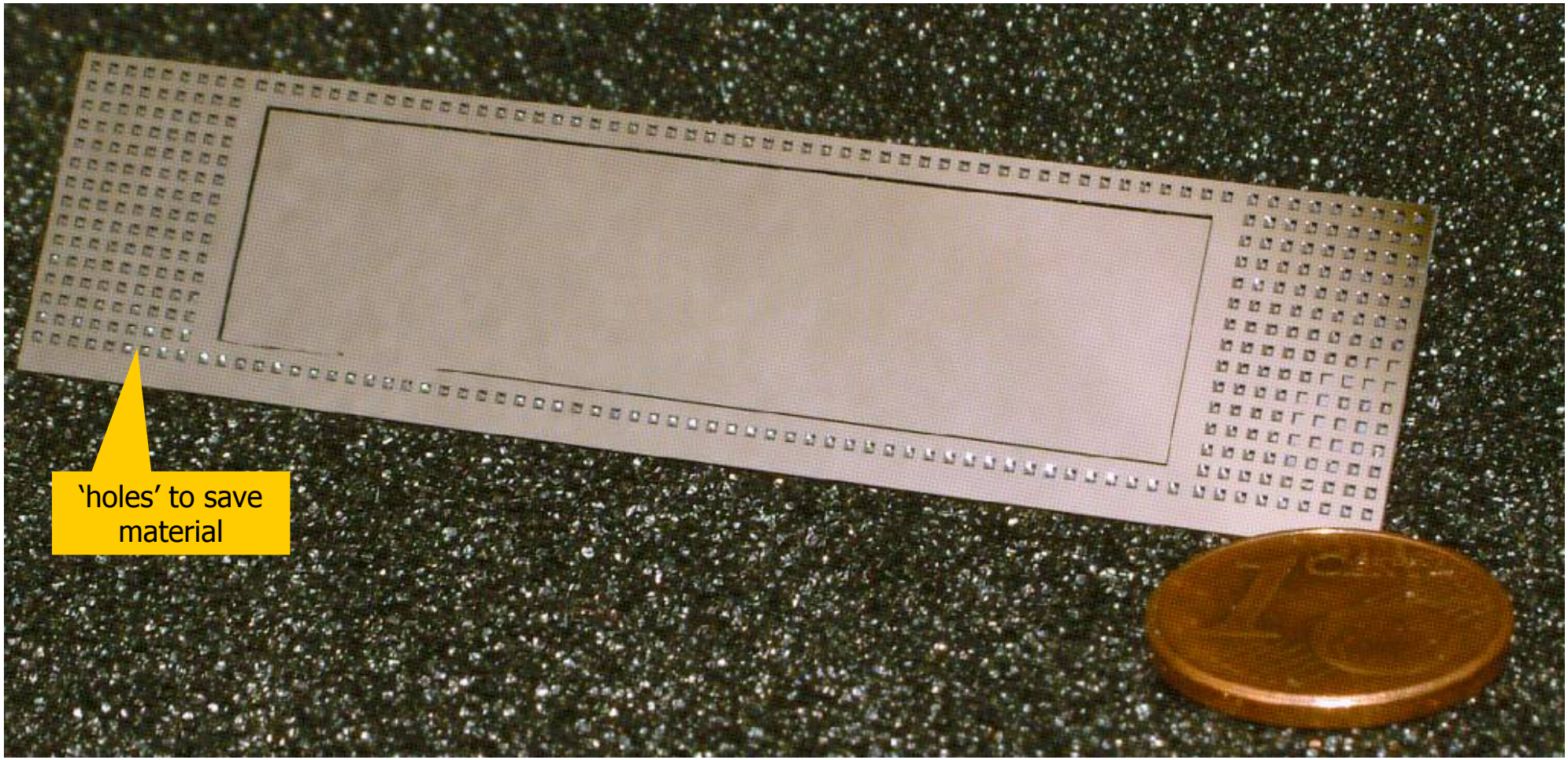






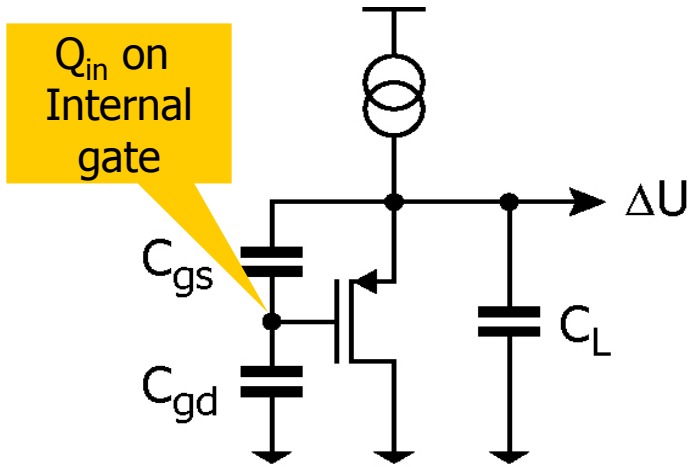
- 10mm^2 diodes on 50µm have been produced
  (in test lab, 'real' devices will be even better!)
- Measured leakage currents are very low: **150 nA/cm^3**
  (~very good strip detector)
- No breakdown is observed even at strong over-depletion

Dummy Module with ~ ILC Geometry



Source Follower and Drain Readout

Readout at the source (follower)

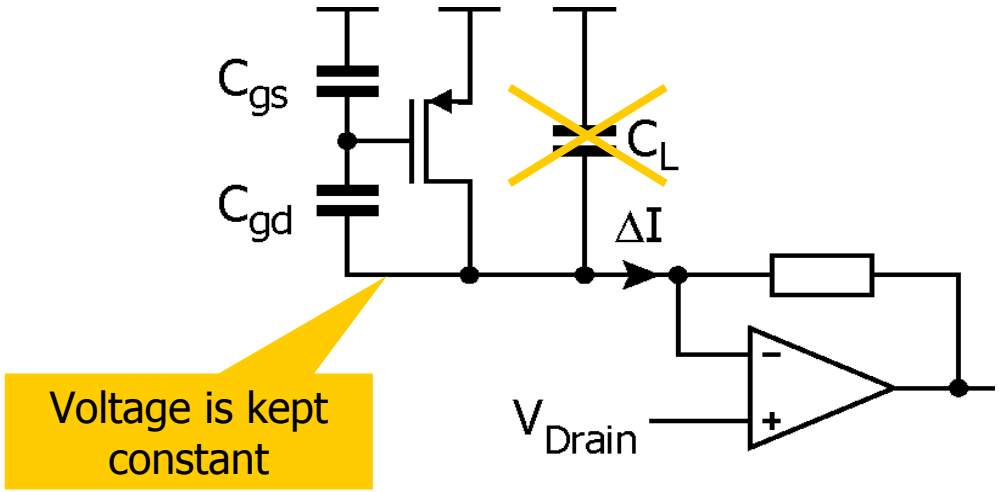


$$\Delta U \approx \frac{Q_{in}}{C_{gd}}$$

$$\tau = 2.2 \times \frac{C_L\,(1+C_{gs}/C_{gd})}{g_m} \approx \mu s$$

Design (C_{gs}, C_{gd}) is a compromise between gain and speed

Readout at the drain

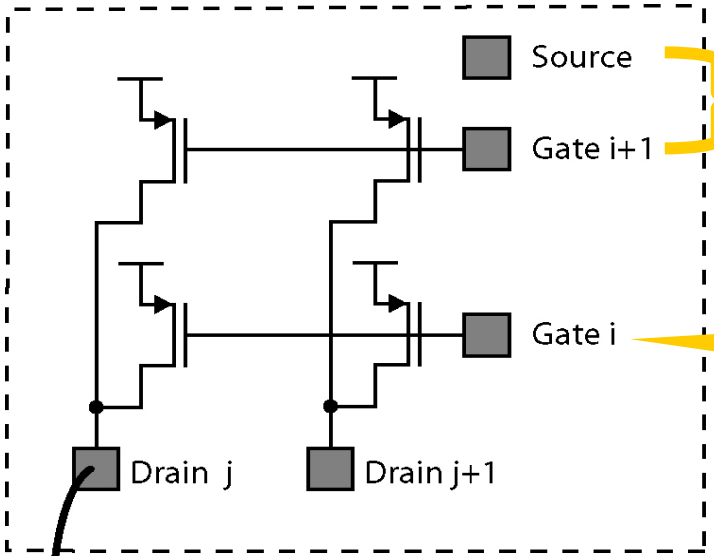


$$\Delta I \approx \frac{Q_{in}}{C_{gd}+C_{gs}} \times g_m$$

$$\tau = \text{very small}$$

High speed: drain voltage does not change due to virtual ground (limited by R_{drain}, charge collection, ...)

Matrix readout (at the Drain)

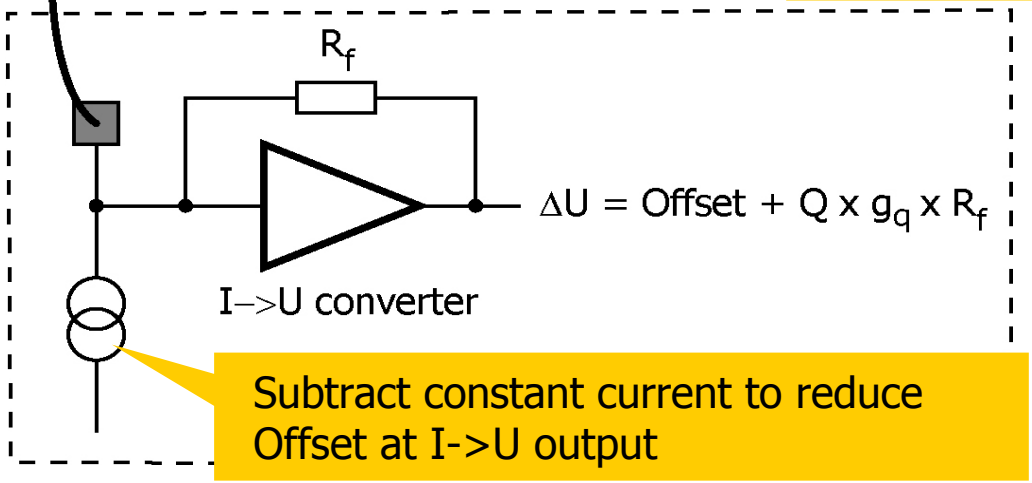


Current is fixed by V_{gs}
(often V_{gs} = 0V for high g_m and to reduce pickup from gate voltage)

External gates are used
to switch on one row only

$I = I_0(V_{gs}) + Q \times g_q$

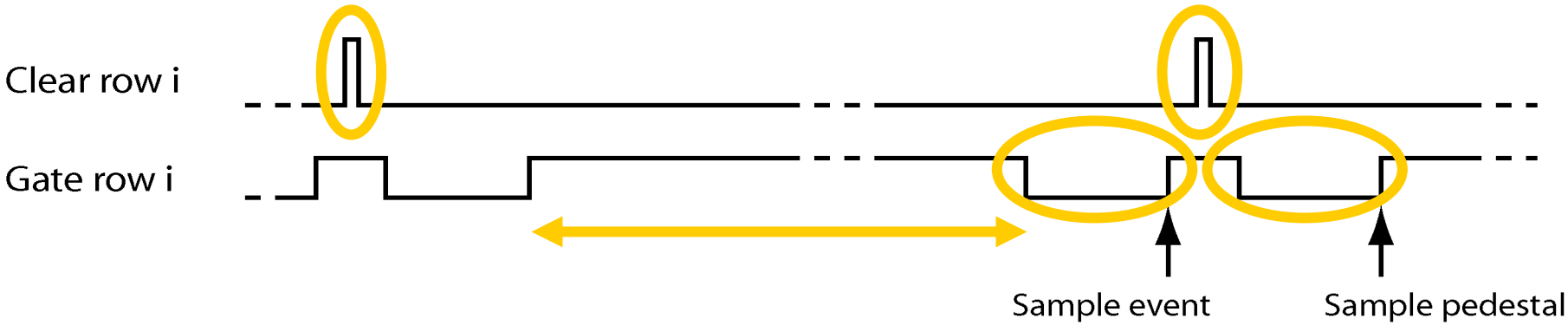
$g_q \approx 200pA$ / electron



Subtract constant current to reduce
Offset at I->U output

Readout with complete clearing of internal gate

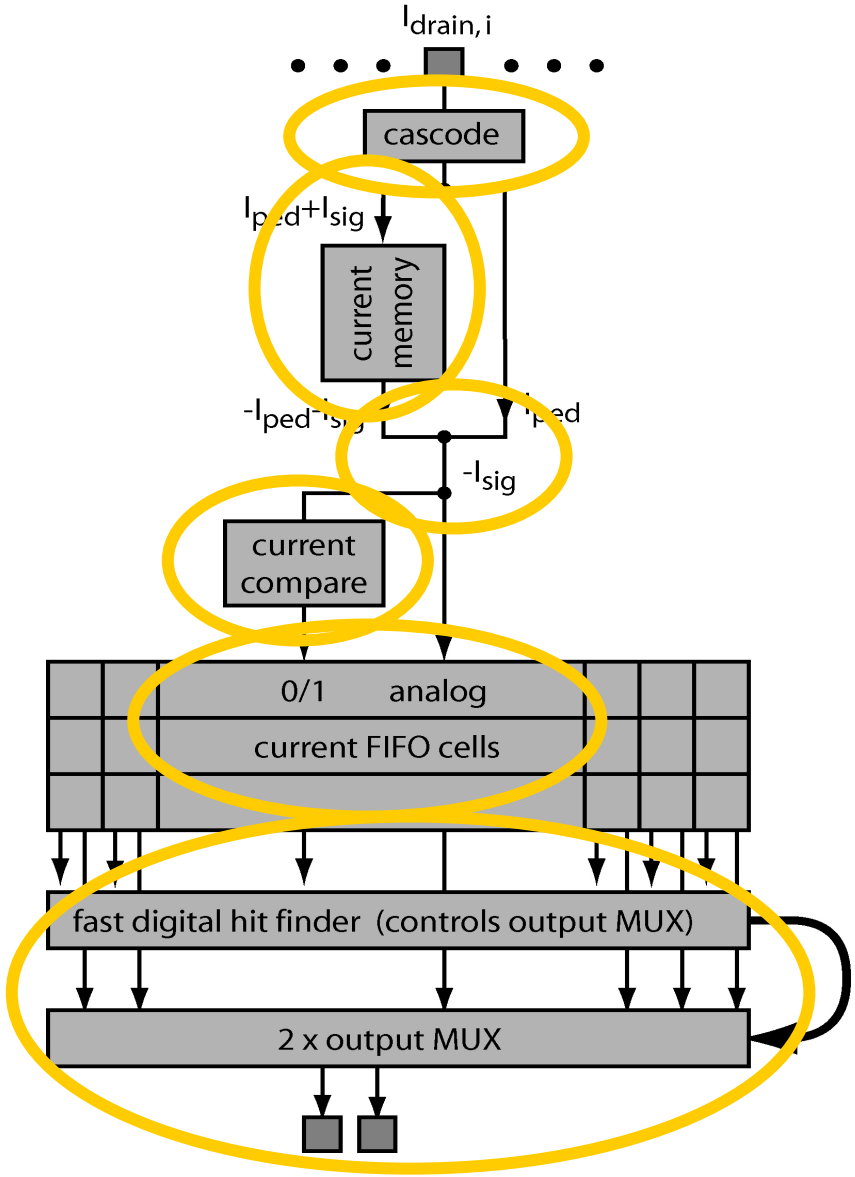
- Assume that clearing removes ALL charges from the internal gate. This works for new devices!
- The pedestal event can then be taken after the clearing.



Advantage: No need to store pedestal event

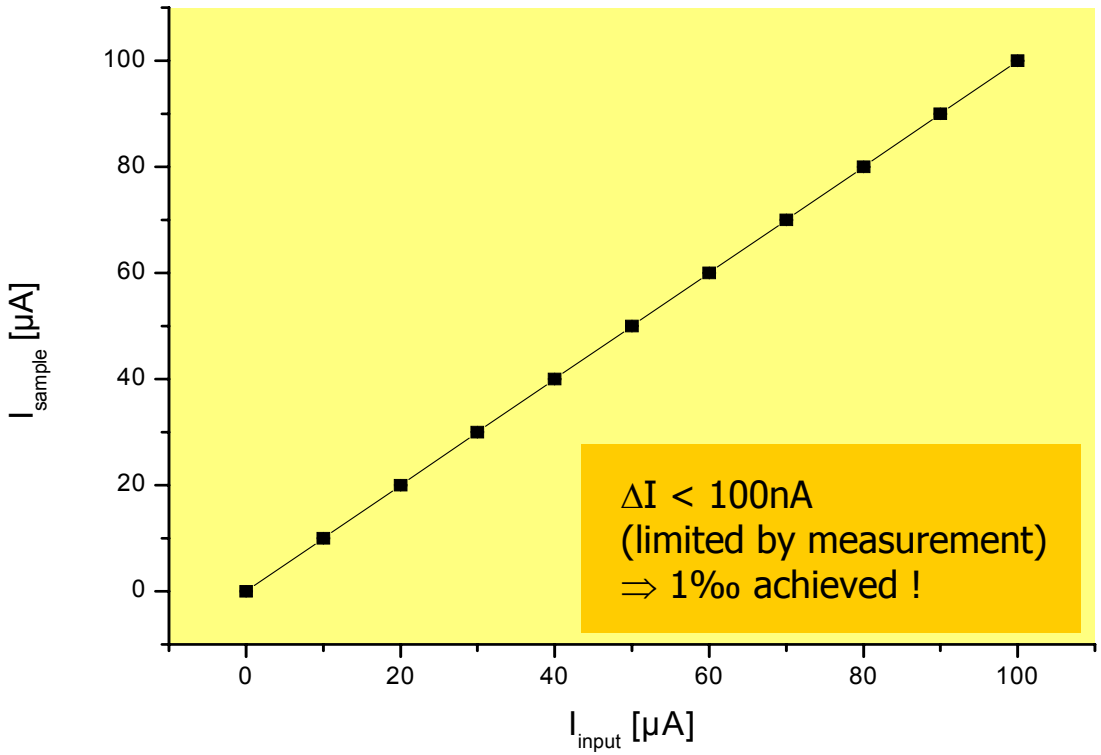
Fast drain readout of matrix with complete reset

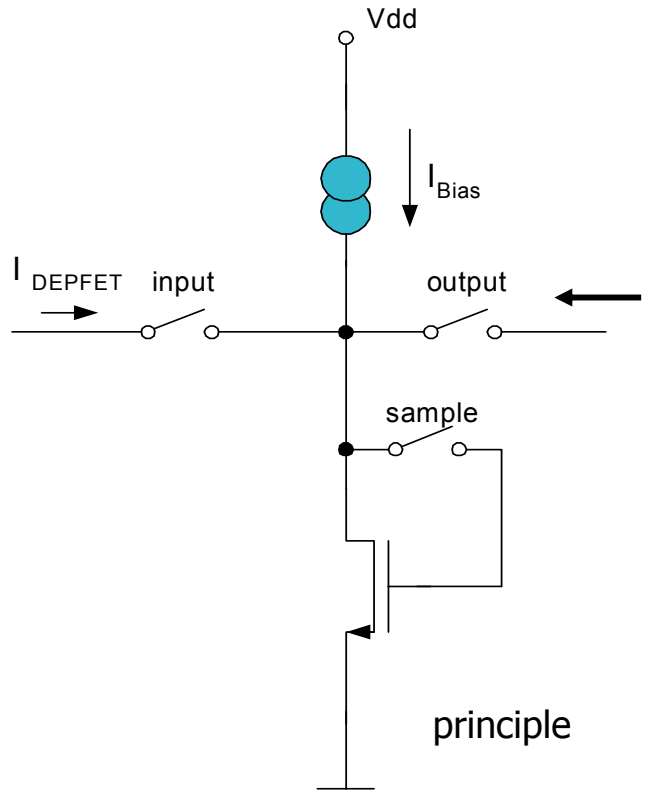
- Keep drain potential at constant potential (regulated cascode)
- Signal+Pedestal are stored in fast current memory cell (20ns)
- Pedestal after reset is subtracted by summing currents
- Hit decision with fast current comparator
- Hit + analog value stored in current memory cells arranged as a 'FIFO'
- A fast digital scanner finds hits and switches the corresponding analog current signals to two outputs.
  This is repeated until no more hits are found.
  Empty FIFO 'rows' are skipped.



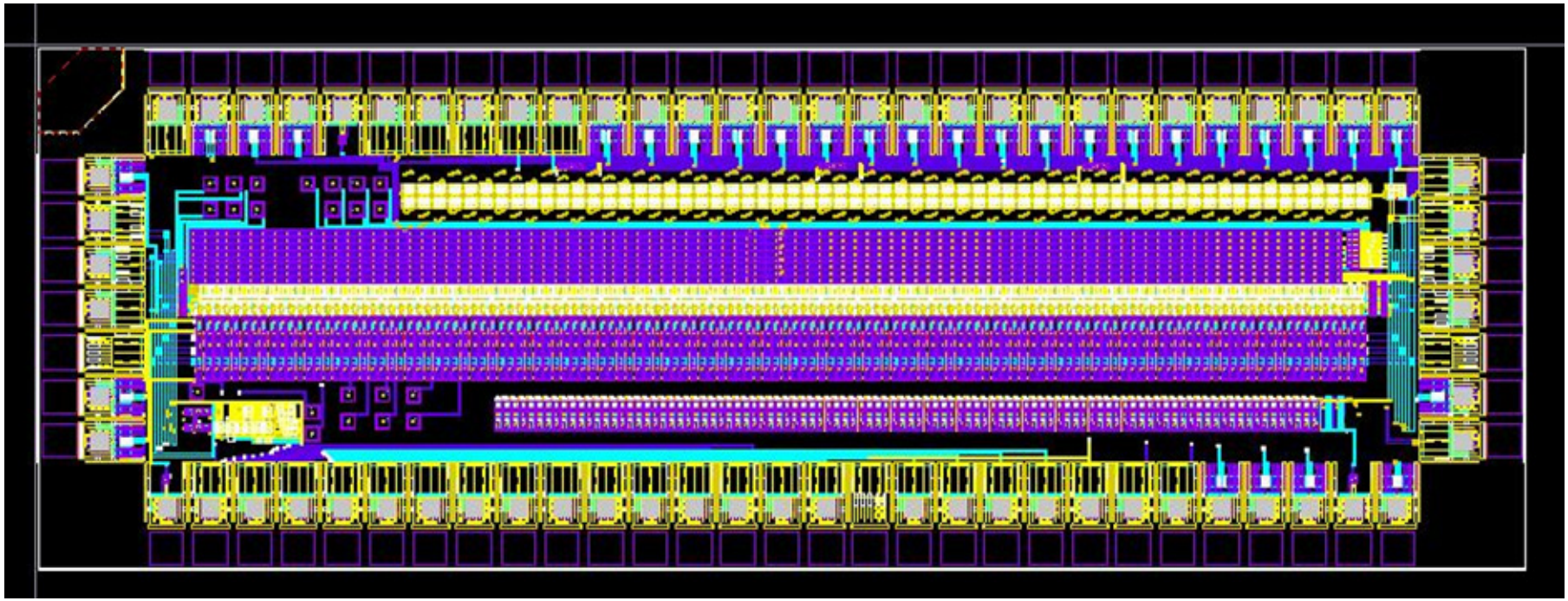
Current memory cell

- Use a 'switched current cell' which outputs $-I_{in}$ after sampling
- Design must compensate for charge injection and finite drain conductance
- Use cascoding and two stage design to meet requirement
- Implemented circuit stores a current in ~20ns with 1‰ (!) resolution (Dynamic Range is 100µA)

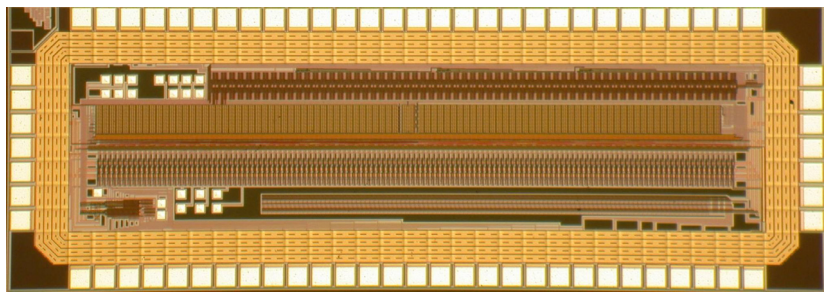




Current Readout – Testchip 1.0



- Contains all basic building blocks
  (input cascode, current memory cells, current comparator, fast hit scanner)
- TSMC 0.25 µm technology with radiation-tolerant layout rules
  (causing severe restrictions in possible NMOS geometries!)

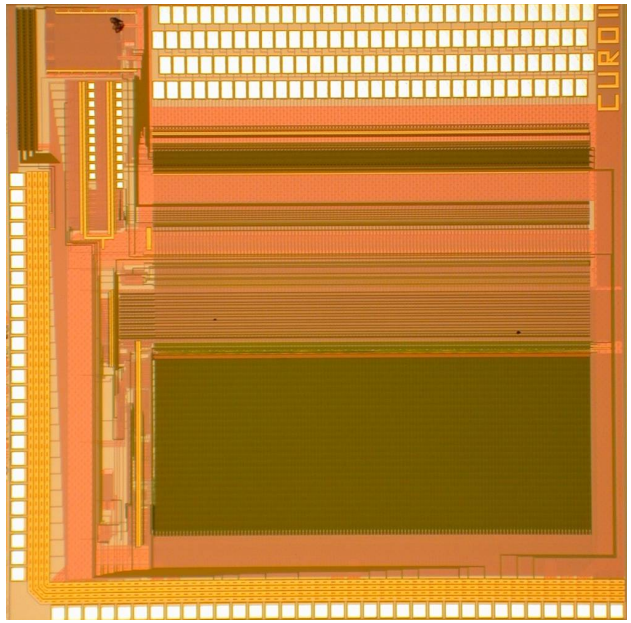


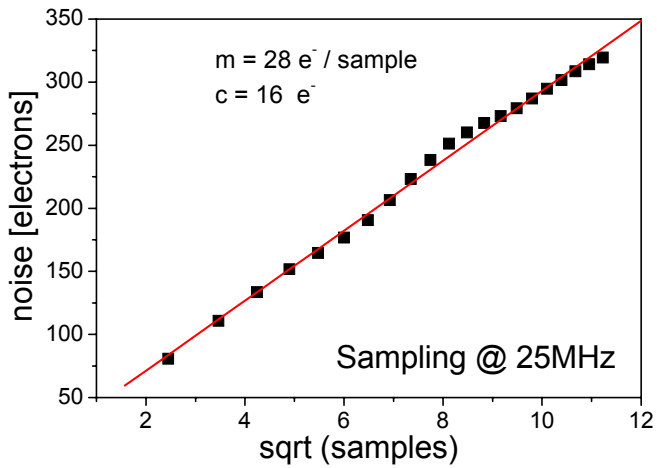
Full CURO ASIC (Drain Readout)

- **128 channel** drain readout chip
- Drain voltages are kept constant with regulated cascode circuits
- Direct **current subtraction** by switched current technique
- Real time **hit finding** and **zero suppression**
- No analog FIFO so far (only one row)
- Hit addresses store in on-chip RAM
- Many test features

- 0.25µm technology with enclosed devices. Radiation tolerance should be high

- 2.8mW/channel @ 50MHz
- Noise per sampling: 30e$^-$ @ 25MHz
- **Row rate of 25 MHz has been achieved** (i. e. sampling @ 50MHz)
- Digital zero suppression works at >100 MHz

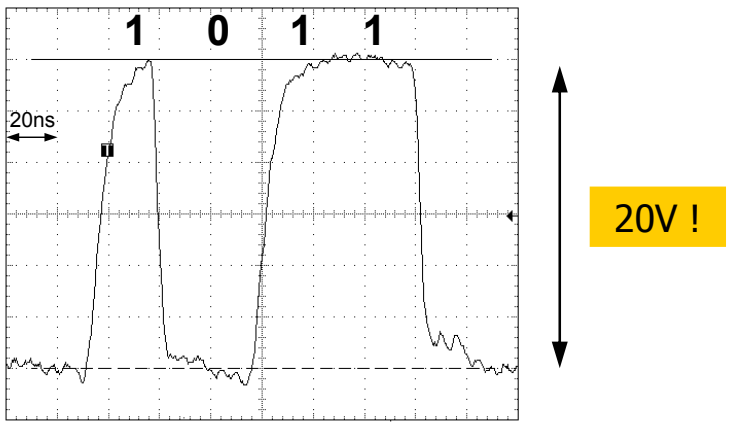




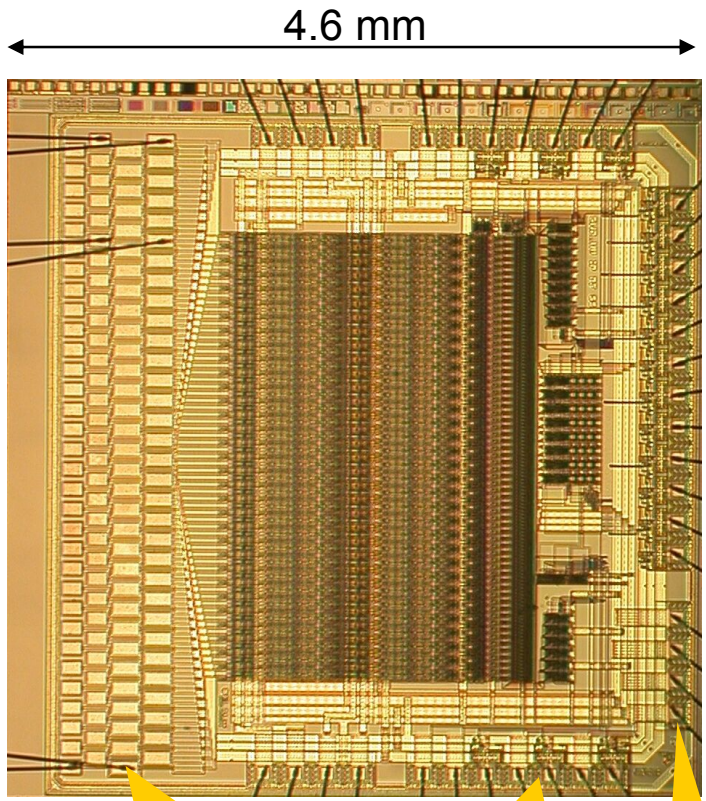
noise for multiple sampling

Switcher ASIC (Multiplexer)

- **64 channels** with **2 analog MUX** outputs ('A' and 'B')
- Can switch up to **25 V**
- **digital control ground + supply floating**
- **fast internal sequencer** for programmable pattern (operates up to 80MHz)
- **Daisy chaining** of several chips on a module possible
- Present dissipation: **1mW/channel @ 30MHz**
- 0.8µm AMS HV technology
- Chip becomes unusable at ~50krad



Switching 20V @ 30MHz

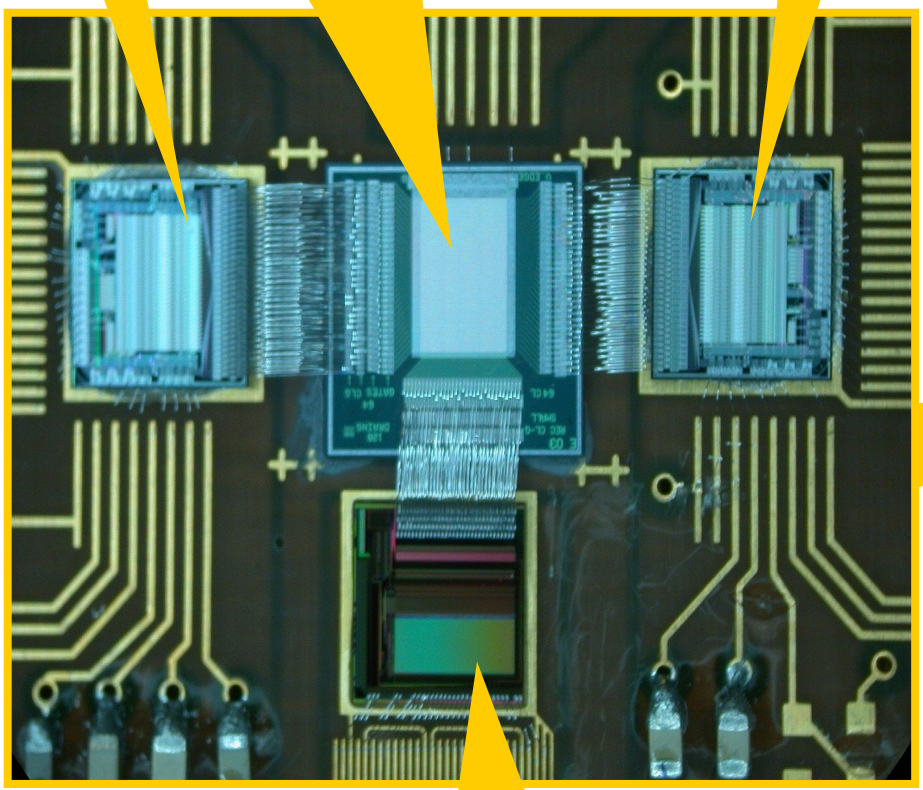


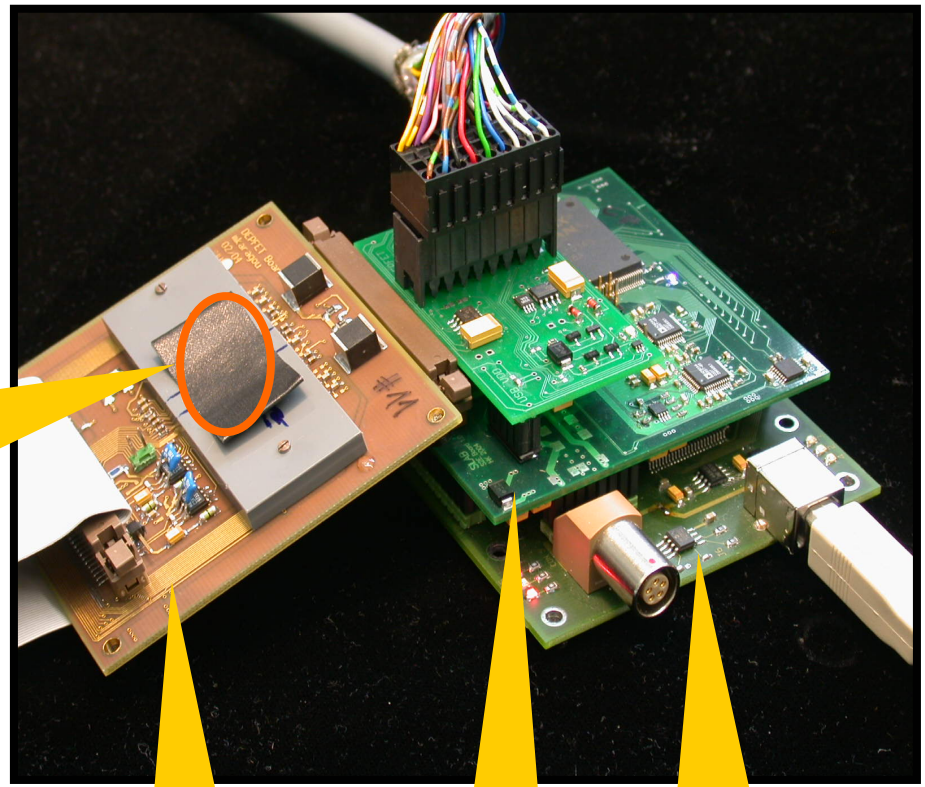
2x64 outputs with spare pads

Pads for daisy chain

control inputs

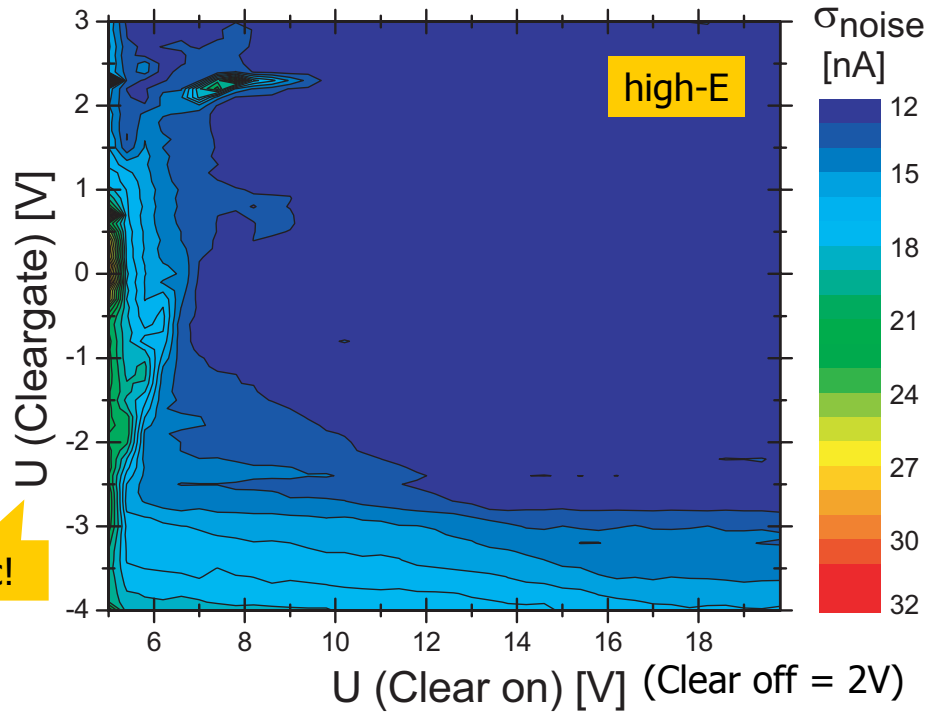
ILC Prototype System



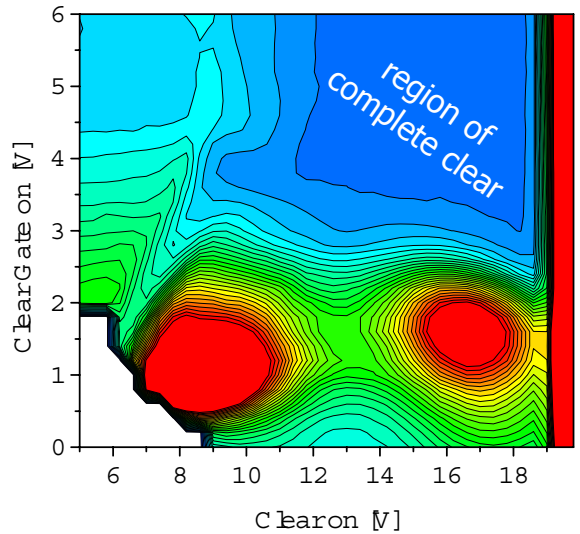


Example of device study: Clear Efficiency

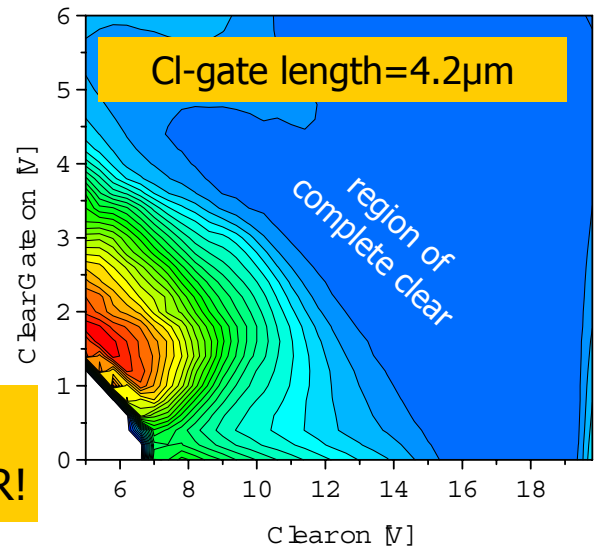
- Study mini matrix devices in laser setup
- Plot pedestal variations ('noise'). If they are constant, clearing is complete!
- Study various designs (high-E, no high-E), geometries (length of clear gate) and operating conditions (static or clocked clear gate)



Cl-gate length=7.2µm



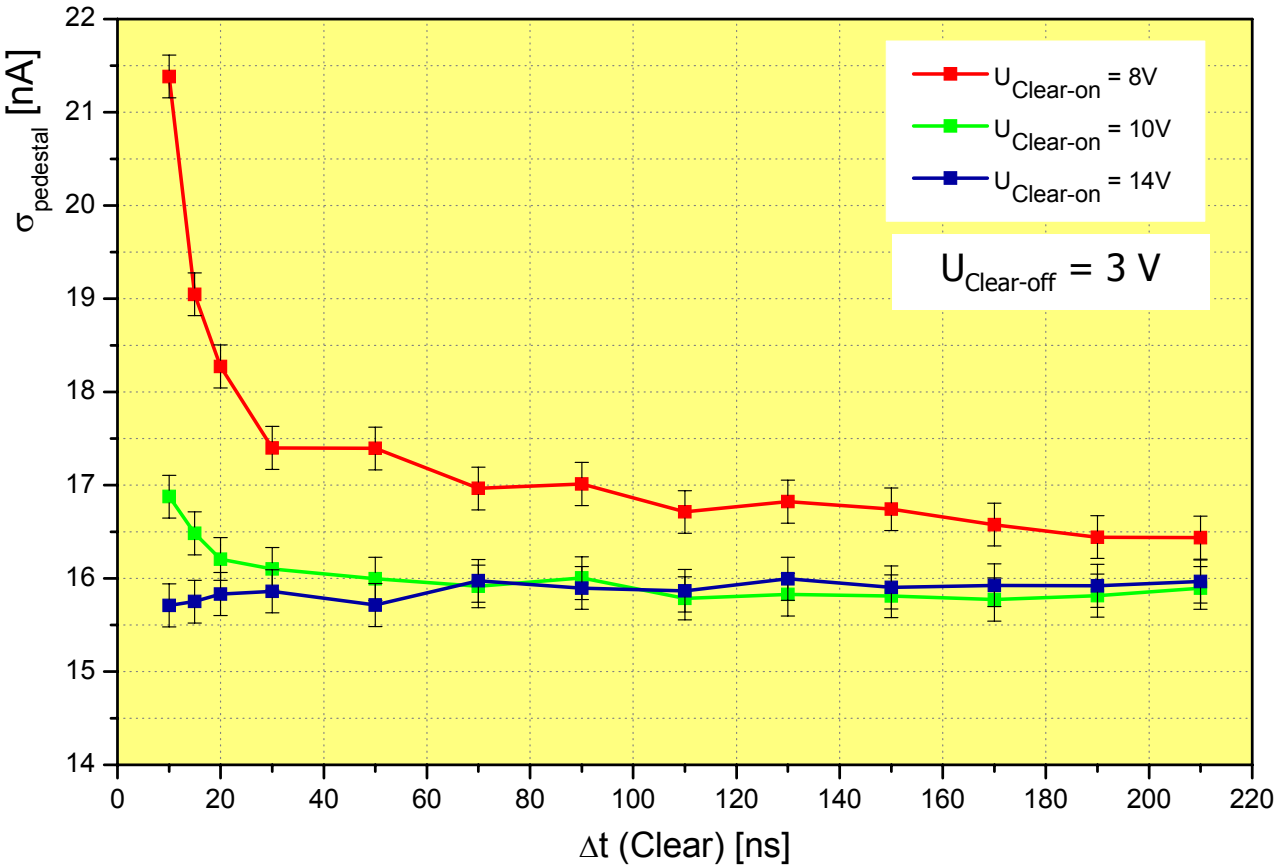
Cl-gate length=4.2µm



Complete clear achieved with static clear gate !
Required voltages are small (5-7V) – very important for future SWITCHER!

Fast Clearing

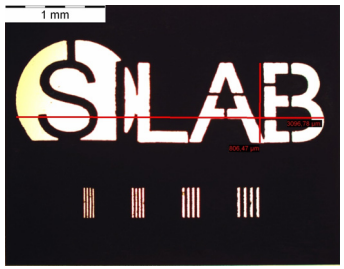
- Study clear efficiency for short clear pulses
- device has common clear gate, High-E



Already existing devices provide complete clear in only <10ns…20 ns @ ΔV_{clear} = 11-7 V

ILC DEPFET-System in the Lab

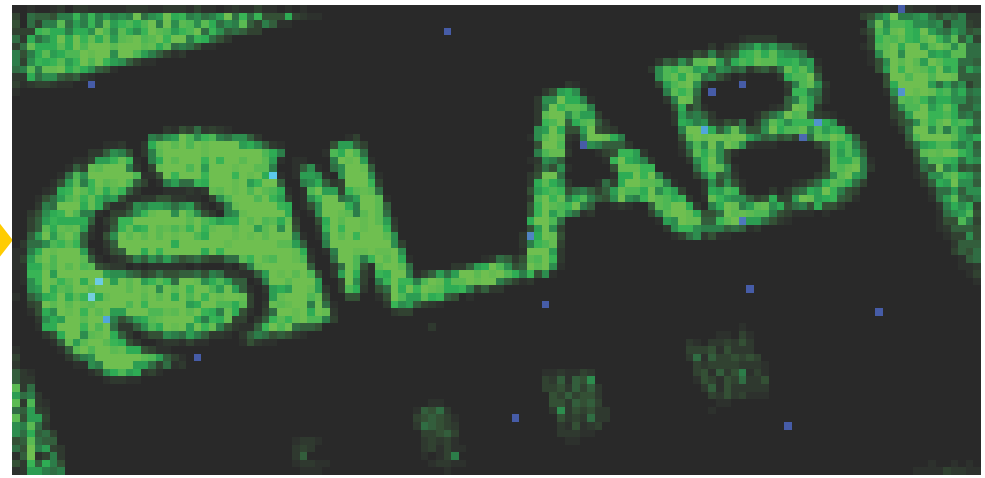
10µm thick Tungsten-Mask

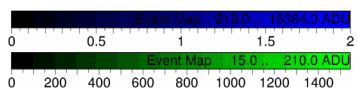


2.7 mm

3.4 mm

irradiation with ^{55}Fe
(6keV γ, 1700 e^-)





13keV...1MeV

1keV...13keV

ILC system performance in the lab:

- **High speed**: row rate: 0.6 MHz
- **Noise: 230 e^-**

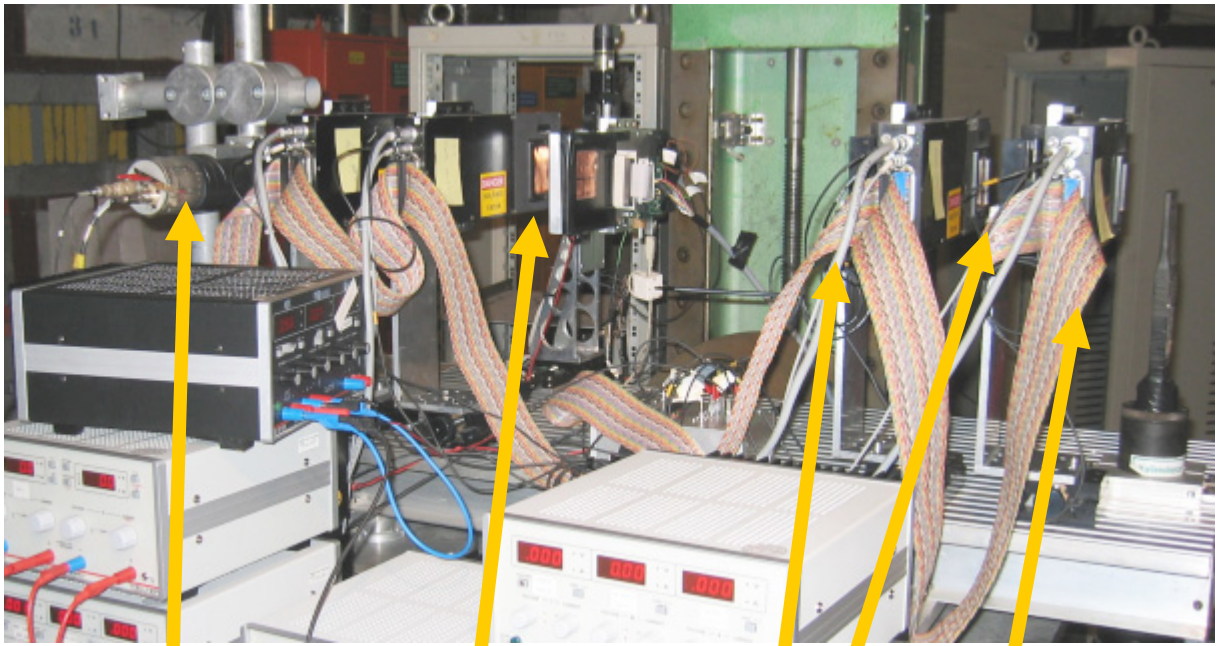
Noise contributions:

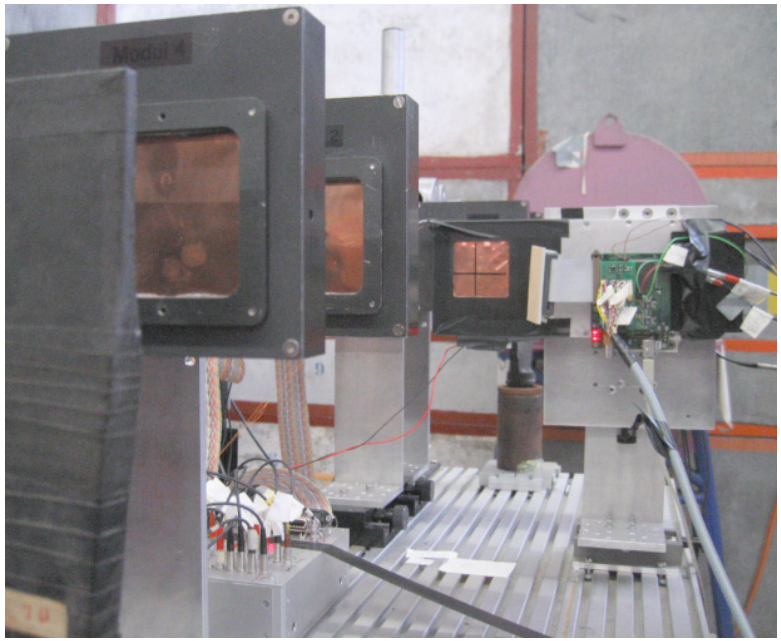
~ 100e- from CURO etc.

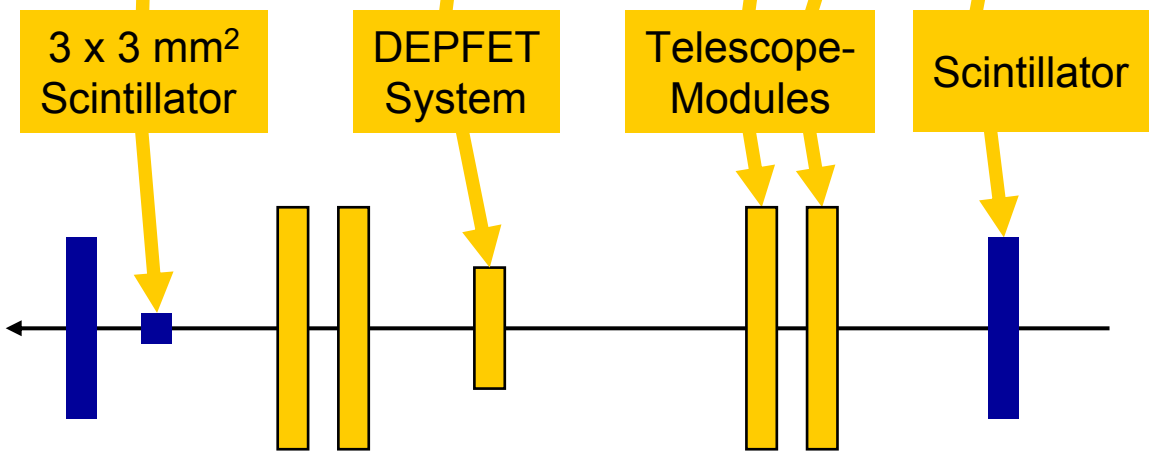
~ 60e- from I2U converter (CURO → ADC)

~ noise pickup of I2U converter

Test Beam Setup (@ T24, DESY)



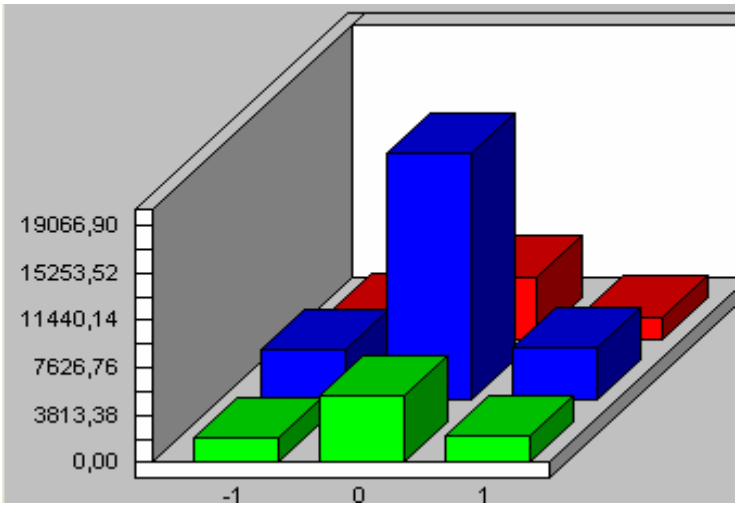




- Two test beam at DSEY
- Electrons @ 4GeV
- Reference telescope:
  4 Si-strip planes (pitch in x- and y: 50µm)

- Two matrices have been tested with
  4 x 128 pixels of 36µm x 28.5µm
- Sensor is 400µm thick!

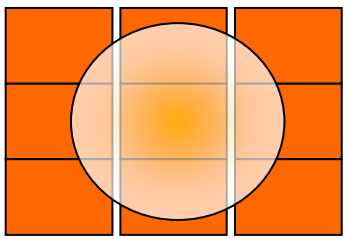
Preliminary analysis: Average cluster shape



PH averaged over all clusters

2030	5388	2220
4101	19793	4188
2031	5009	1920

Pixel-shape is not a square

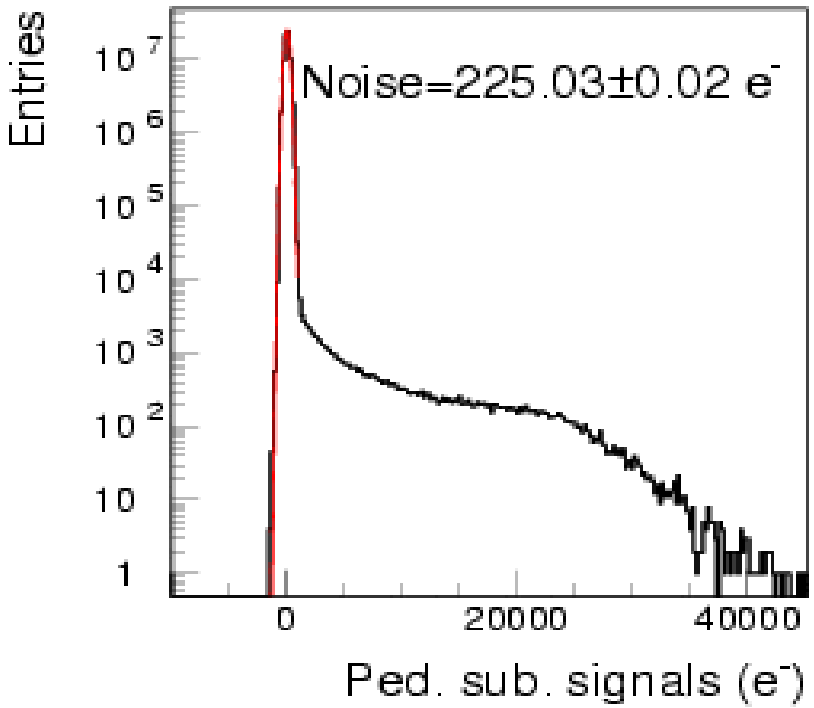


Charge in adjacent
Y pixel > X pixel

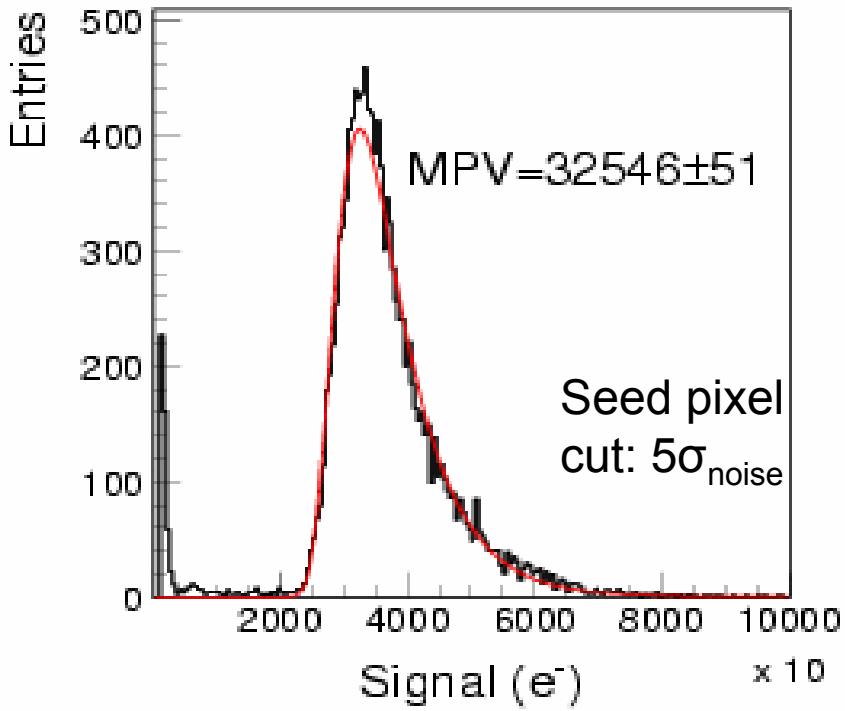
- Asymmetry (2% in x, 7% in y) not yet understood
- clusters are wide because sensor is thick and bias voltage was set rather low.

Noise and Signal

- Readout with 1µs sampling time per row, slower readout
- Data analyzed in a small area only so far
- Signal / Noise = 144

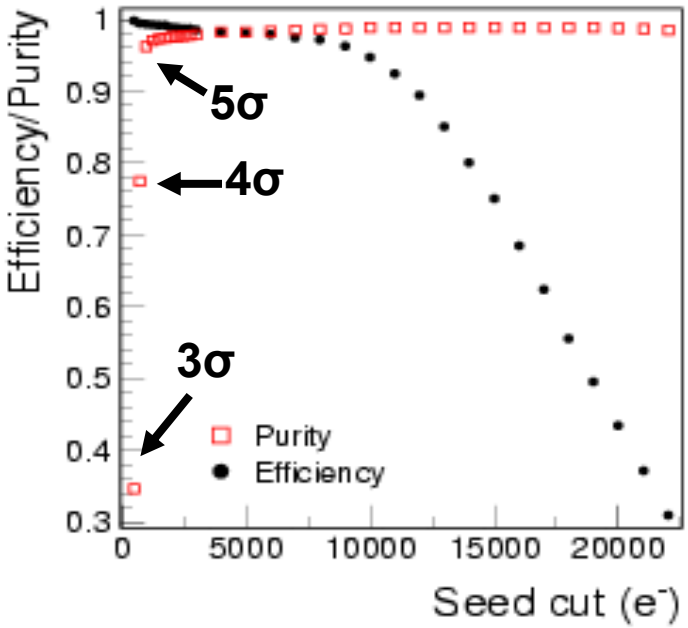


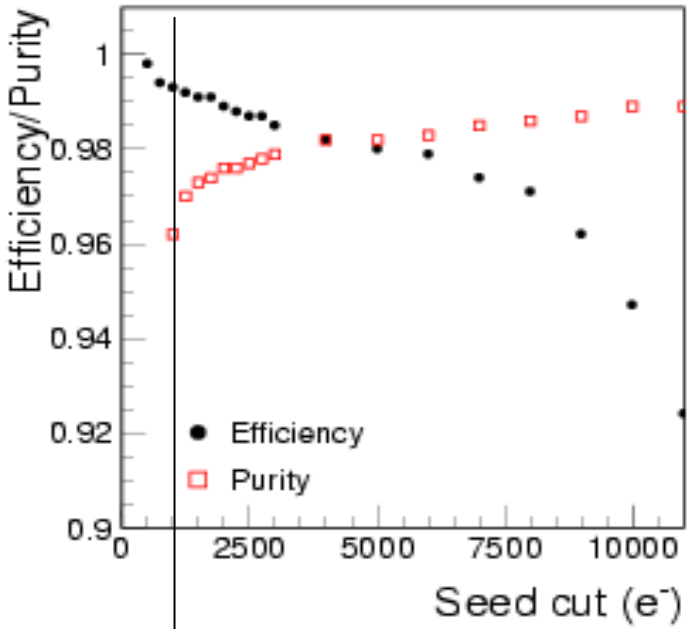
Noise ~230 e



Nice Landau Distribution

Efficiency vs. Purity





Efficiency = $\dfrac{\text{Number of tracks with cluster}}{\text{Total number of tracks}}$

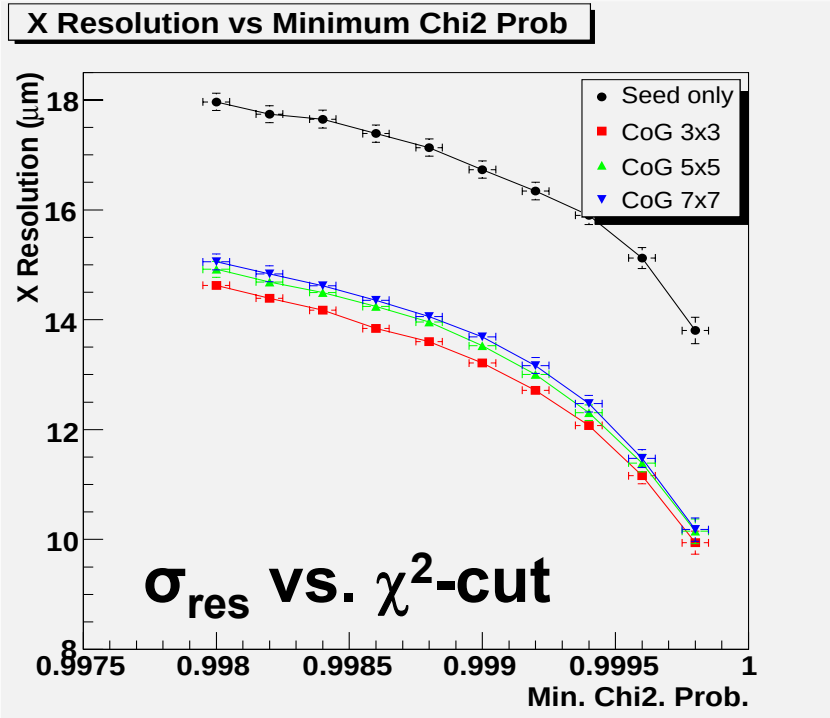
Purity = $\dfrac{\text{Number of clusters with track}}{\text{Total number of clusters}}$

For 5 σ seed cut (1125 e⁻)

- Purity ≈ 0.963
- Efficiency ≈ 0.993

Spatial resolution

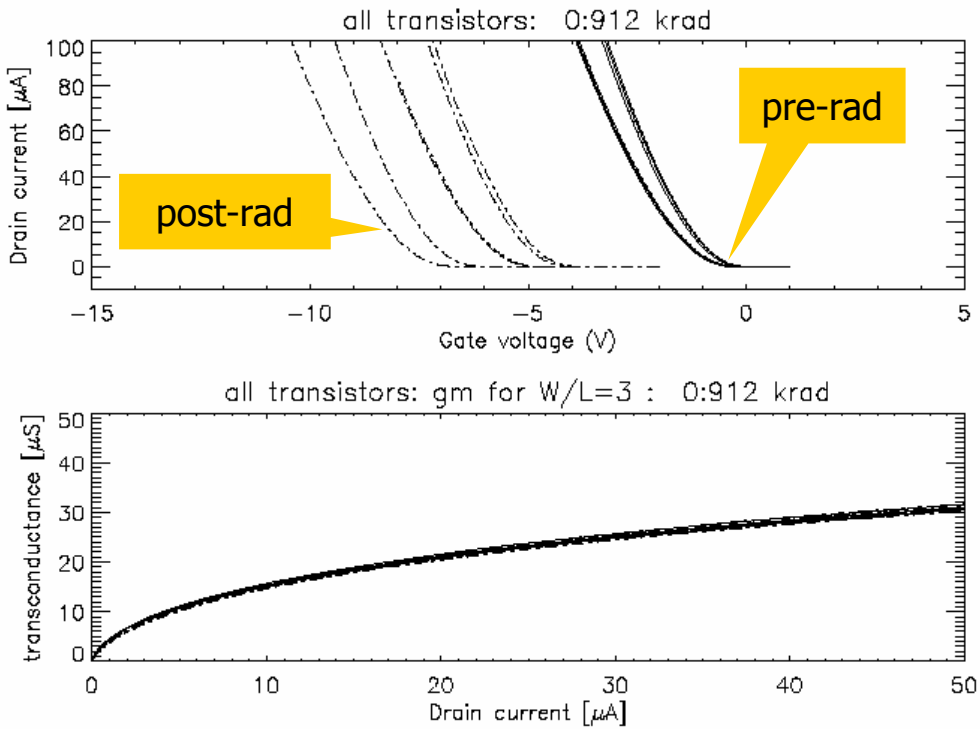
- Due to low energy beam, multiple scattering limits spatial resolution
- Telescope position prediction in DEPFET plane has ~11µm error
- Expect better measured resolution (DEPFET position – extrapolation) for very straight tracks:



- Remember: Pixel size is 36µm x 28.5µm. Will be ~ 24µm x 24µm soon…
- Resolution for thin sensor will depend on track angle etc…

Irradiation of Single Pixels

- Crucial question: Threshold shift of the (external) MOSFET (oxide thickness ~200nm)
- Irradiations with ^{60}Co and Xrays (~17keV,Mo) up to ~1Mrad



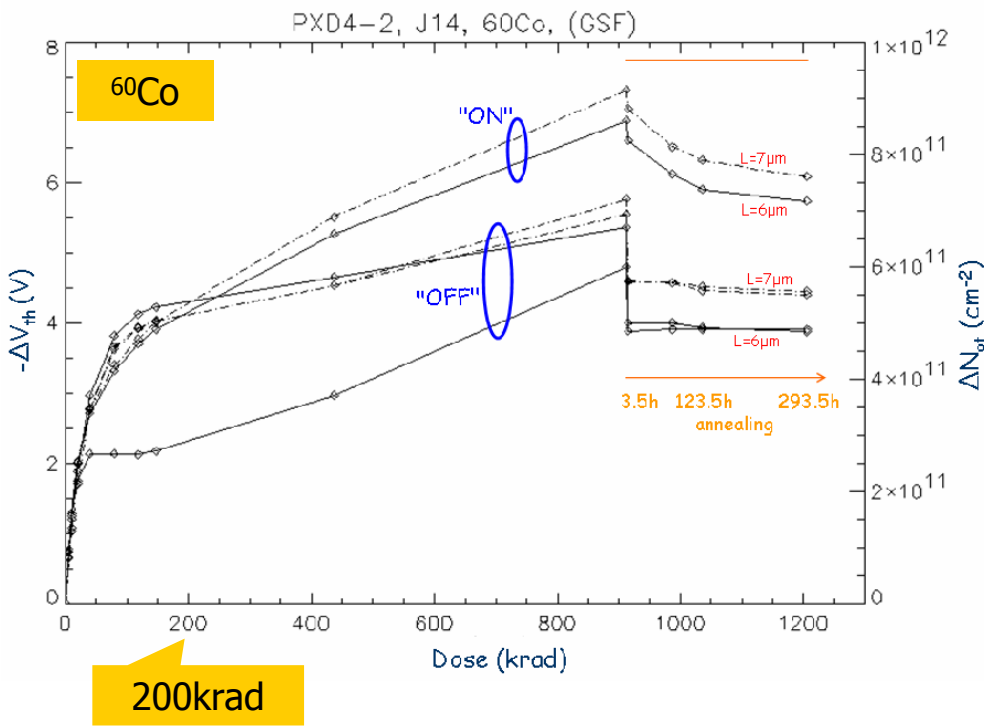
drain current vs. gate voltage

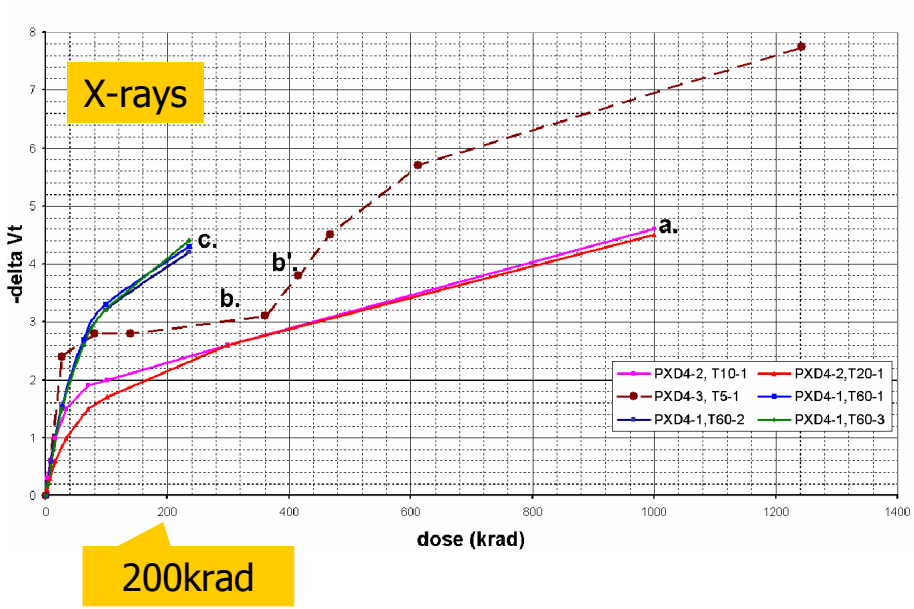
transconductance vs. drain current

- Threshold shifts are negative, as expected from positive oxide charge
- This can be compensated for by variation of bias voltages
- Transconductance remains unchanged ⇒ noise should not degrade. This has been confirmed by direct measurement.

Effect of dose rate / annealing

- **Shifts are small**: only - 4...- 6 V
- Observe saturation after 200 krad
- Device 'off' state is slightly better – good: this is where devices are operated most of the time!





- But: possible explanations for these good results need to be confirmed

Conclusion

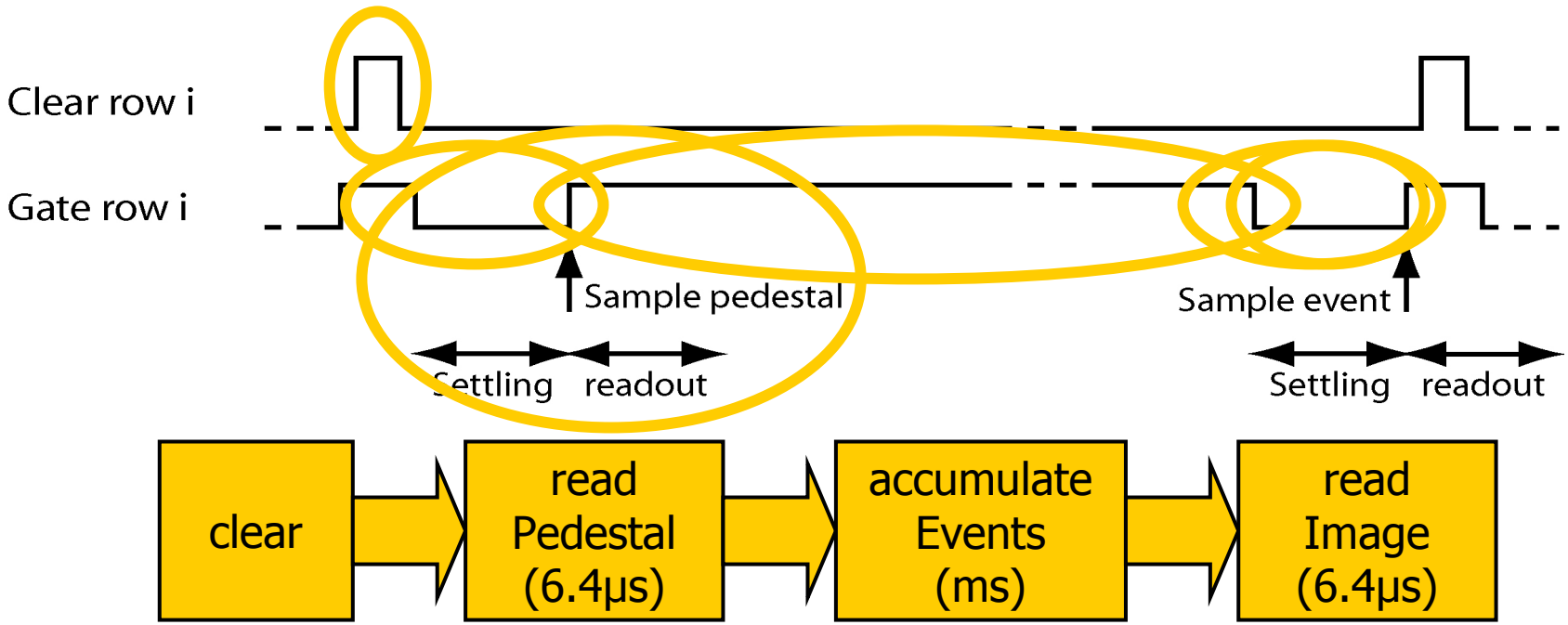
- Achievements:
  - Technology for thin ($\leq$ 50µm) detectors established (total budget of sensor 0.11% X_0)
  - Present Pixel size: 24x33 µm^2 – can go to ~ 20x20 µm^2, limited only by manufacturing equipment !
  - Complete clearing works with short (10ns) clear pulses at moderate voltages. No need to clock clear gate !
  - Radiation tolerance (threshold voltage shift) demonstrated up to 1MRad !
  - System operated in test beam with 240e noise at '1 MHz'

- Advantages DEPFET
  - Charge collection in fully depleted bulk with high charge collection field. Charge is not shifted.
  - High S/N (~40 at 100e noise), high spatial resolution (expect ~2µm)
  - Low *average* power dissipation for full ILC system (4W, dominated by CUROs. Benefit from 1:200 cycle @ ILC)
  - Fast readout should be possible (some 10 MHz)
  - Low material

- Next steps
  - Irradiate chips and full system – is underway
  - Operate complete system at full ILC speed
  - Decrease matrix noise
  - Produce thin sensors with larger matrices
  - Design new SWITCHER (lower voltage operation, smaller chip, radiation hardness) – is underway
  - Design new CURO (deeper FIFO, standby mode, ADC?, …)

Spare: Readout cycle with incomplete clear

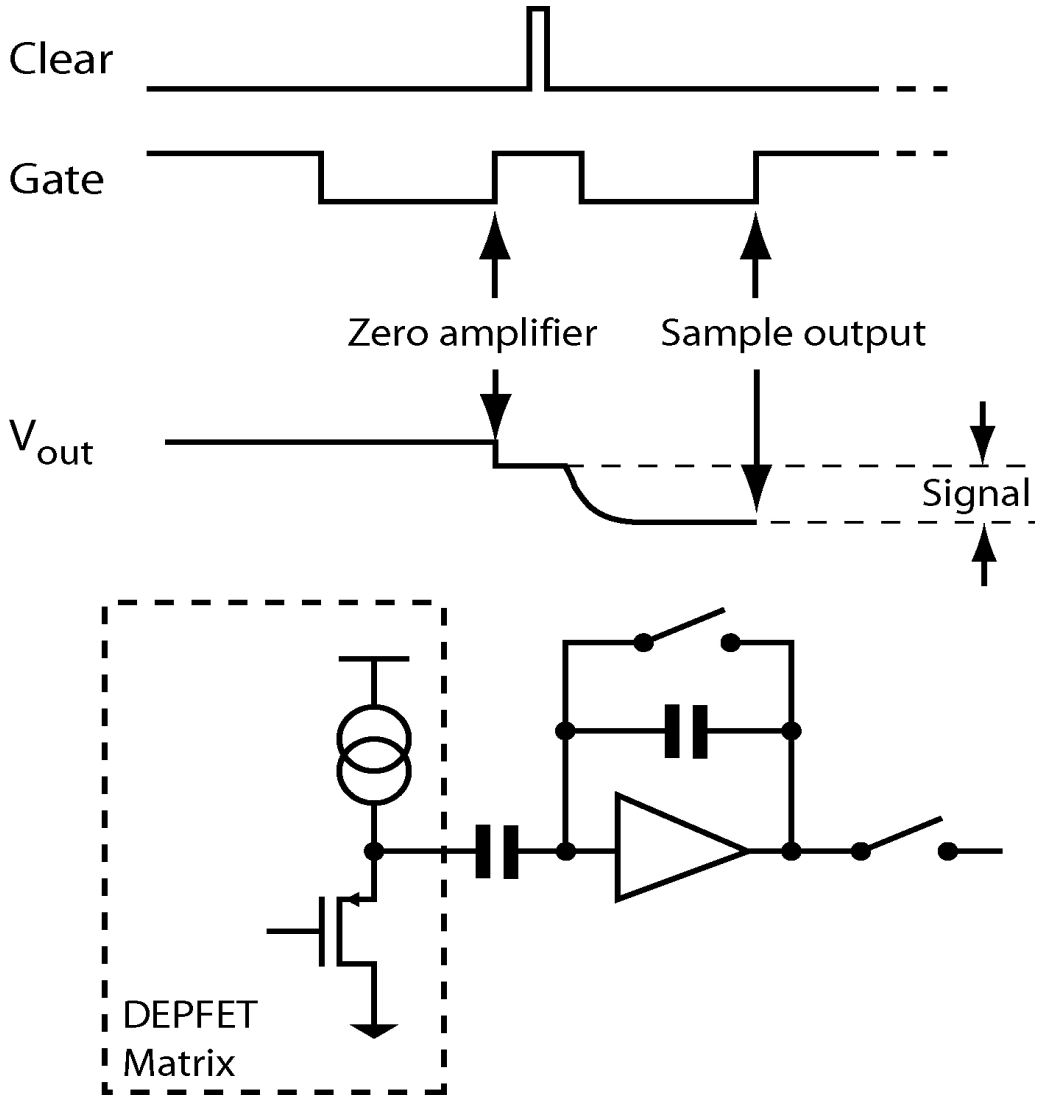
- Depending on device geometry, clearing of the internal gate can be incomplete.
- The remaining charge fluctuates, causing 'reset noise'
- Therefore, a pedestal value must be recorded directly AFTER the clearing.
- Result is recorded just BEFORE next clearing



- Pedestal data must be stored for a long time – this cannot be done on-chip

Spare: Source follower readout

- Possible implementation:
  Voltage amplifier with reset
- This assumes that no large spikes
  are introduced on source during reset.
- DEPFET mismatch is no problem
- Possible applications:
  - X-ray astronomy (XEUS)
  - Autoradiography



Spare: Expected Power Dissipation

- For V_{Drain} = 5V and I_{Drain} = 100µA (conservative values): P_{DEPFET} = 0.5mW per *active* device

- **Layer1** (8 Modules x 2 sides x 512 = 8192 pixels), duty cycle = 1/200:

Sensor:	only active pixels dissipate power	⇒ 8192 x 0.5mW / 200 =	**20 mW**
SWITCHER:	6.3mW per active channel at 50MHz (measured)	⇒ 16 x 6.3mW / 200 =	**0.5 mW**
CURO:	2.8mW / channel (measured)	⇒ 8192 x 2.8mW / 200 =	**114 mW**
		Sum:	**~ 135 mW**

- Scaling up from 18.7 Mpixels (L1) to ~493 Mpixels for **5 layers** gives: **Total: ~ 3.6 W**

- **Note:** Largest dissipation (CUROs) is outside active area where cooling is less problematic!

- This calculation assumes that all chips can be switched into a stand-by mode with ~ zero power dissipation between bunch trains. This feature must be included in future chip versions.