Front-end electronics for the PANDA pixel detectors: a custom solution in 0.13 μm?

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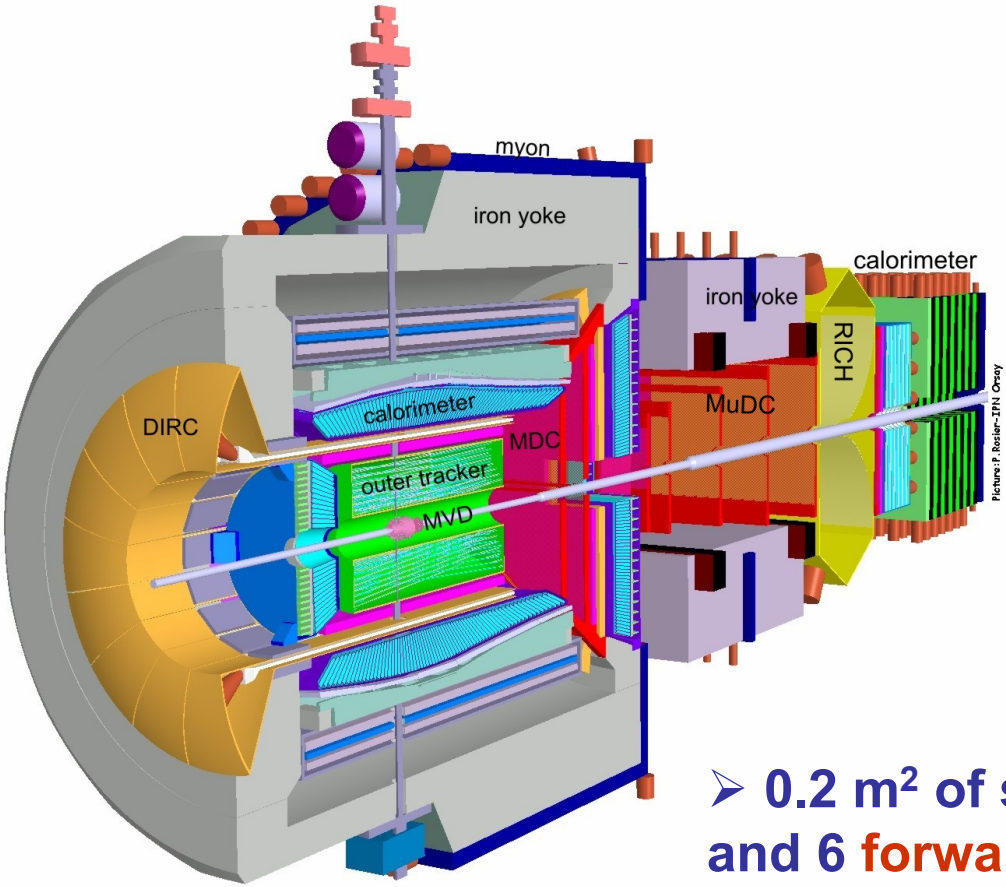
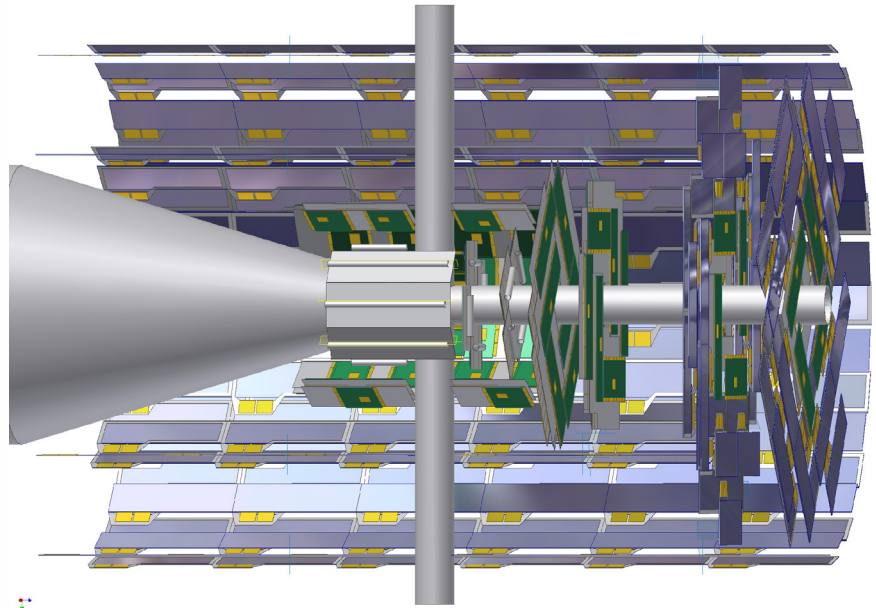
Outline

- The PANDA MVD: overview and requirements for pixels.
- Design options: “off the shelf” versus custom.
- Architecture of the custom solution: first considerations.
- Technology selection.
- R&D timeline.
- Summary.

The PANDA MVD





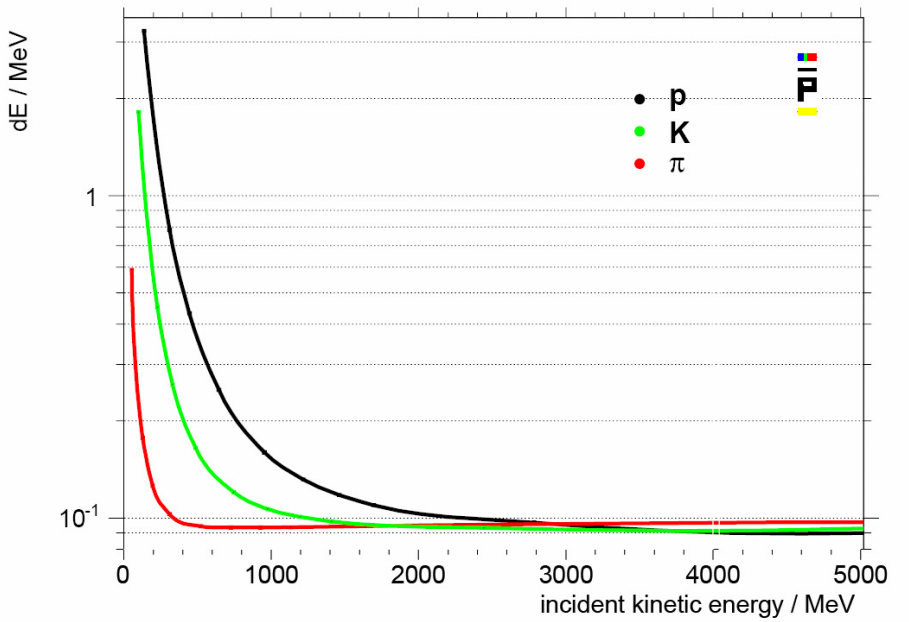
- 0.2 m^2 of silicon detectors: 4 **barrels** layers and 6 **forward disks.**
- 2 barrels and all disks equipped with **hybrid pixel sensors.**

Major constraints

- Annihilation rate: 10^7/sec.
- Low-momentum particles:
  - Low material budget
  - High dynamic range
- Analogue read-out for dE/dx PID (<700 GeV/c).
- Space resolution: better than 100 μm.
- Radiation tolerance (10^{14} n_{eq}/cm^2).
- Triggerless DAQ.

Dynamic range for dE/dx

- Assuming a 200 μm thick detector we can estimate:



- Minimum input charge: 7,000 electrons.
- Maximum input charge: 250,000 electrons.
- Full scale analogue resolution: 9.2 bits.
- Good overdrive recovery

Warning: amplitude distribution not taken into account!

Energy loss in 400 μm silicon as a function of kinetic energy (from the PANDA TPR).

Other numbers

- Recent simulations done in Jülich* about resolution and hit rate.
- Three different pixel sizes were compared:
  - ATLAS (50 μm x 400 μm → resolution: 84 μm (z); 75 μm (r, ϕ))
  - CMS (150 μm x 100 μm → resolution: 55 μm (z); 62 μm (r, ϕ))
  - Custom (75 μm x 75 μm → resolution: 48 μm (z); 52 μm (r, ϕ))
- The goal of a resolution smaller than 100 μm is always achieved. However a square pixel of 100 μm x 100 μm or less would give more safety margin and simplify the mechanics (with very asymmetric pixels orientation have to be changed in different layers).
- For the ATLAS chip (8 mm x 7.2 mm) maximum hit rates of 1.54 MHz/chip and 16 kHz/pixel have been estimated.

* T. Stockmanns, J. Ritman and A. Sokolov, "The Micro-Vertex-Detector of the PANDA Experiment at FAIR", presented at Pixel05, Bonn September 2005.

Possible options

- A lot of developments have been done by the LHC community, but:
  - ALICE chip purely binary.
  - CMS ROC has a too small dynamic range (2 MIPS).
  - ATLAS chip closest to the required specs.
- However:
  - the ATLAS module can not be used in a triggerless environment (module controller to be redesigned).
  - Asymmetric pixels complicate the layout and limit the resolution.
  - Performance at the required event rate in triggerless mode must be assessed.
- Room for investigating a custom solution.

Starting with architecture...

- Pixel size: 100 μm x 100 μm.
- Chip size: 13 mm x 15 mm.
- Chip active area 13 mm x 13 mm → 16384 pixels
- Data for each event
  - Pixel address (14 bits)
  - Time stamp (8-10 bits)
  - Amplitude information (8 – 10 bits)
  - Parity (1 bit)
  - Chip header (3 bits)
- Total: 38 – 40 bits per chip (80 differential pads).
- In 13 mm about 185 pads are possible, but power distribution on both sides preferable. Pad number can be reduced serializing data transmission at the expense of bandwidth or power consumption.

Data transmission

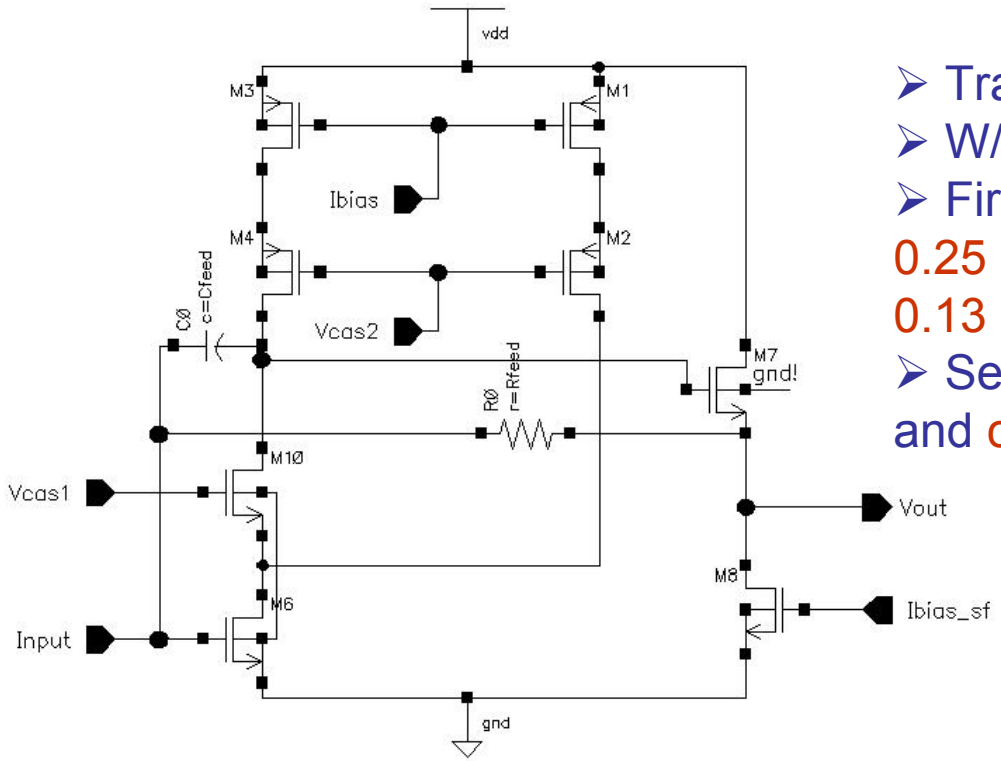
- Master clock of 50 MHz.
- Simple time domain multiplexing should be adequate.
- Four chips multiplexed on one bus.
- At each clock cycle one of the chips put on the bus either valid data (information of one pixel) or dummy data.
- Bandwith per chip: 12.5 MHz.
- Data are reorganized in the controller unit (dummy suppression).
- Output bandwith: between 1.5 and 2 Gbits/sec.
- More flexible architectures under considerations.

Technology

- The development will run for a few years: state of the art process.
- CMOS 0.13 μm seems the most appropriate choice.
- Gain in density with respect to 0.25 μm, expecially for digital parts:
  - Less power consumption for the same clock speeds.
  - Increased functionality at the pixel level.
  - Reduced dead area at the chip periphery (25% in the ATLAS chip).
- Some interesting features (ligthly doped substrate, triple well NMOS transistor...)
- Cost is an issue (600 k$ for an engineering run)

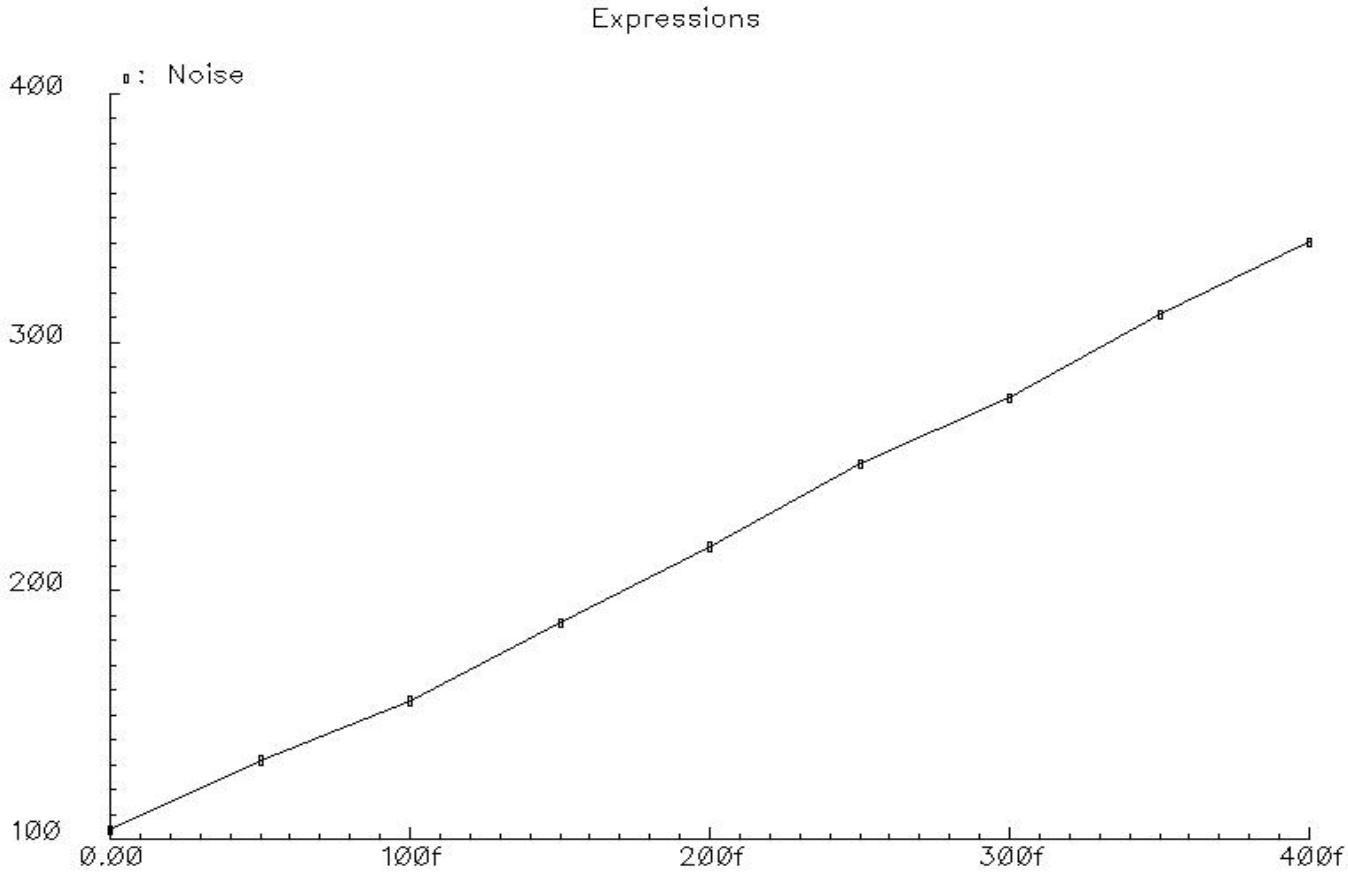
A simple example

- Same circuit simulated in 0.25 μm and in 0.13 μm.



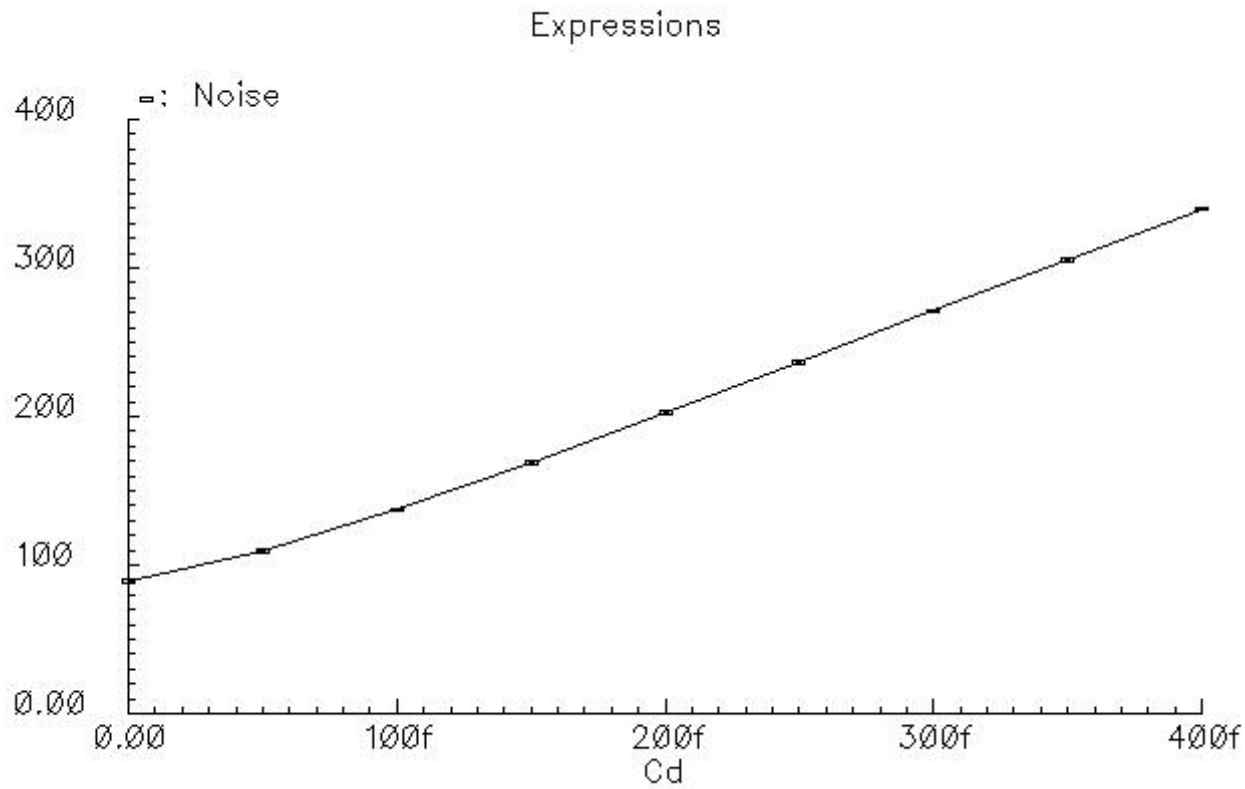
- Transistor length = 2 * Lmin.
- W/L kept constant.
- First simulation: circuit implemented in 0.25 μm at 2.5 V and circuit implemented in 0.13 μm at 1.5 V. Same power.
- Second simulation: same power supply and current in both amplifiers.

Simulated noise in 0.25 μm



Noise slop: 64 electrons/100 fF @ 7ns peaking time

Simulated noise in 0.13 μm



Noise slop: 68 electrons/100 fF @ 6ns peaking time

Some considerations

- With the same current in the input transistor, both circuits have basically the same performance.
- At the current level allowed in a pixel, transistors will be in weak inversion in any deep submicron process.
- The higher noise slope in 0.13 μm is easily explained with the faster peaking time.
- The faster peaking time is explained with reduced parasitic capacitance.
- Comparable analogue performance should be achieved in half the area.
- Dynamic range is an issue with 1.5 V power supply, but also the LHC pixel chip are operated with a reduced power supply to reduce power consumption.

From the literature

A New Prototype 10 μ by 340 μ Pixel Cell in a 0.13 μ CMOS Process for Future HEP Applications

Abder Mekkaoui,
Jim Hoff, Ray Yarema

Fermilab, Batavia, IL

- Work presented at the Pixel05 workshop by the Fermilab group
- Pixel cell: 10 μm x 340 μm.
- Power consumption: 80 μW/pixel.
- General purpose R&D design with several test structures.

From the literature

Pixel Cell Operating Conditions

Parameter	Value
VDDA	1.5 V
VDDD	1.5 V
IDDA	12 mA
IDDD	1 mA

Bias	Simulated	Measured
VBP2	1.066 V	1.04 V
VBN2	0.297	0.28
VBN1	0.374	0.364
VBBND	0.318	0.300

Power dissipation is around 80 uw/pixel cell.

The good correlation between simulated and measured bias voltages suggests that the models used for the pixel cells are good. (Also good noise correlation.)

Look at ENC and threshold characteristics for different columns.

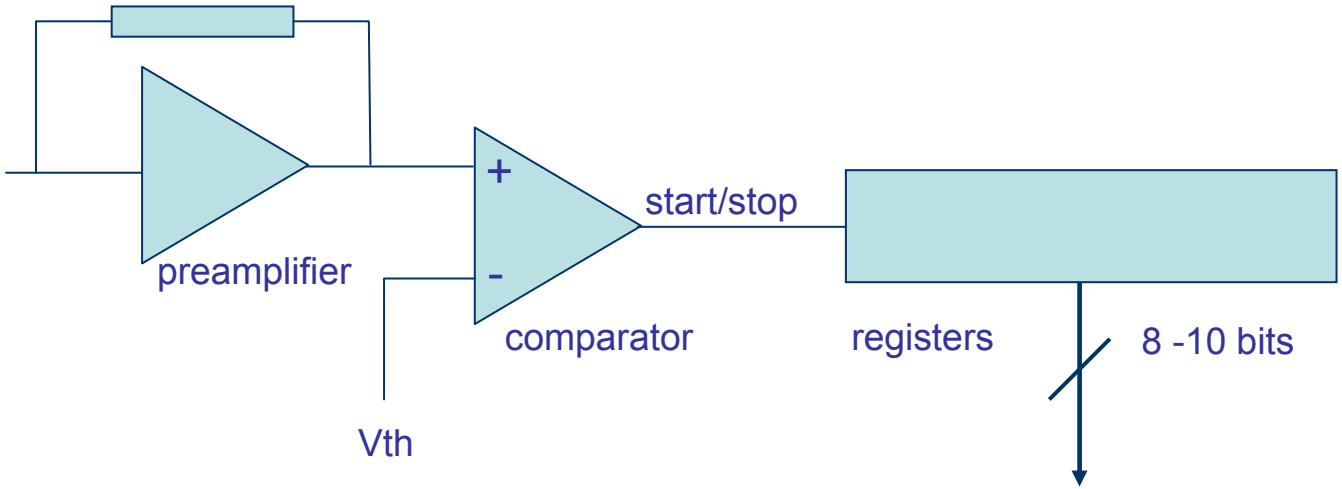
September 5, 2005 Pixel 2005, Bonn, Germany 6

- The authors observed good correlations between simulations and results

Possible R&D timeline

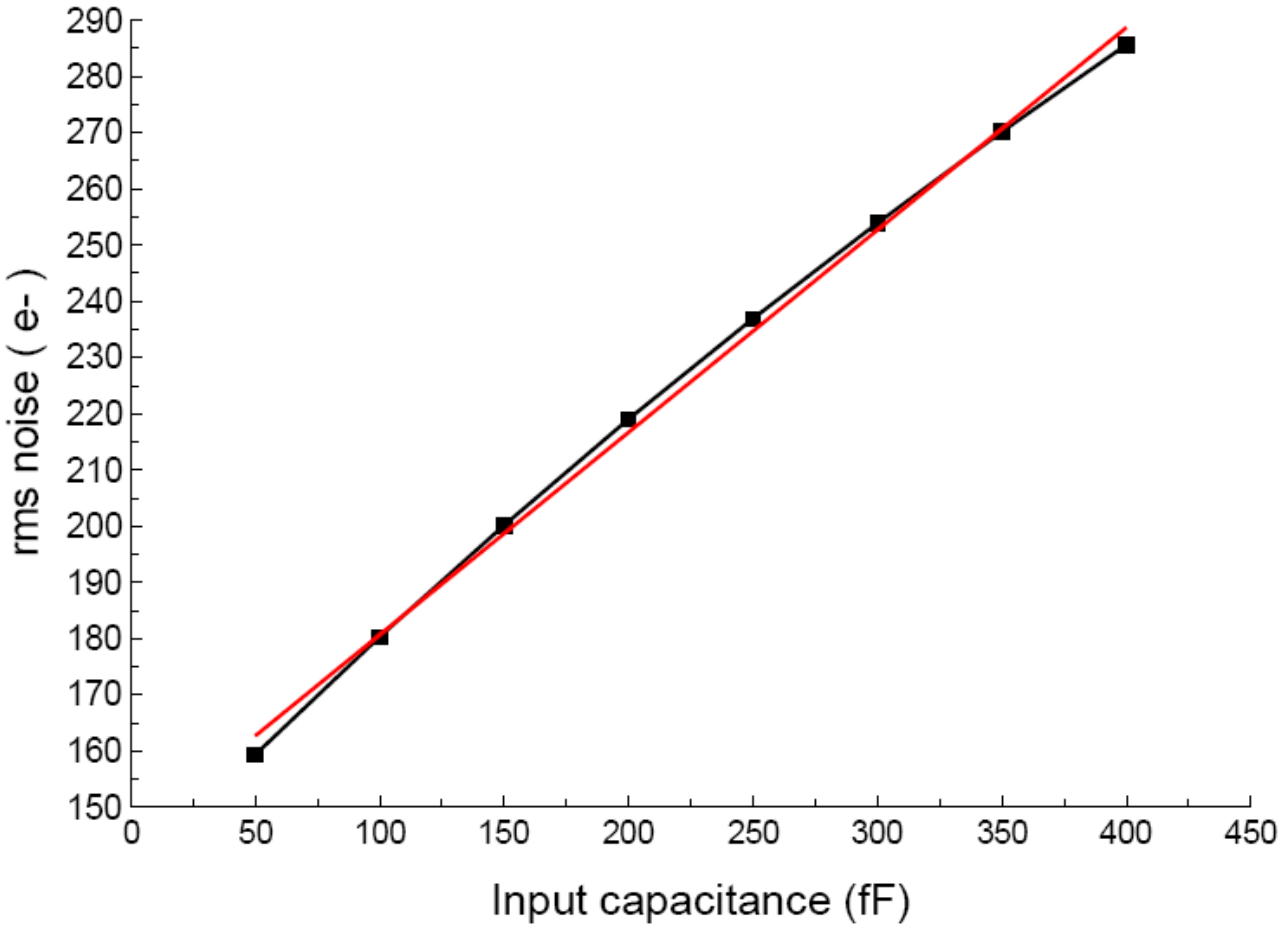
- Submission of first building blocks in 0.13 μm in December 2005.
- Submission of an array of complete pixel cells: December 2006.
- First reduced scale prototype: beginning of 2008.
  - Full functionality
  - Reduced number of pixel cells
- One additional prototype for bug fixing: end of 2008.
- FPGA based prototype of the control chip: 2006 – 2007.
- Prototype of the control chip: mid 2008.
- Engineering run: late 2009.
- More electronics is needed (optoelectronics components, detector control chip) but it may be re-used from other applications (semi-custom system).

First steps...

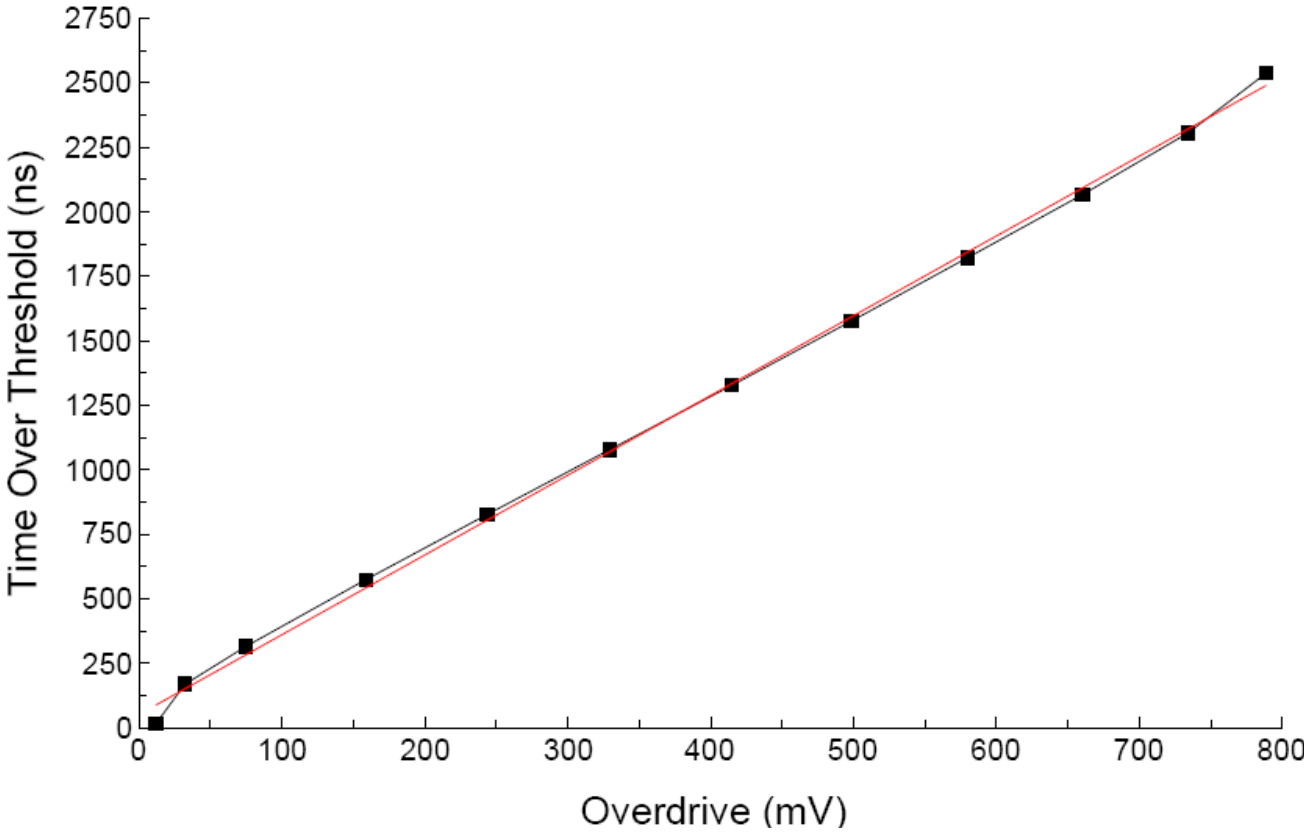


- Few pixel cells with different device options.
- Digitization with time over-threshold.
- Some read-out logic.

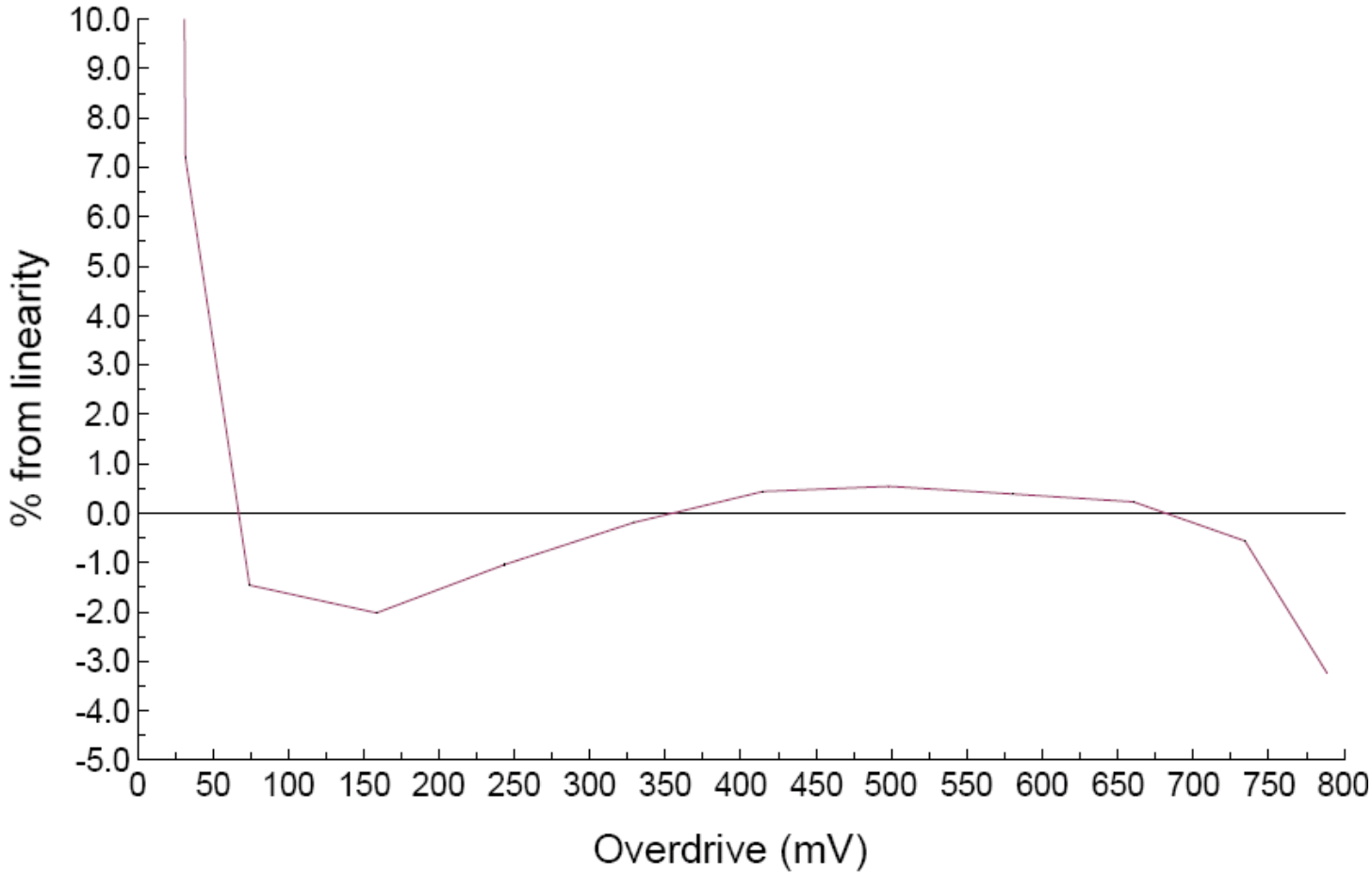
Noise


rms noise (e-)
290
280
270
260
250
240
230
220
210
200
190
180
170
160
150
0
50
100
150
200
250
300
350
400
450
Input capacitance (fF)

ToT


Time Over Threshold (ns)
2750
2500
2250
2000
1750
1500
1250
1000
750
500
250
0
0
100
200
300
400
500
600
700
800
Overdrive (mV)

Non-linearity

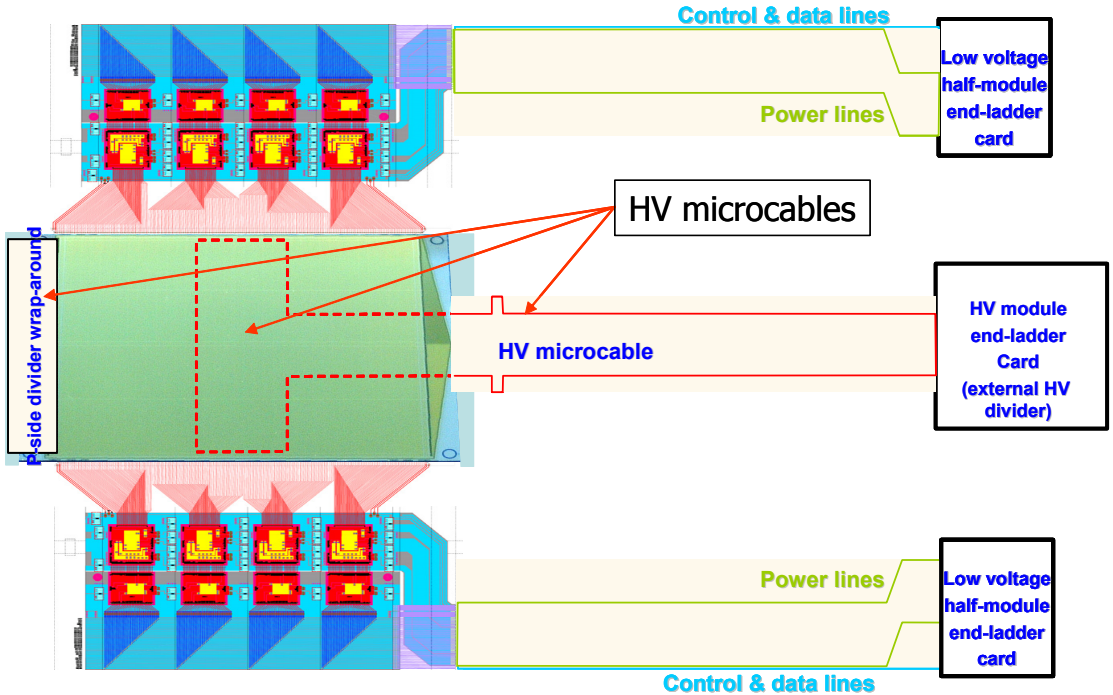


Thinning

- Material budget is critical for the MVD.
- Hybrid pixels are worse in this respect than MAPS or strips.
- State of the art: ALICE pixel detectors (200 μm sensor and 150 μm electronics).
- In principle, there is room for further thinning.
- In practice, the yield of bump bonding is the major concern.
- The issue needs to be addressed before the final approach is chosen.
- A dedicated effort is under discussion.

A system example

ALICE SDD system



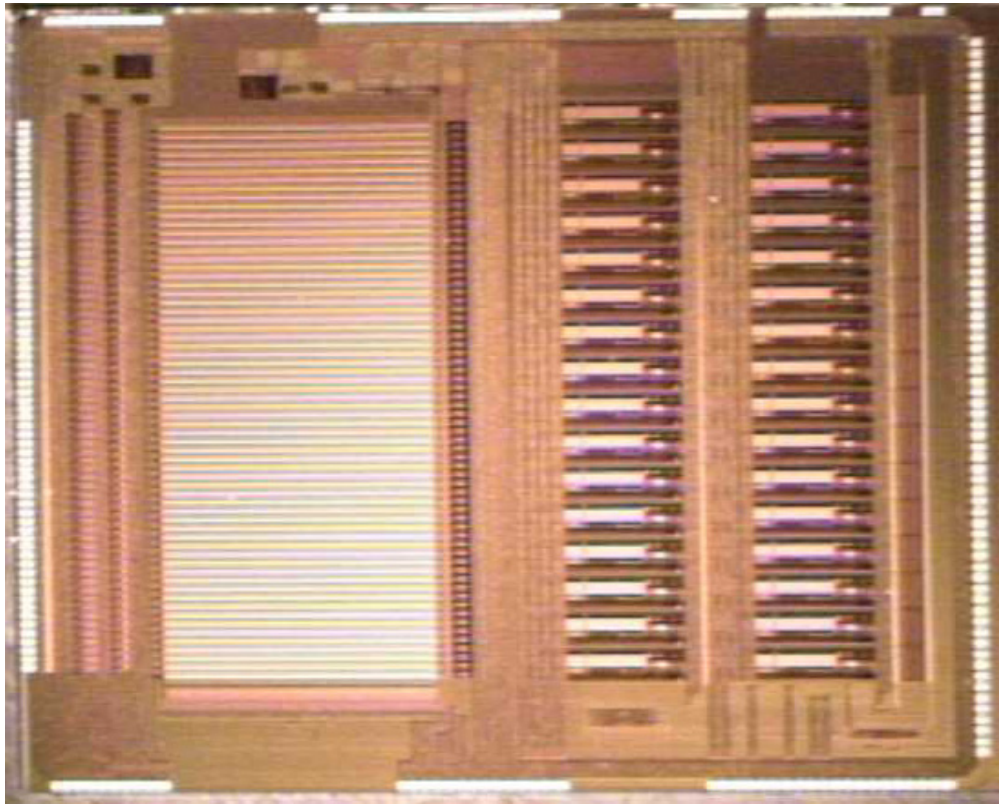
Custom for the experiment:

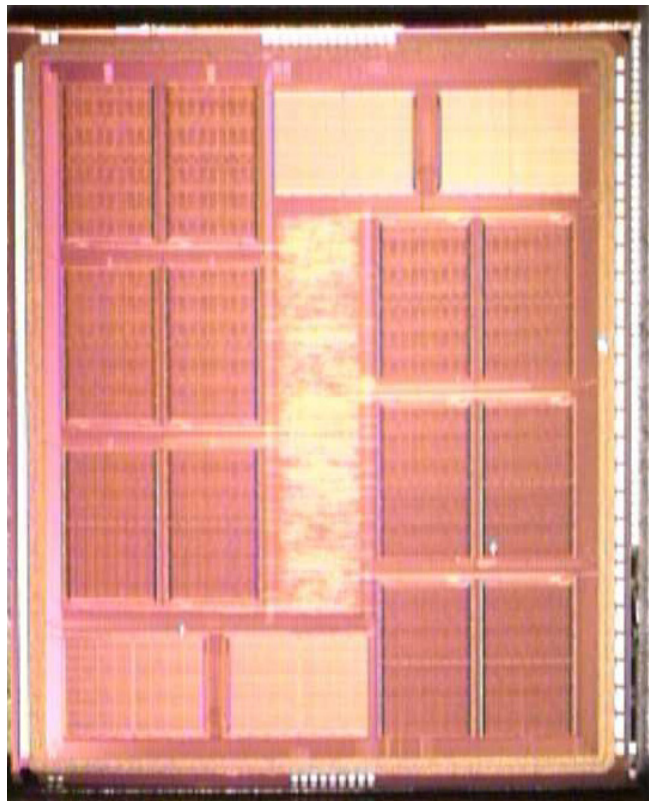
- Detector (INFN Trieste)
- FE electronics (INFN Torino)
- Data compression chip (INFN Bologna)

Re-used from other experiments (CMS)

- GOL (CERN)
- RX 40 (CERN)
- DCU (CERN)

ALICE SDD front-end





Mixed mode front-end chip:

- 64 channels
- 32 10 bit SAR ADC
- 40 MHz clock

Digital front-end chip:

- Baseline correction
- Multi-event buffering
- 40 MHz clock

Summary

- The design of the MVD is still evolving.
- First steps towards the design of a custom front-end being done.
- CMOS 0.13 μm could provide improvements in several area.
- The major concern is the cost, that can be reduced:
  - By sharing the same chips among different applications.
  - By sharing the same masks.
- The design of a complex ASIC is a lengthy process, but there is some time ahead.
- However, there are other aspects equally important to achieve good system performance (mechanics, cabling, cooling).
- Several of those issues can be addressed without the final electronics (dummy chips, etc.).