PADIWA Response Studies

Matthias Hoek

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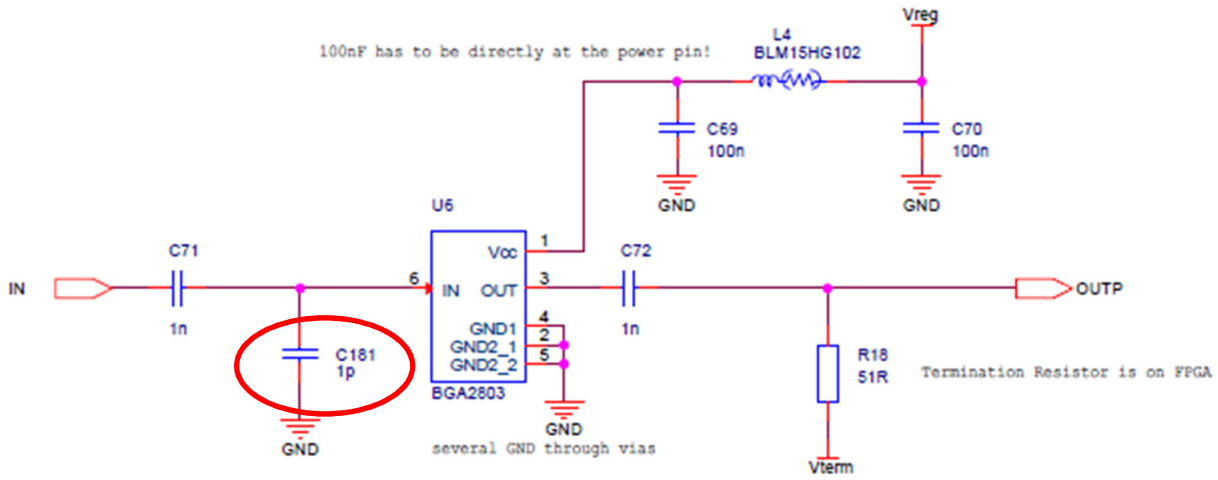
PADIWA Input Stage Modifications

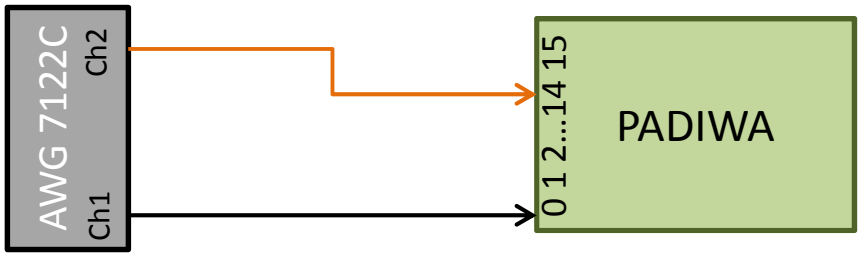
- Limit bandwidth to reduce noise
  - Standard 1pF (~3.2GHz cut-off)
- Study impact on timing
  - 1pF – 100pF selected (see table)

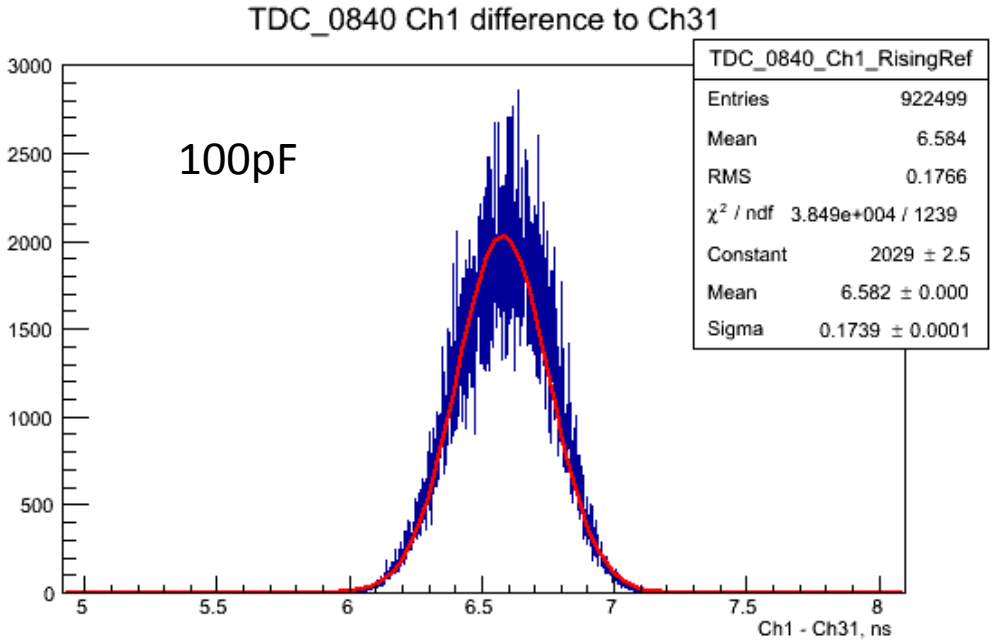


Input	Cap ID	Capacitance (pF)	Cut-off (GHz)
1	C196	1	3.2
2	C181	15	0.2
3	C182	1	3.2
4	C189	15	0.2
5	C183	2	1.6
6	C190	20	0.16
7	C184	2	1.6
8	C191	20	0.16
9	C185	4.7	0.7
10	C192	47	0.07
11	C186	4.7	0.7
12	C193	47	0.07
13	C187	10	0.3
14	C194	100	0.03
15	C188	10	0.3
16	C195	100	0.03

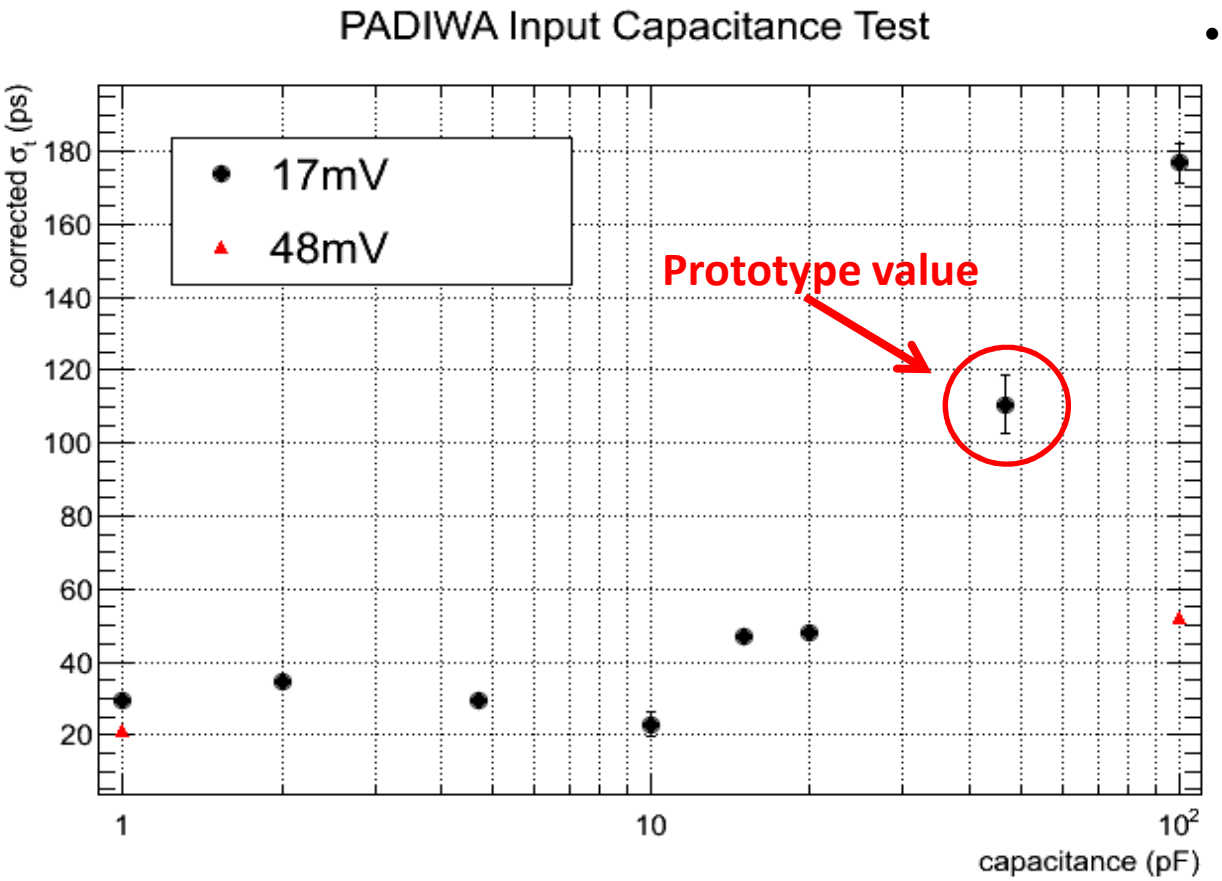
Test Setup @ GSI Electronics Lab

- Signal generator Tektronix AWG 7122C (GSI)
  - 10bit, 12Gs/s
  - 2 Channels (coupled)
  - Rectangular signal
- Signal properties checked with Tektronix DPO 7254 oscilloscope
  - Amplitude $-17.3 \pm 0.5mV$
  - Width $2.50 \pm 0.02ns$
  - Rise time $492 \pm 48ps$
- Procedure
  - PADIWA channel 15 as reference
  - Measure time difference between two channels
  - Extract width of distribution (Gauss)



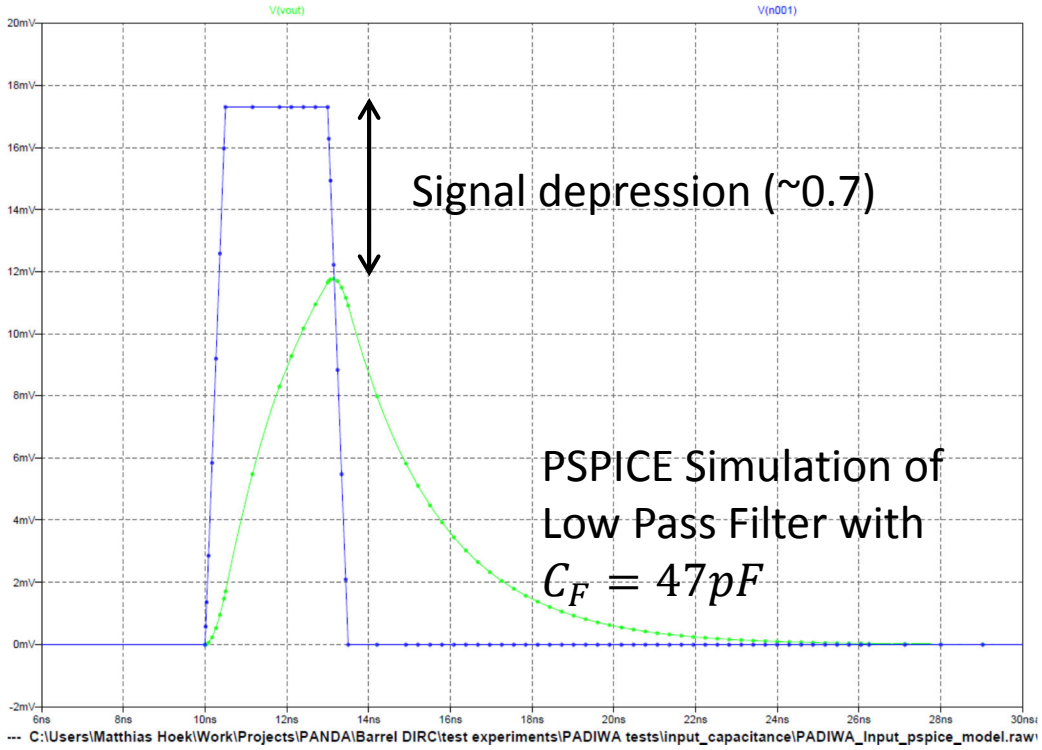


Results

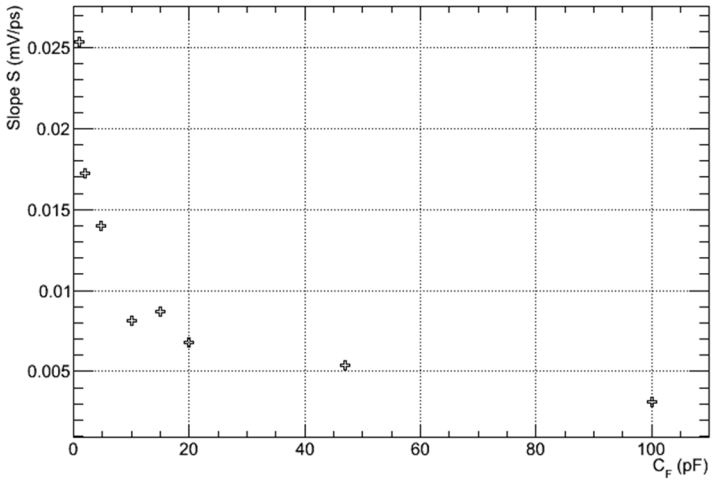


- Ideas on timing degradation
  - $\sigma_t \propto \frac{V_{noise}}{S_{signal}}$, with $S_{Signal} = \frac{\Delta V}{\Delta t}$
  - Slope decreases with C_F
  - Frequency behaviour of noise?
    - Must be low frequency
  - Test with larger amplitude
    - S_{Signal} increases
    - σ_t improves!

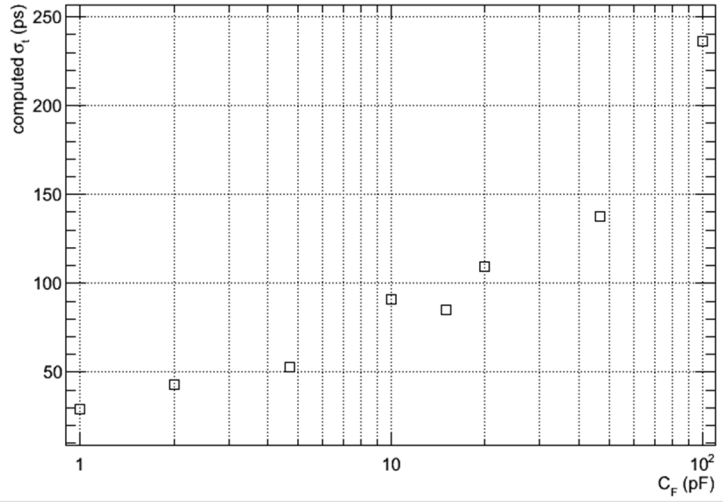
PSPICE Simulations



- Model Low Pass with PSPICE
  - Extract slope at 1mV level



  - Estimate required noise level
    - 0.75mV at 1pF
  - Compute jitter



Conclusions

- Clear dependence of timing resolution on capacitance observed
- Need better understanding of circuit properties
  - PSPICE simulations
- Investigate noise properties
  - Not pure White Noise
  - Must have low frequency component