Status of PASTA

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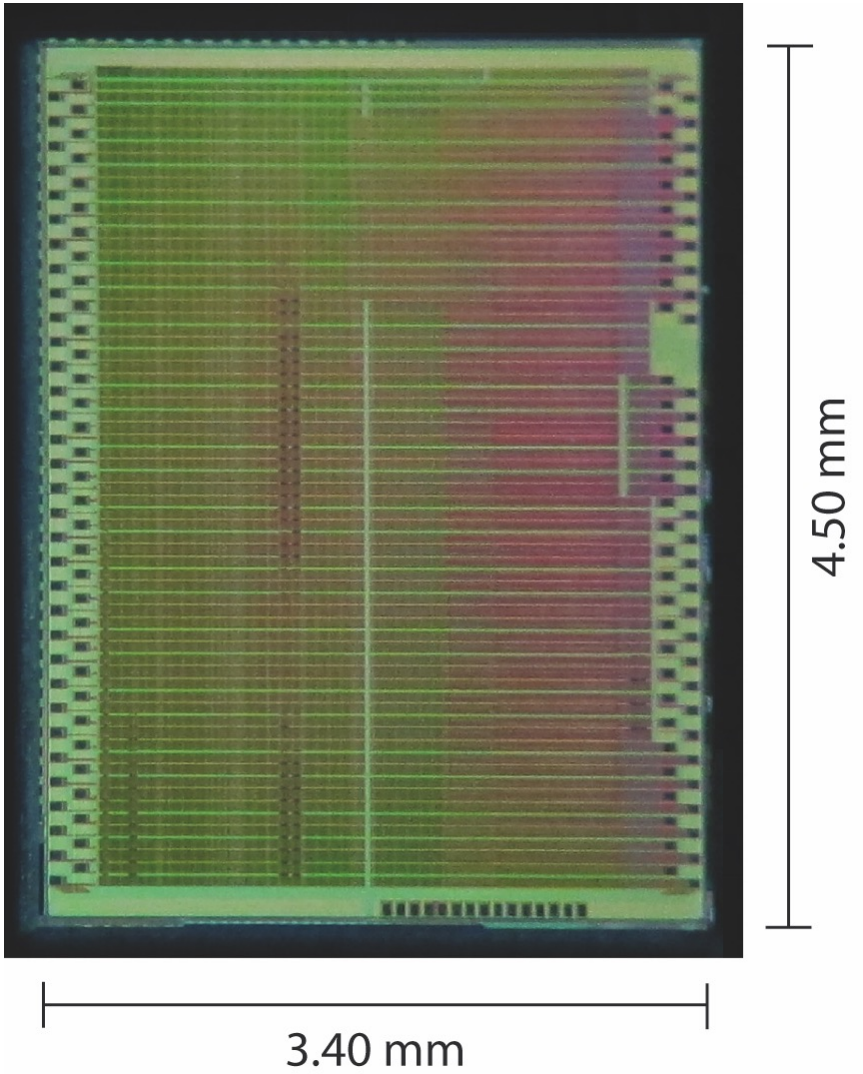
PANDA Collaboration Meeting
Vienna, November 30th, 2015

PASTA: PANDA Strip ASIC

- Current Status
- Perspectives
- Power test (slides from Robert Schnell)

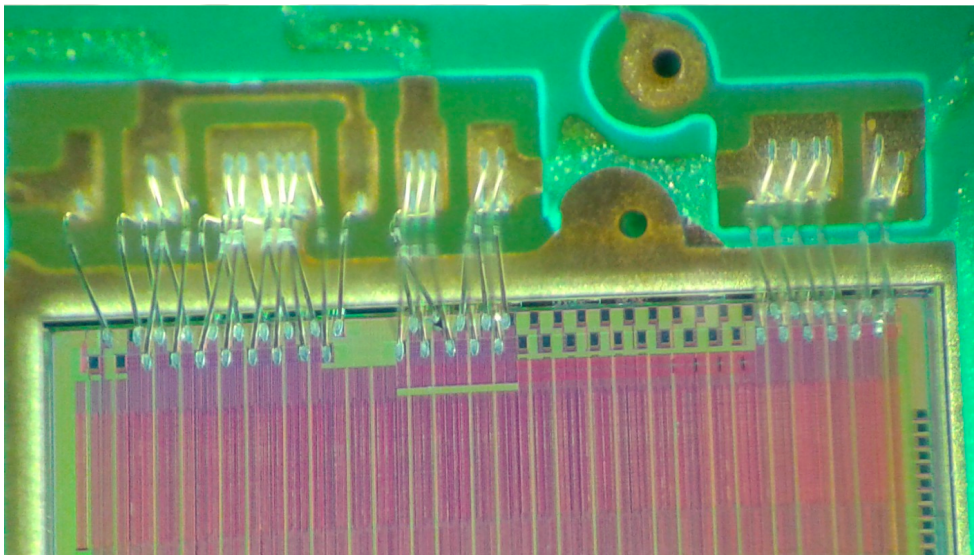
Current Status

- Chip submitted in April 2015 and received in September
- Chip manual in preparation
- First board for power and bonding test designed and produced
- Chip(s) bonded, first tests in progress



Perspectives

- Readout system (HW/FW/SW) under development (Gießen / Jülich) → lab tests
- Beam test at COSY planned in 2016
- Radiation hardness test: no information on this technology available! TID and SEU tests required



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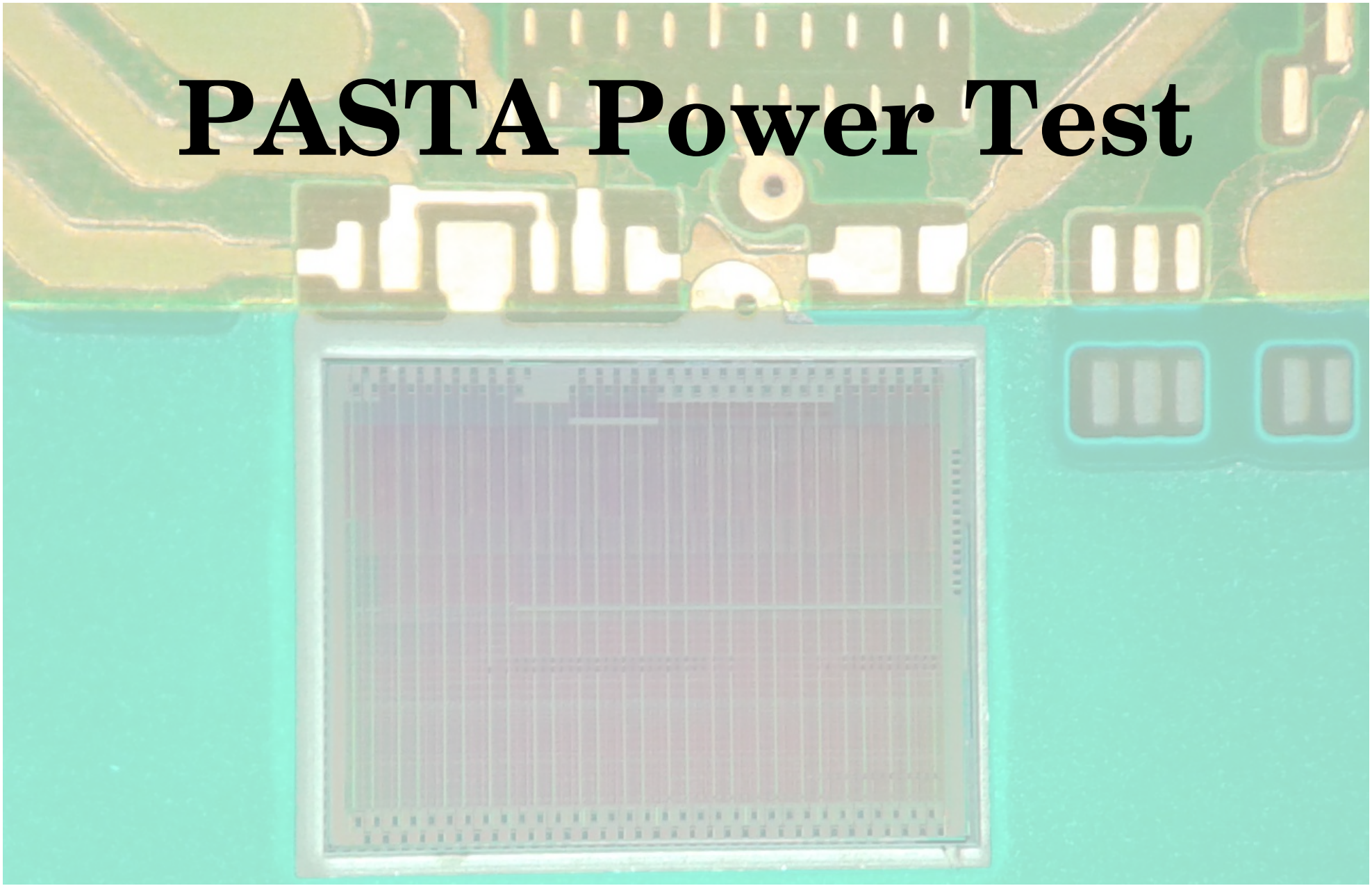
PASTA Power Test

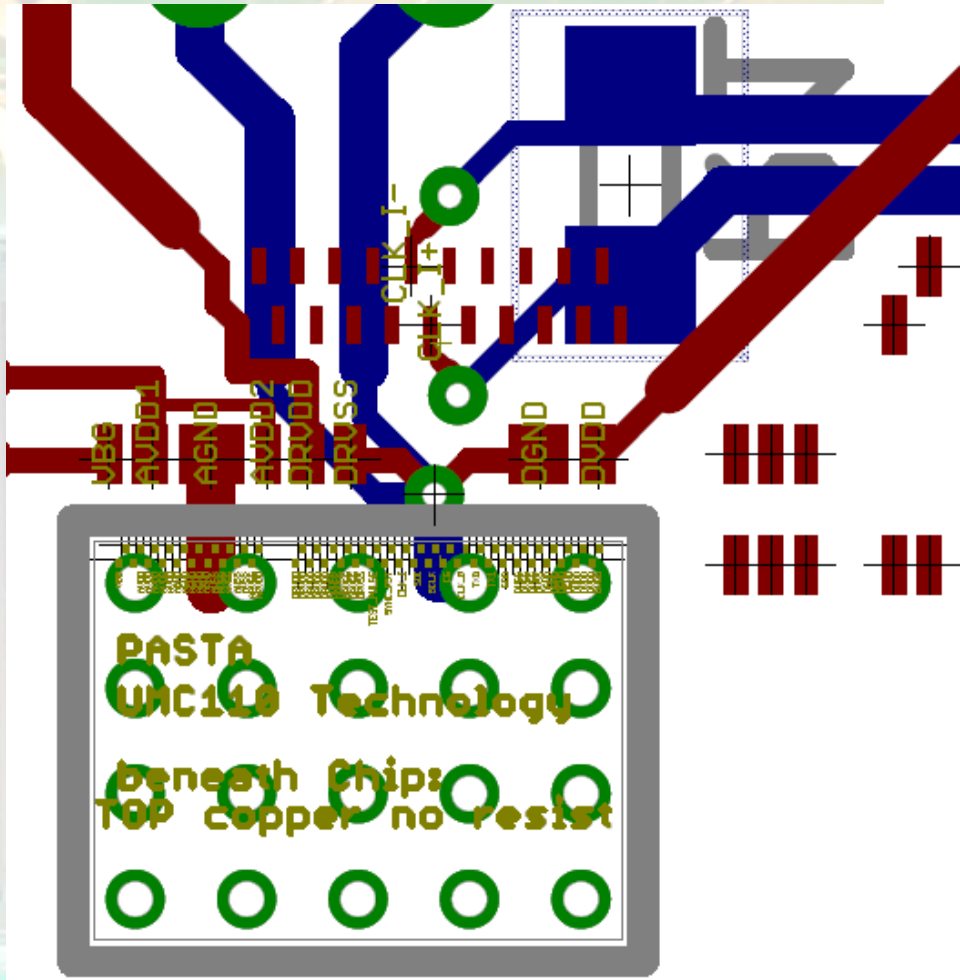


LV. PANDA Meeting, Vienna – Nov/Dec 2015

Power Test Board

- Board serves 2 test cases – Powering and Bonding

- Powering
  - bond pads for all voltages
  - one reference - VBG
- Bonding
  - test bond pads for all I/O's
  - arranged according to advanced PCB specs (75µm line width)
- I/O connection
  - one differential pair to connector
  - line termination available
  - intended for clock input

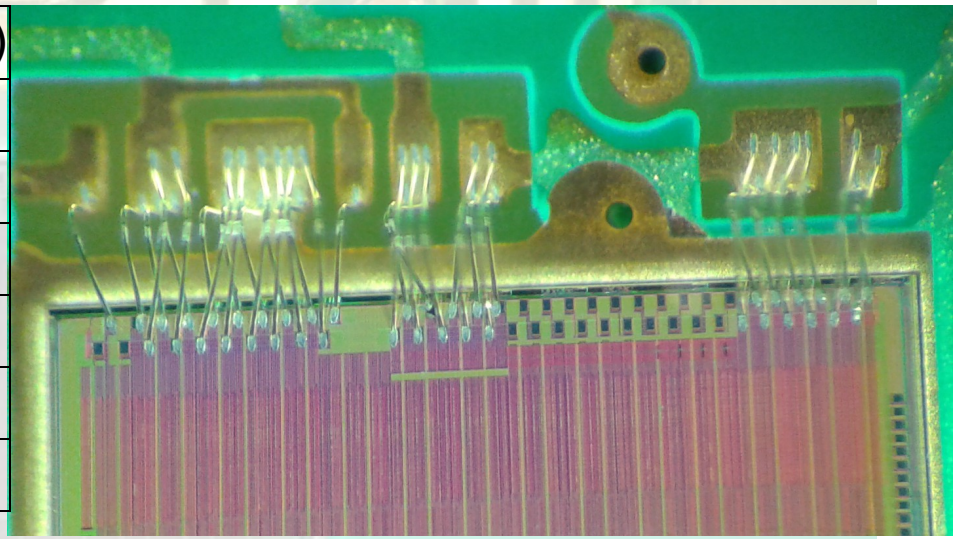


Results Test Board "P1"

- Voltages bonded: AVDD, DVDD, DRVDD and VBG

- Currents

event	I(AVDD)	I(DVDD)	I(VBG)	I(DRVDD)
AVDD on	10.5 mA	-	-	-
DVDD on	6.0 mA	0.3 mA	-	-
VBG on	50.5 mA	0.3 mA	0.0 mA	-
DRVDD on	50.5 mA	0.3 mA	0.0 mA	limit
DVDD off	89.5 mA	-	0.0 mA	limit
VBG off	10.5 mA	-	-	limit

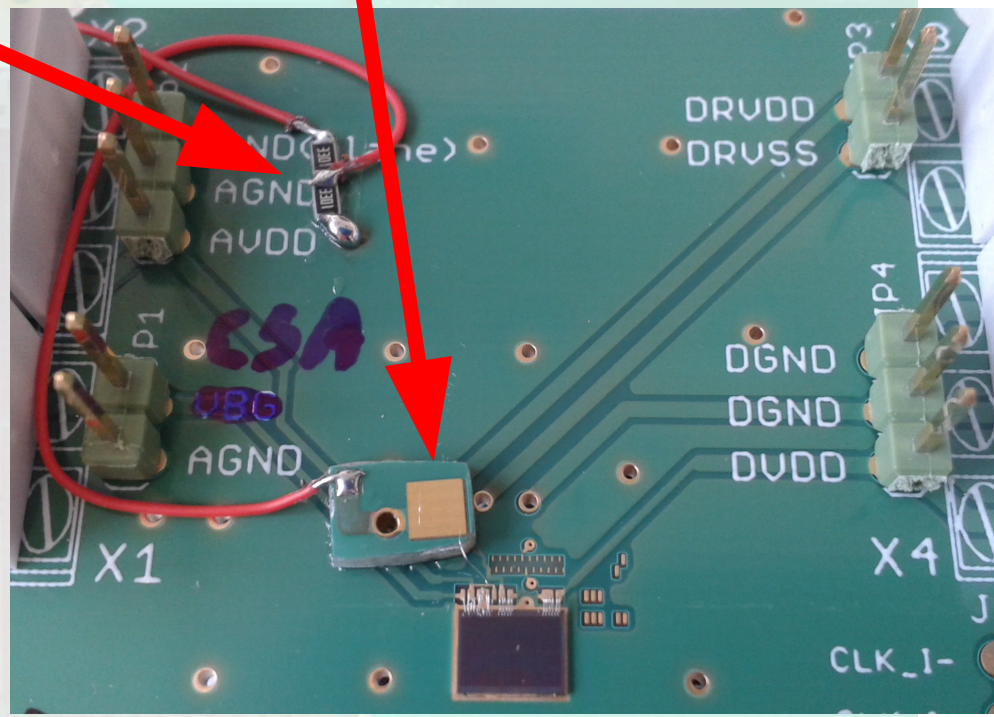


- Observations
  - I(VBG) < 1 nA (measured with source meter)
  - always same final currents, independent of power on sequence
  - no clock applied - no current in digital part, but influence on analog part clearly visible

Results Test Board "P2"

- Voltages bonded: AVDD, DVDD, DRVDD and VBG + CSA_IB2

- Modification
  - VBG from voltage divider and additional pad
  - CSA_IB2 bonded to pad of VBG
- Currents
  - bonded DRVDD first
    → current in limit
  - bonded all other voltages
    → all currents in limit
- Shorts created - how?



Probe Station Test

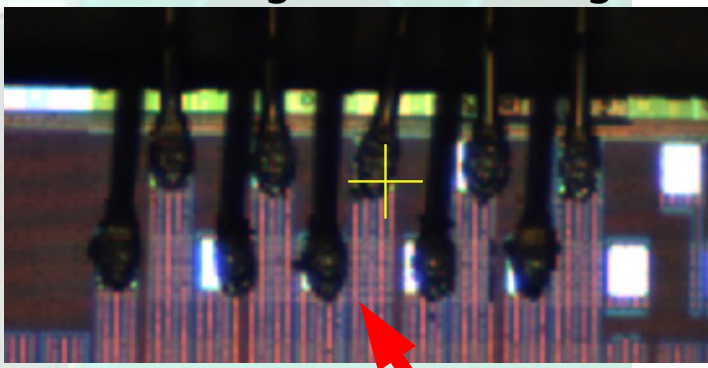
- Single PASTA die put on probe station
  - DRVDD check
    - applied 2.5 V using 2 needles
    - current: 6.7 ... 9.7 mA
  - Pad assignment
    - verified assignment of the 5 DRVDD and 5 DRVSS pads

- Test Board "P3" (not bonded) on probe station
  - all voltages and its corresponding ground probed
  - currents reasonable
    - analog part ≈ 30 mA
    - digital part ≈ 1 mA
    - drivers ≈ 10 mA

Outcome

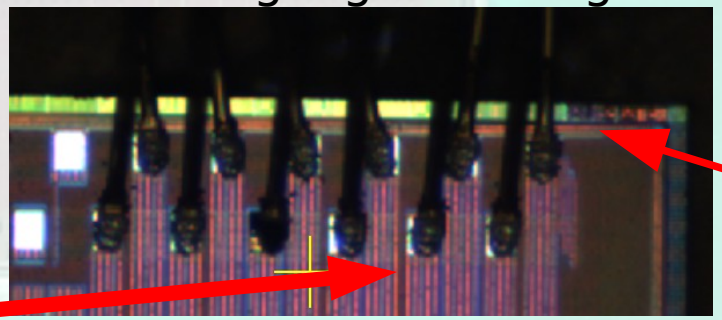
- First realistic current of analog part measured
- No value for current of digital part
  - clock can not be applied since drivers/receivers don't work
- Currents measured on probe station
  - in agreement with test board "P1"
  - demonstrated functionality for all voltages
- Shorts created in bonding process?
  - no passivation on chip
  - pads very small (width=48µm)
  - lines very close to pads
  - bond could create short

bonding driver voltage



short?

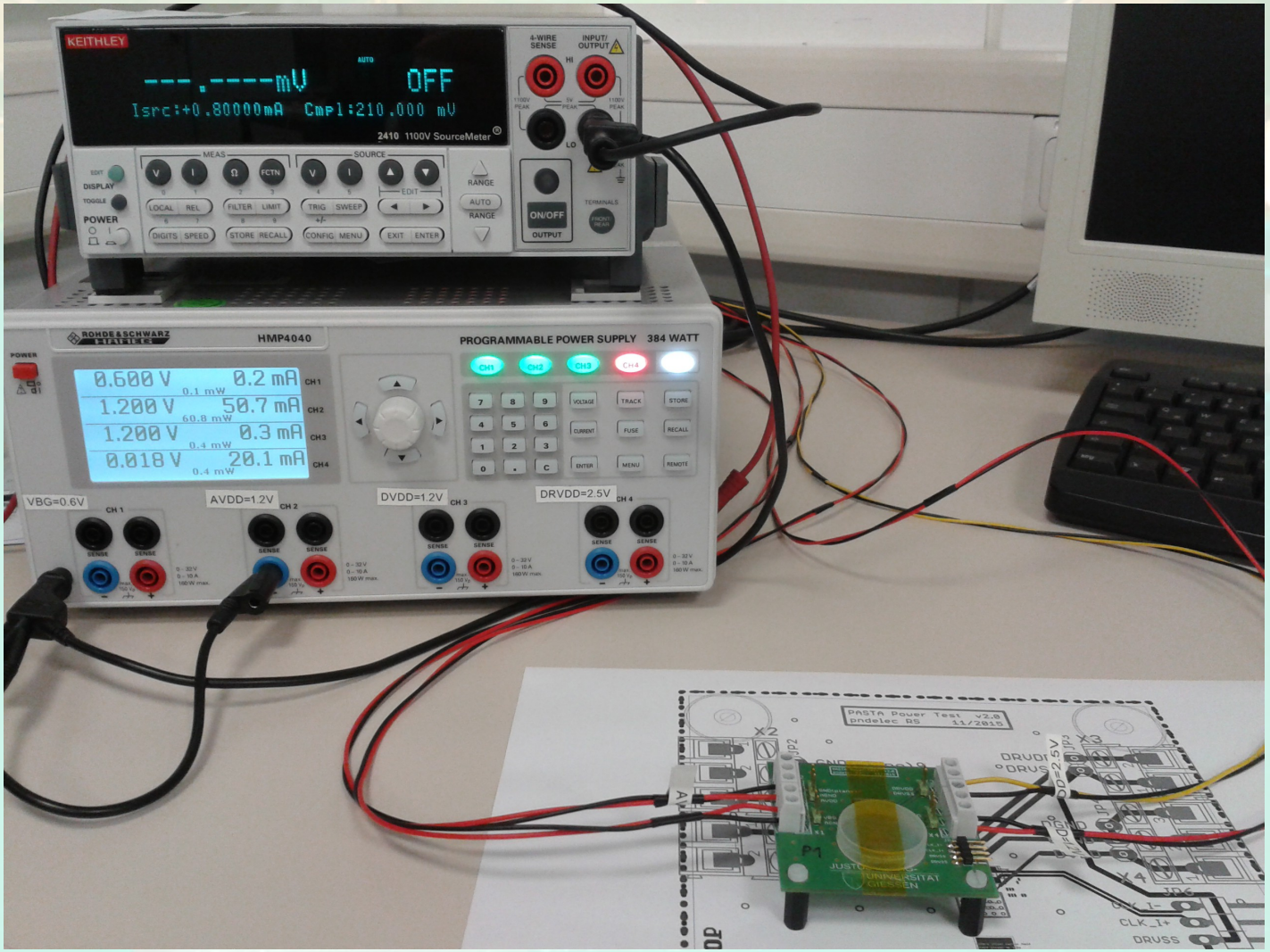
bonding digital voltage



whats that structure? (conducting?)

clearly no short

Thank you for your Attention



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