



PANDA Collaboration Meeting



Status and perspectives for the MVD pixel detector readout ASIC

G. Mazza

on behalf of the Torino MVD pixel group

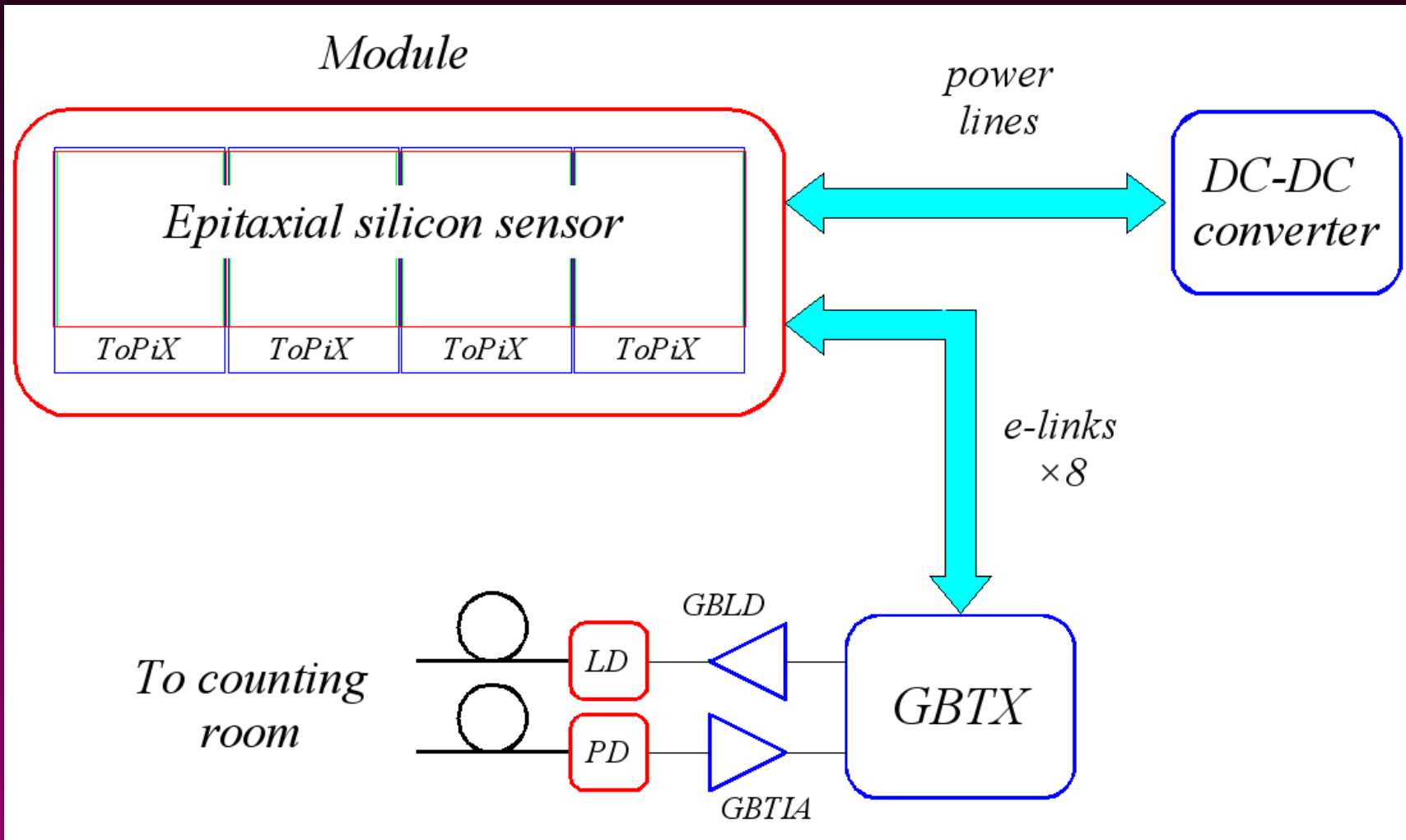


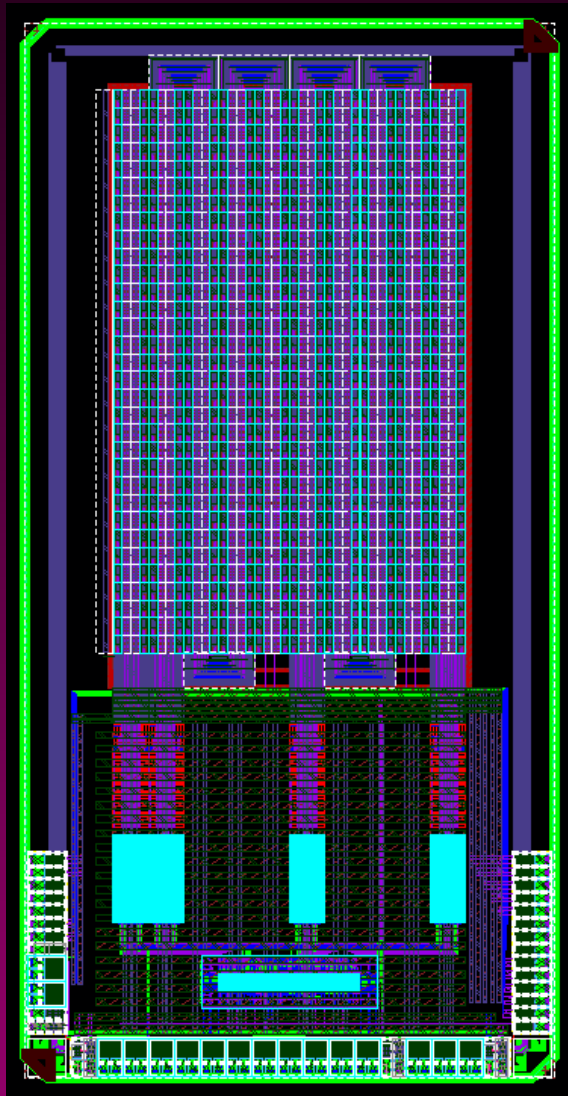
Pixel Detector



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| | |
|-----------------------|--|
| Pixel size | $100 \times 100 \mu\text{m}^2$ |
| Chip active area | $11.4 \times 11.6 \text{ mm}^2$ (116 rows, 110 columns) |
| dE/dx measurement | ToT, 12 bits dynamic range |
| Max input charge | 50 fC |
| Noise floor | $< 32 \text{ aC}$ (200 e^-) |
| Input clock frequency | 160 MHz |
| Time resolution | 6.25 ns (1.80 ns r.m.s.) 12.5 ns (3.61 ns r.m.s.) |
| Power consumption | $< 800 \text{ mW/cm}^2$ |
| Max event rate | $6.1 \cdot 10^6$ |
| Total ionizing dose | $< 100 \text{ kGy}$ |





- * Size : 3 mm × 6 mm
- * CMOS 130 nm
- * 640 pixel cells, 2×2×128 and 2×2×32 columns
- * Hamming encoding and TMR pixel logic protection schemes
- * Compatible with v3 sensors
- * Clock frequency 160 MHz
- * SEU protected EoC
- * Serial data output (SDR and DDR)
- * GBT-compatible SLVS I/O
- * *Received on Feb 18th 2014*



Data format



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| | | | | |
|----|----------------------------|-------------------|--------------------|-----|
| 2 | 12 | 8 | 12 | 6 |
| 01 | Chip address | FC | Not used | ECC |
| 2 | 14 | 12 | 12 | |
| 11 | Pixel address | Leading edge time | Trailing edge time | |
| 2 | 16 | 16 | 6 | |
| 10 | # of events | CRC | ECC | |
| 2 | 38 | | | |
| 00 | idle code (Hex 3A55AA55AA) | | | |

Frame header packet

Data packet

Frame trailer packet

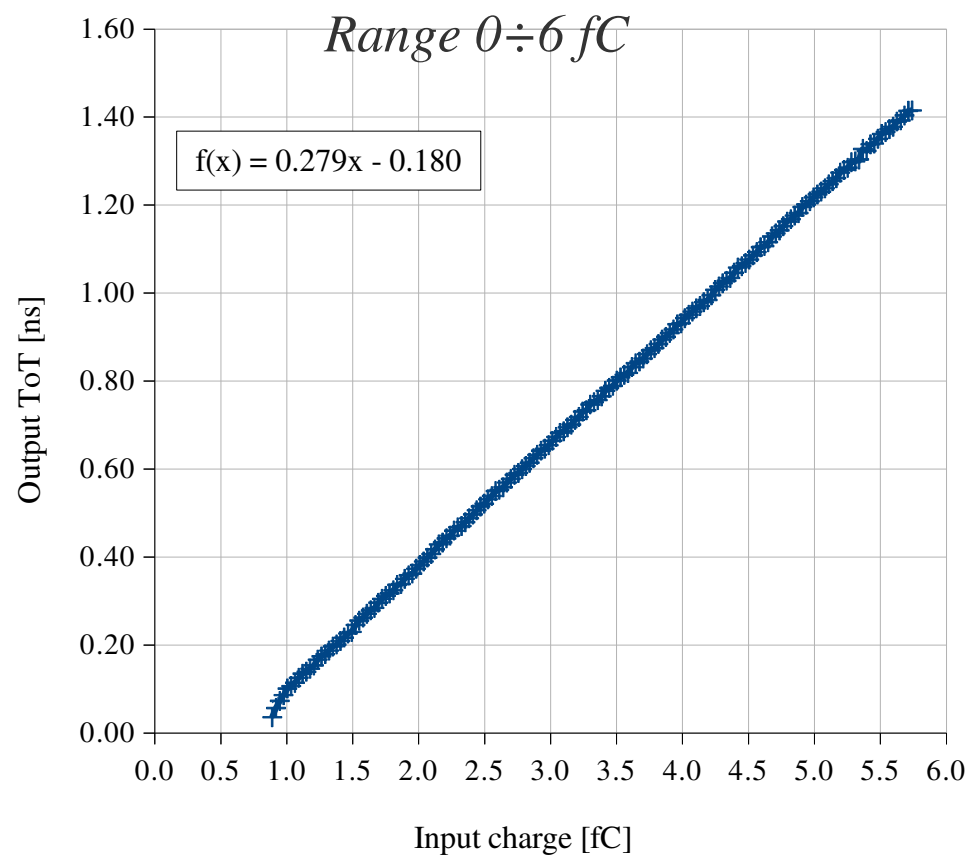
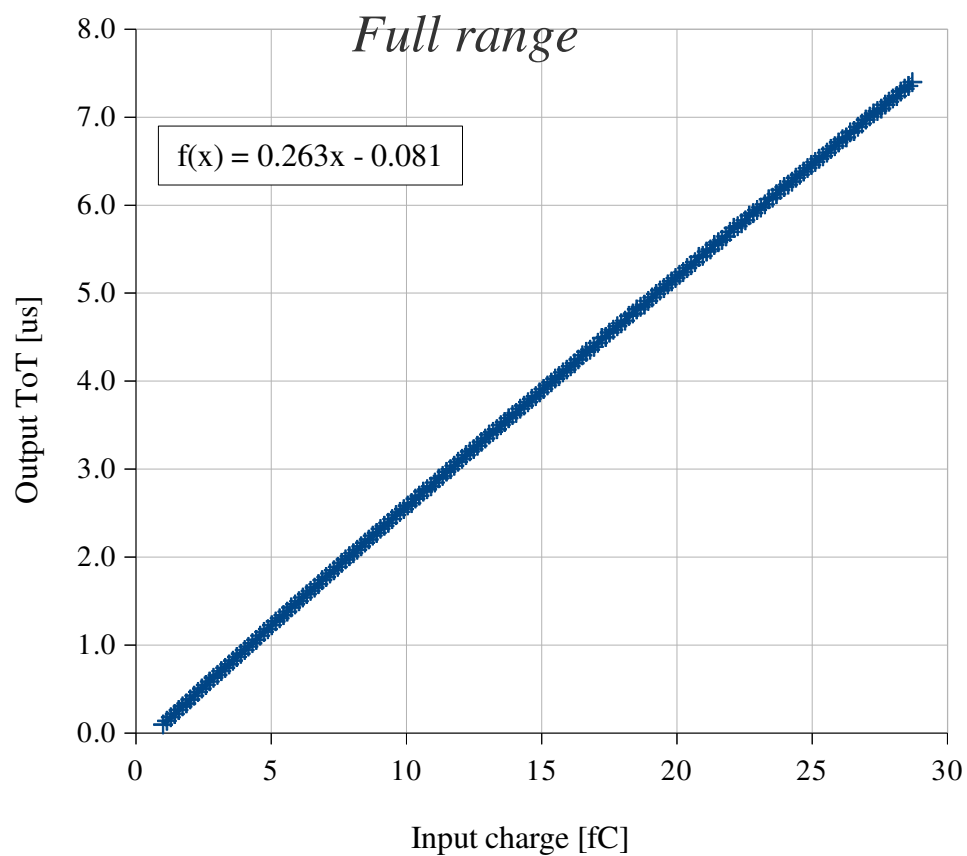
Idle packet



ToT measurements

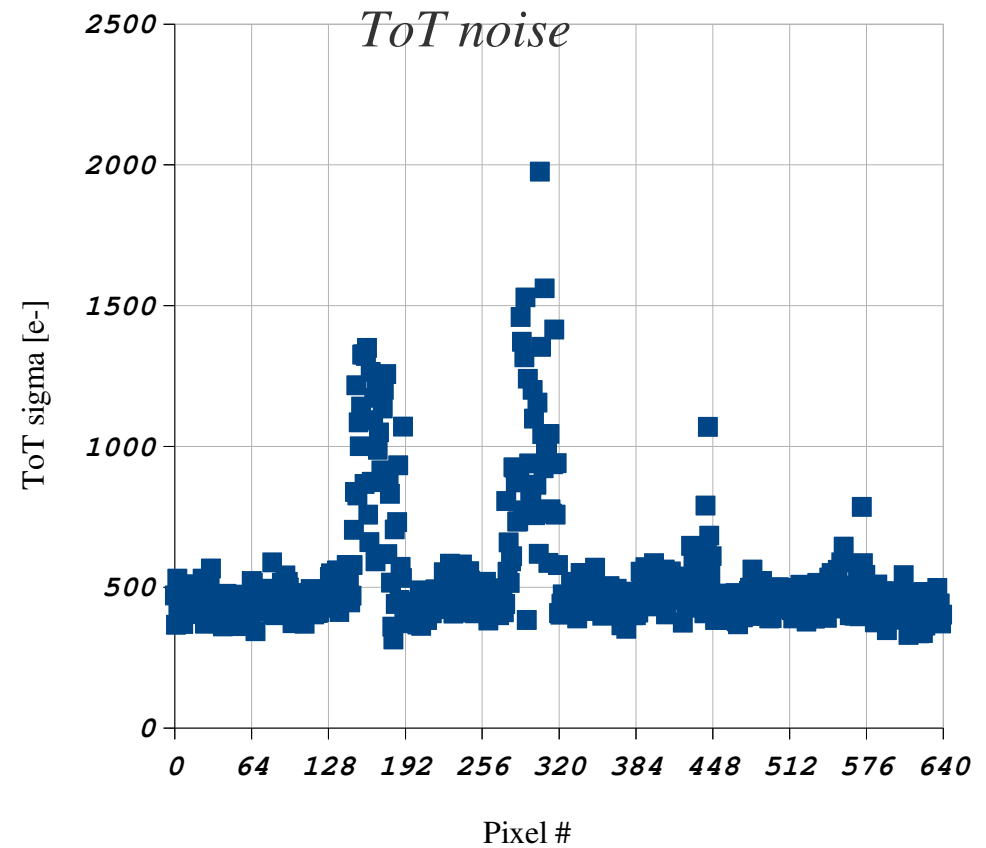
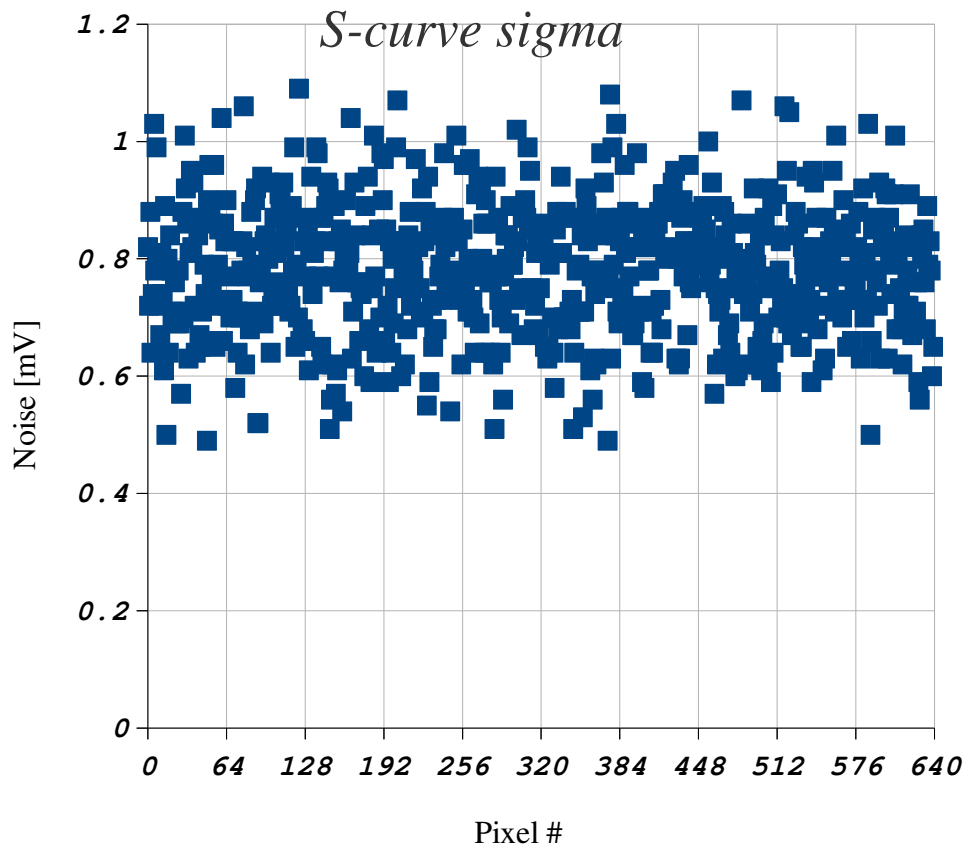


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Noise measurements

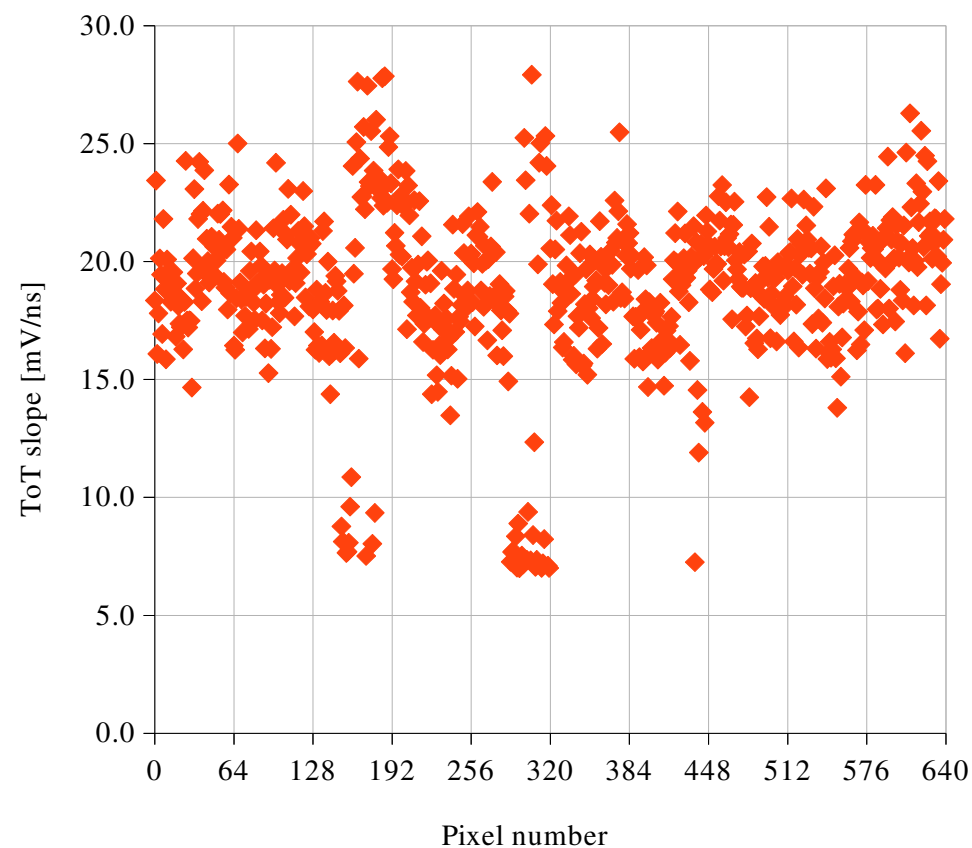
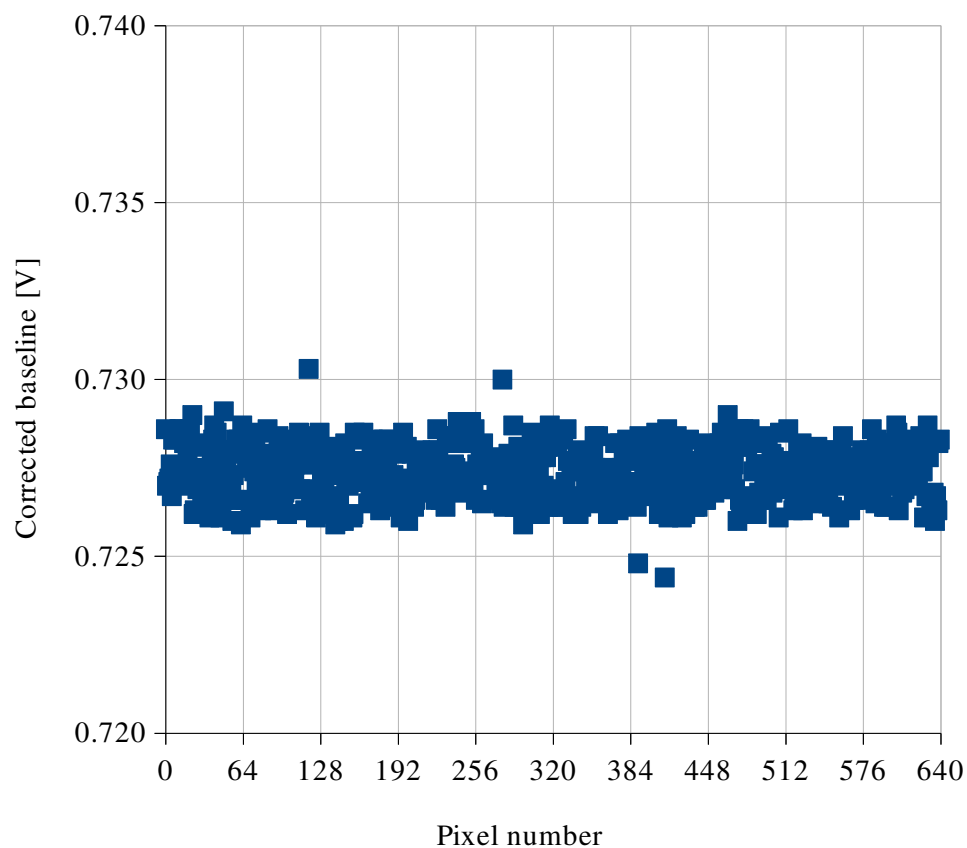




Baseline & ToT



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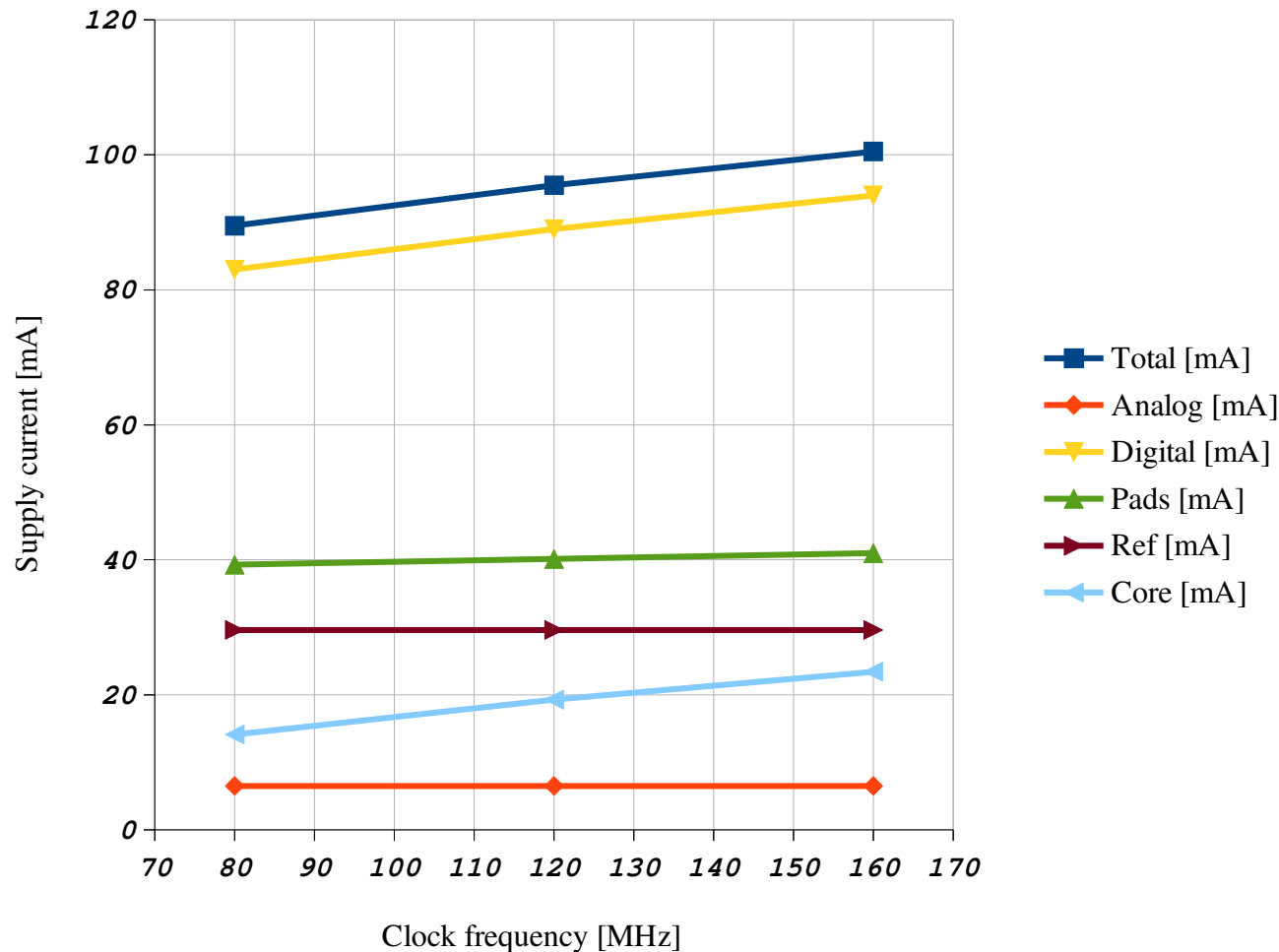


Baseline average value : 727 mV

Baseline sigma : 0.73 mV



Supply current



Estimated power density for the full size version :

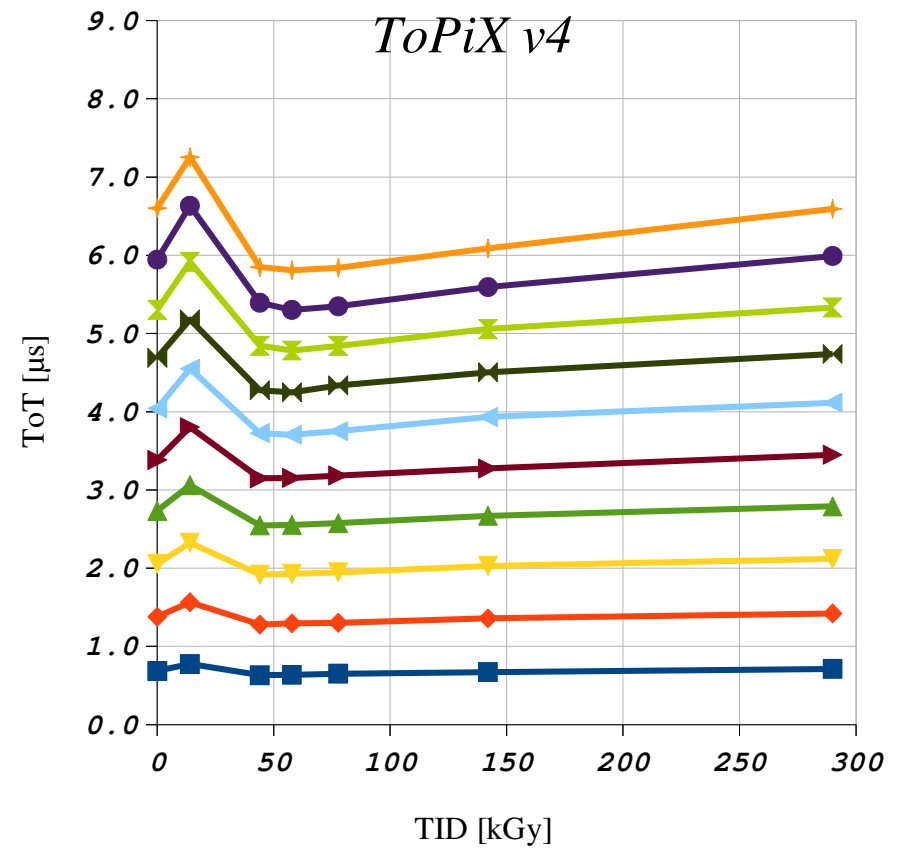
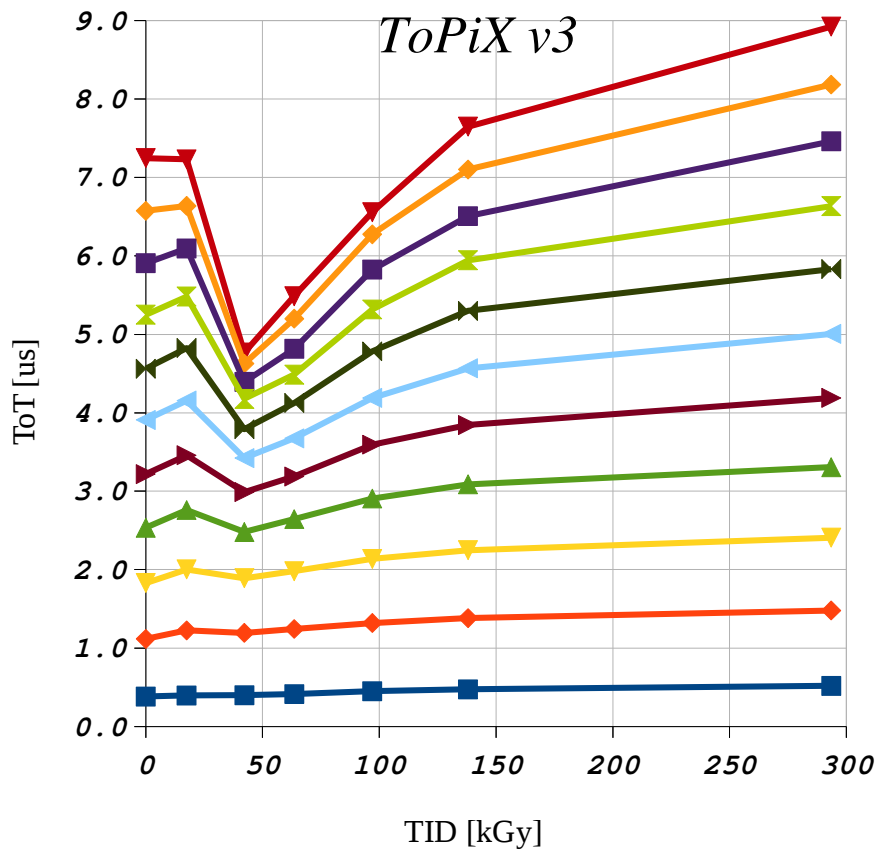
523 mW/cm² @ 80 MHz

666 mW/cm² @ 120 MHz

725 mW/cm² @ 160 MHz



TID measurements ToT

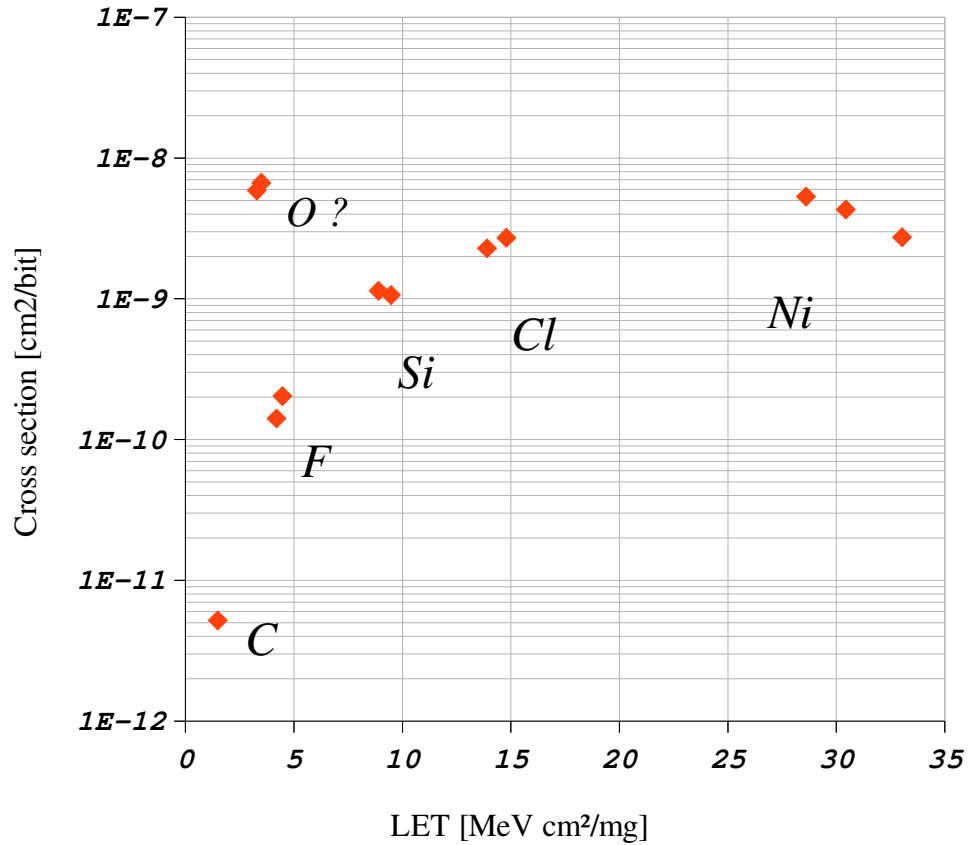




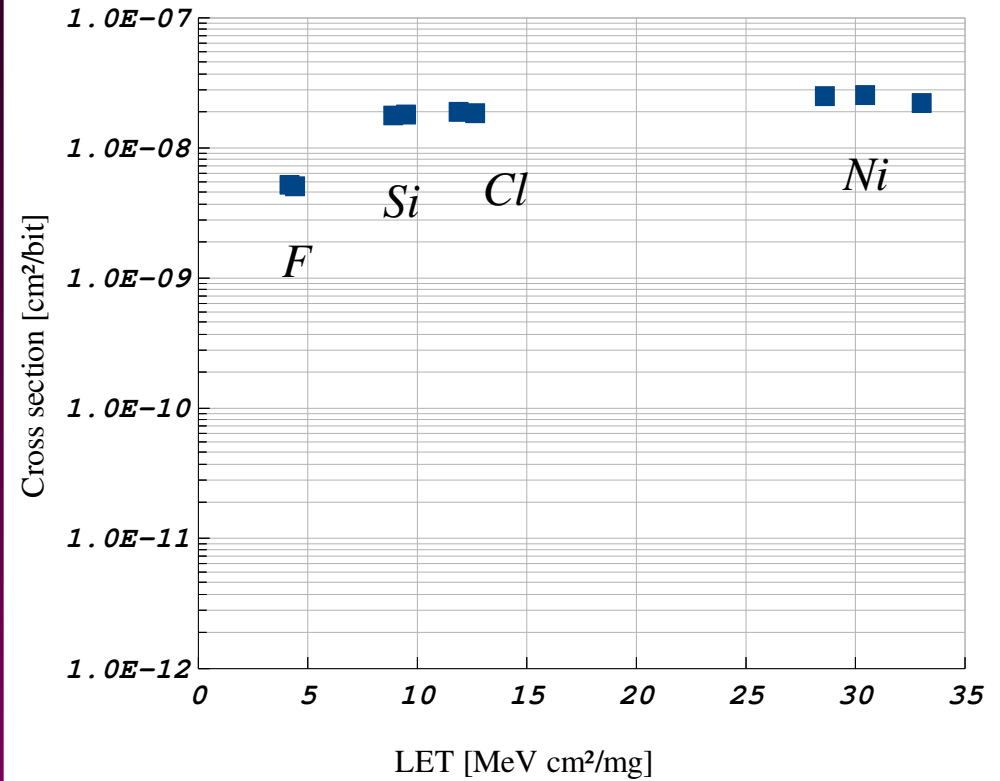
SEU test



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Pixel configuration registers



Hamming-corrected errors

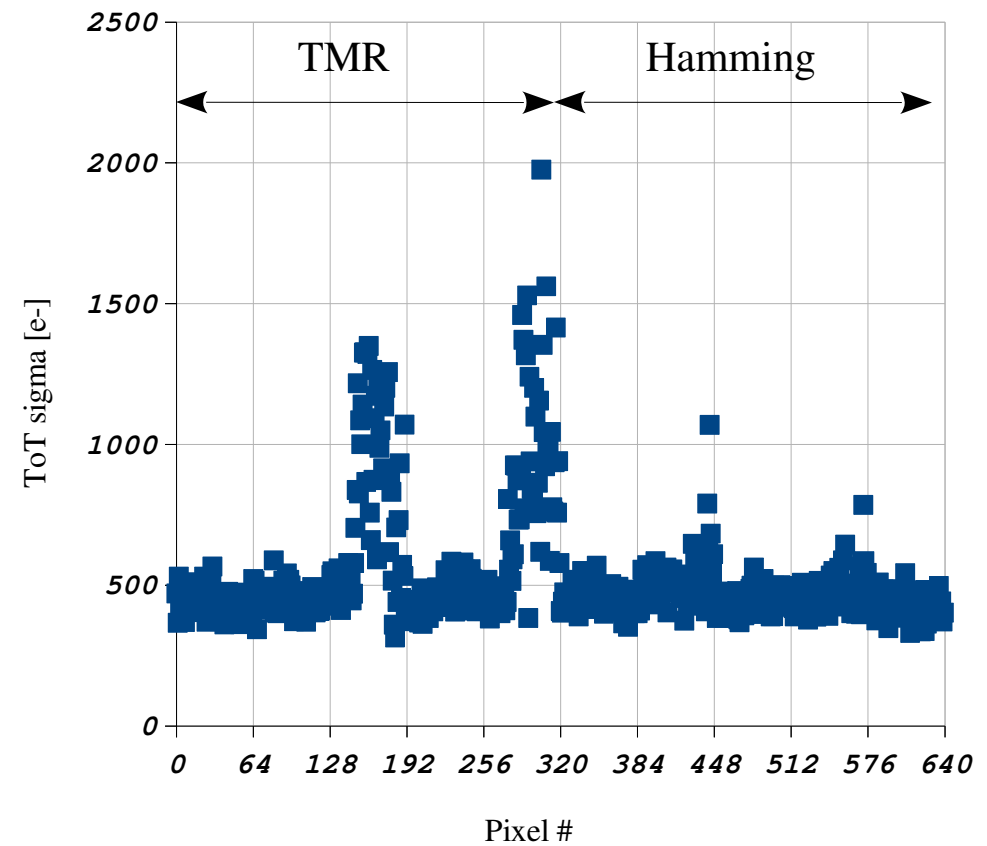
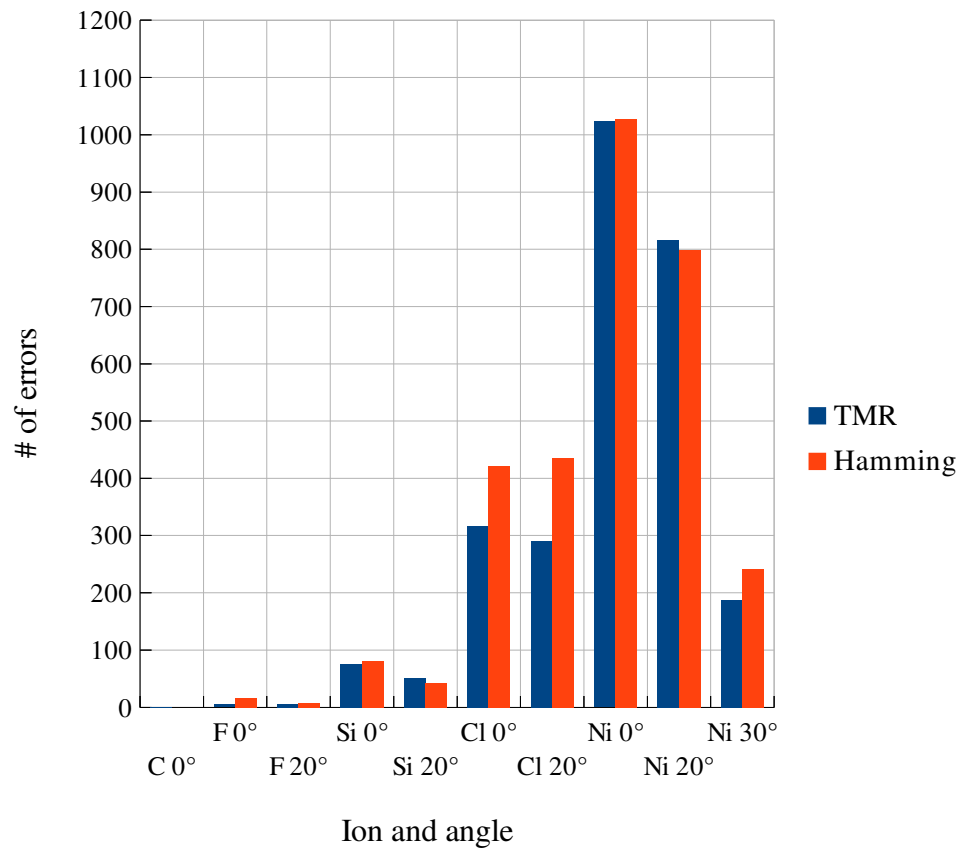
No uncorrected errors detected



TMR vs Hamming



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ToPiX v5



- * Full size chip design started
- * Size (*preliminary*) : 11.2 mm × 14.8 mm
- * Pixel matrix (*preliminary*) : 110 × 116
- * Input clock : 160 MHz
- * Max output bandwidth : 4 × 320 Mb/s
- * Supply voltage : 1.2 V
- * Columns divided in 8 regions with 7 double columns each
- * Triple tier buffering (FIFO at the end of column, region control and chip control units)



Outlook



- * Activity on ToPiX v5 stopped on April 2015 due to issues on FAIR schedule
 - ➔ It can restart in 2016 upon approval by INFN
- * Going ahead with current IBM/GF 0.13 μm technology would be a big hazard (possible technology phase-out in 2017) – looking for alternatives
- * CERN has moved from IBM/GF to TSMC as their reference technology (both for the 65 nm and the 130 nm nodes)
- * Critical issues for the choice of the new technology are :
 - ➔ radiation tolerance
 - ➔ metal lines resistance and capacitance (RC delay)



Technology comparison



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| Foundry | Process | Engineering run relative price | Metal resistance | Metal capacitance | Radiation tolerance |
|---------|--------------------|--------------------------------|------------------|-------------------|---------------------|
| A | 0.13 μm | 1 (2014) | 1 (Cu) | 1 | Tested @ CERN |
| B | 0.13 μm | 0.78 (2012) | 1.5 (Cu) | 1.2 | Tested @ CERN |
| C | 0.11 μm | 0.36 (2015) | 3.5 (Al) | 1.1 | Not tested |
| C | 0.13 μm | 0.40 (2011) | 1.9 (Cu) | 1.4 | Not tested |

Important : price figures are just for 1st order comparison – no exact values



Conclusions



- * ToPiX v4 has been extensively tested and is basically ok.
- * ToPiX v5 (full size) design stopped after problems in the FAIR schedule
- * It is possible a phase out of the current 0.13 μm process in 2017 – it is suggestible to move to a different technology
- * A new reduced size prototype (ToPiX_v4b) will be required
- * 3 processes under evaluation w.r.t. radiation tolerance, RC delay and price



PANDA FEE_DAQT Meeting



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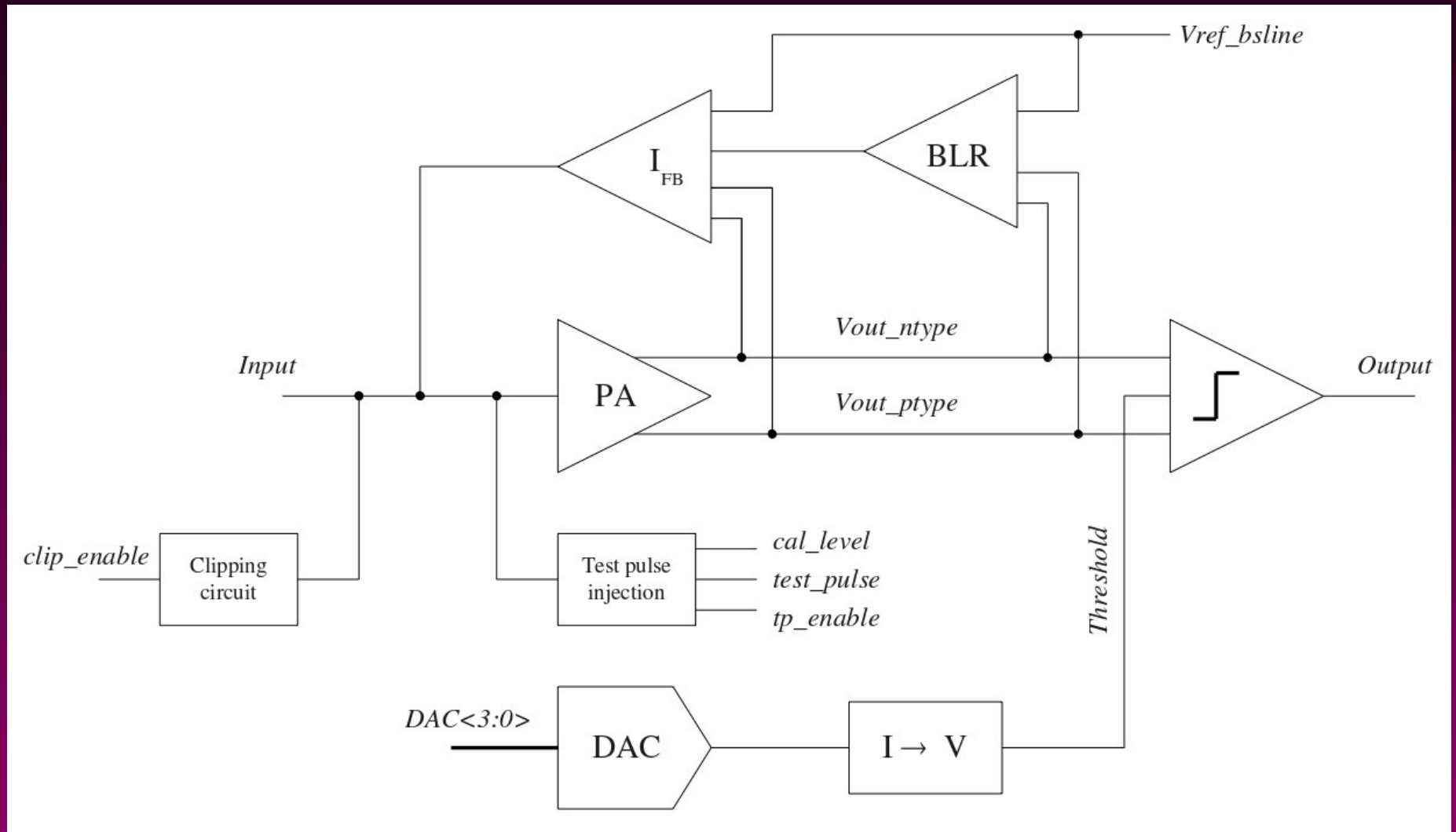
Backup slides



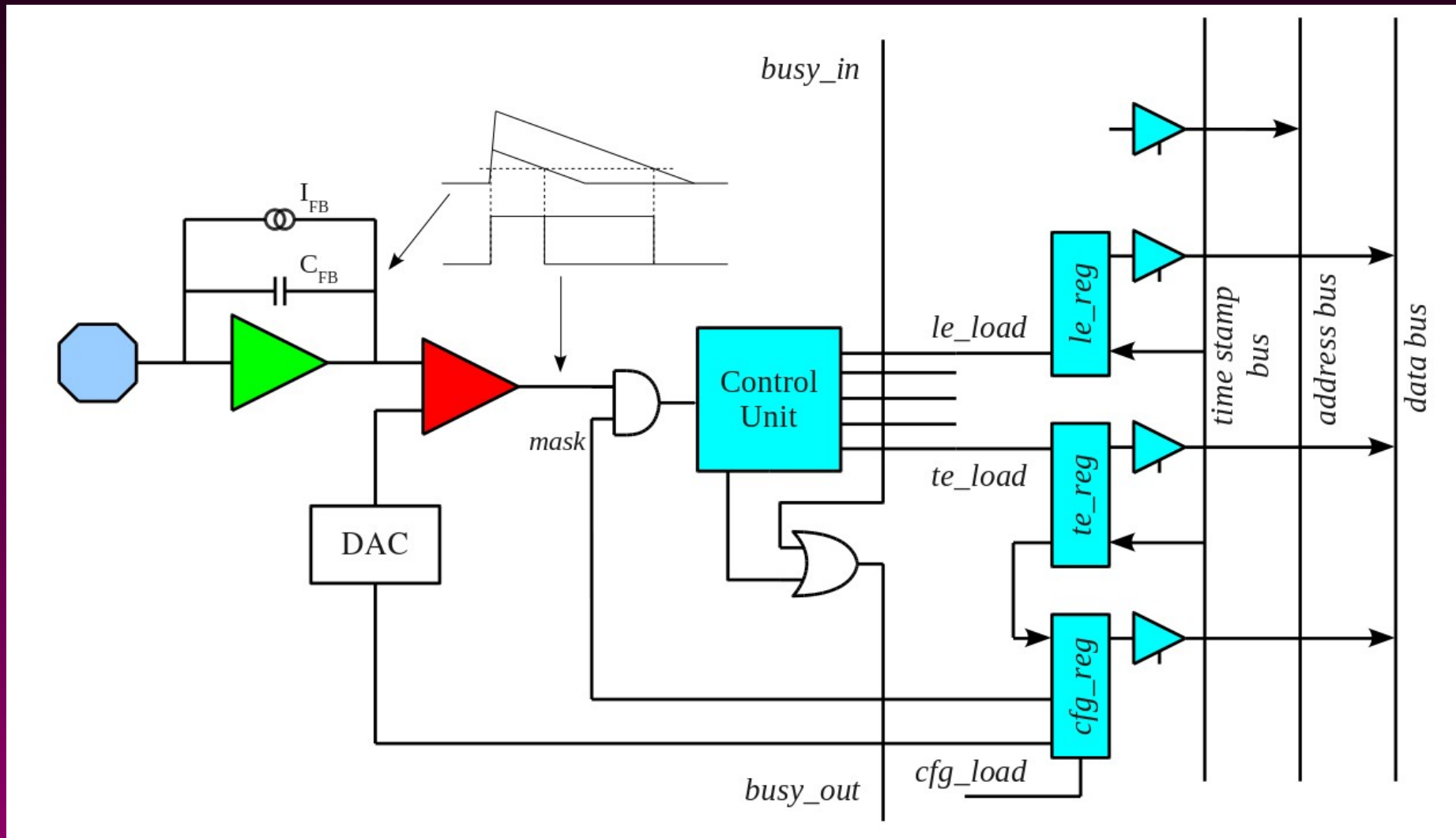
F/E schematic

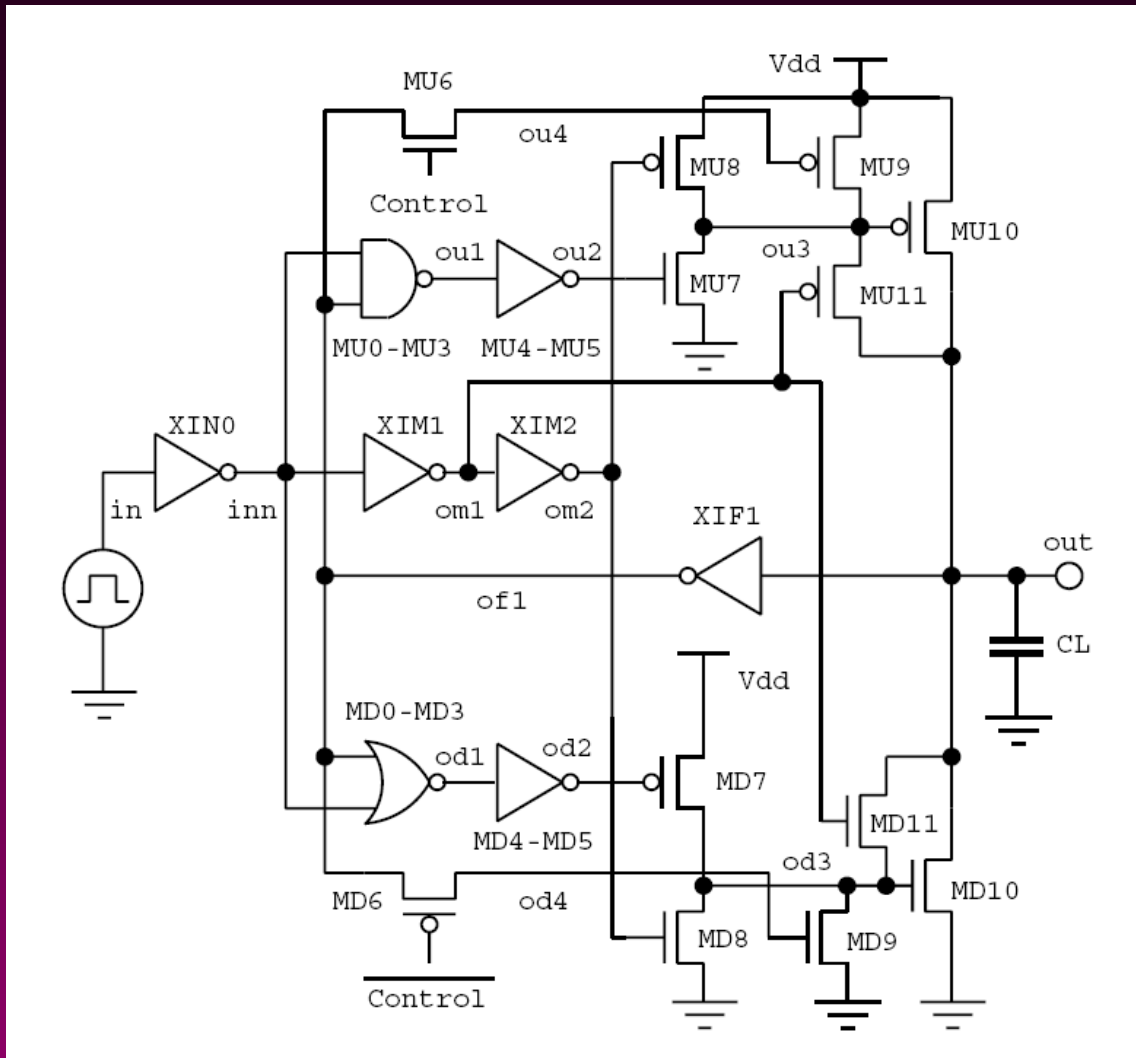


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Pixel cell schematic





Bus capacitance : 49.9 fF/cell

Bus resistance : 9.3 Ω /cell

Provides both reduced voltage swing and pre-emphasis or full voltage swing

J.C.Garcia, J.A.Montiel, S.Nooshabadi
 Adaptive Low/High Voltage Swing
 CMOS Driver for On-Chip Interconnects
 ISCAS 2007



On ToPiX data rates capabilities



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| | <i># links</i> | <i>Clock freq.</i> | <i>Event size</i> | <i>Rate/chip (SDR)</i> | <i>Rate/chip (DDR)</i> | <i># pixels</i> | <i>Rate/px (SDR)</i> | <i>Rate/px (DDR)</i> | <i>Rate/cm² (SDR)</i> | <i>Rate/cm² (DDR)</i> |
|-----------------|----------------|--------------------|-------------------|------------------------|------------------------|-----------------|----------------------|----------------------|----------------------------------|----------------------------------|
| | | <i>[MHz]</i> | <i>bits</i> | <i>Mev/s</i> | <i>Mev/s</i> | | <i>kev/s</i> | <i>kev/s</i> | <i>Mev/s</i> | <i>Mev/s</i> |
| <i>ToPiX v3</i> | <i>1</i> | <i>50</i> | <i>32</i> | <i>1.43</i> | <i>-</i> | <i>640</i> | <i>2.23</i> | <i>-</i> | <i>22.32</i> | <i>-</i> |
| <i>ToPiX v4</i> | <i>1</i> | <i>50</i> | <i>40</i> | <i>1.11</i> | <i>2.22</i> | <i>640</i> | <i>1.74</i> | <i>3.47</i> | <i>17.36</i> | <i>34.72</i> |
| <i>ToPiX v4</i> | <i>1</i> | <i>160</i> | <i>40</i> | <i>3.56</i> | <i>7.11</i> | <i>640</i> | <i>5.56</i> | <i>11.11</i> | <i>55.56</i> | <i>111.11</i> |
| <i>ToPiX v5</i> | <i>1</i> | <i>160</i> | <i>40</i> | <i>4.0</i> | <i>8.0</i> | <i>12760</i> | <i>0.31</i> | <i>0.63</i> | <i>3.13</i> | <i>6.27</i> |
| <i>ToPiX v5</i> | <i>2</i> | <i>160</i> | <i>40</i> | <i>8.0</i> | <i>16.0</i> | <i>12760</i> | <i>0.63</i> | <i>1.25</i> | <i>6.27</i> | <i>12.54</i> |
| <i>ToPiX v5</i> | <i>3</i> | <i>160</i> | <i>40</i> | <i>12.0</i> | <i>24.0</i> | <i>12760</i> | <i>0.94</i> | <i>1.88</i> | <i>9.40</i> | <i>18.81</i> |
| <i>ToPiX v5</i> | <i>4</i> | <i>160</i> | <i>40</i> | <i>16.0</i> | <i>32.0</i> | <i>12760</i> | <i>1.25</i> | <i>2.51</i> | <i>12.54</i> | <i>25.08</i> |