Status of the MVD Strip Electronics

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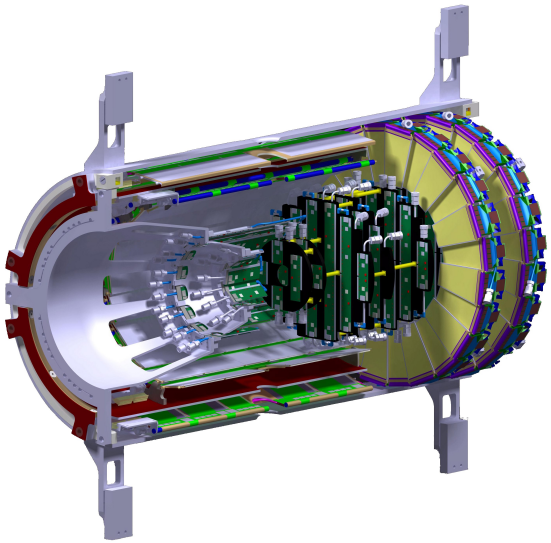
II. Physikalisches Institut

Status of the MVD Strip Electronics

- Introduction
- The PASTA Chip
- Current Status
- Perspectives

Introduction

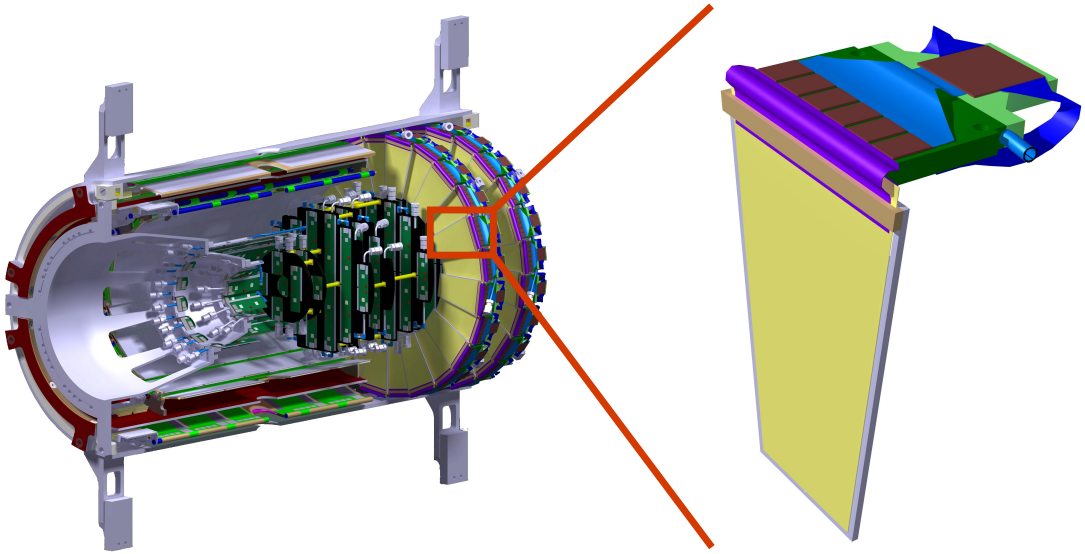
Micro Vertex Detector



Introduction

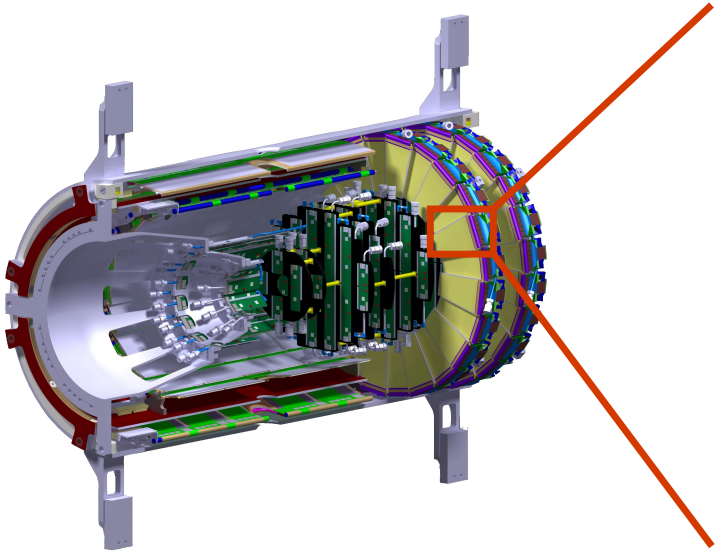
Micro Vertex Detector

Sensor Module

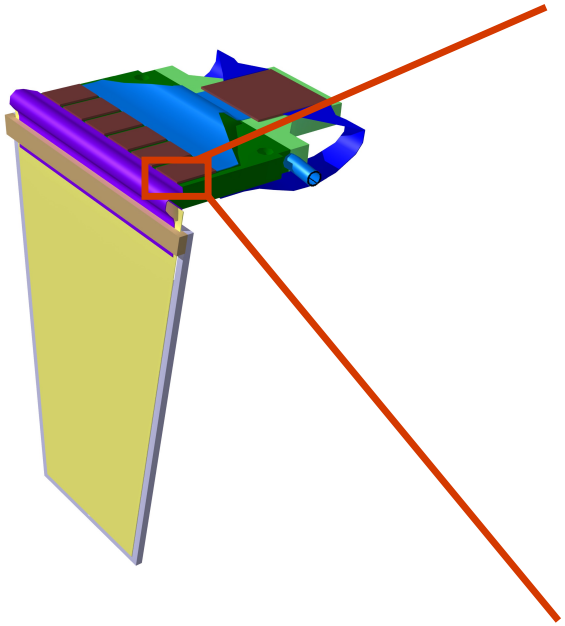


Introduction

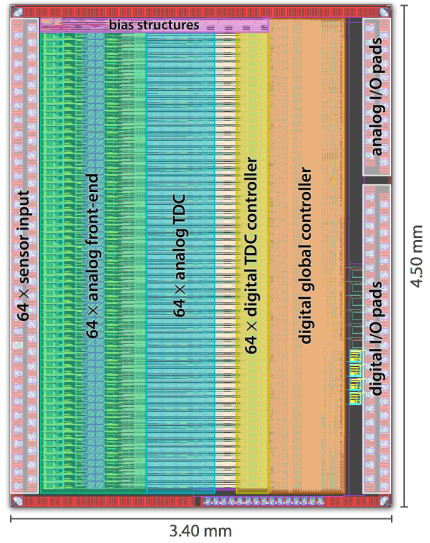
Micro Vertex Detector



Sensor Module



Readout ASIC



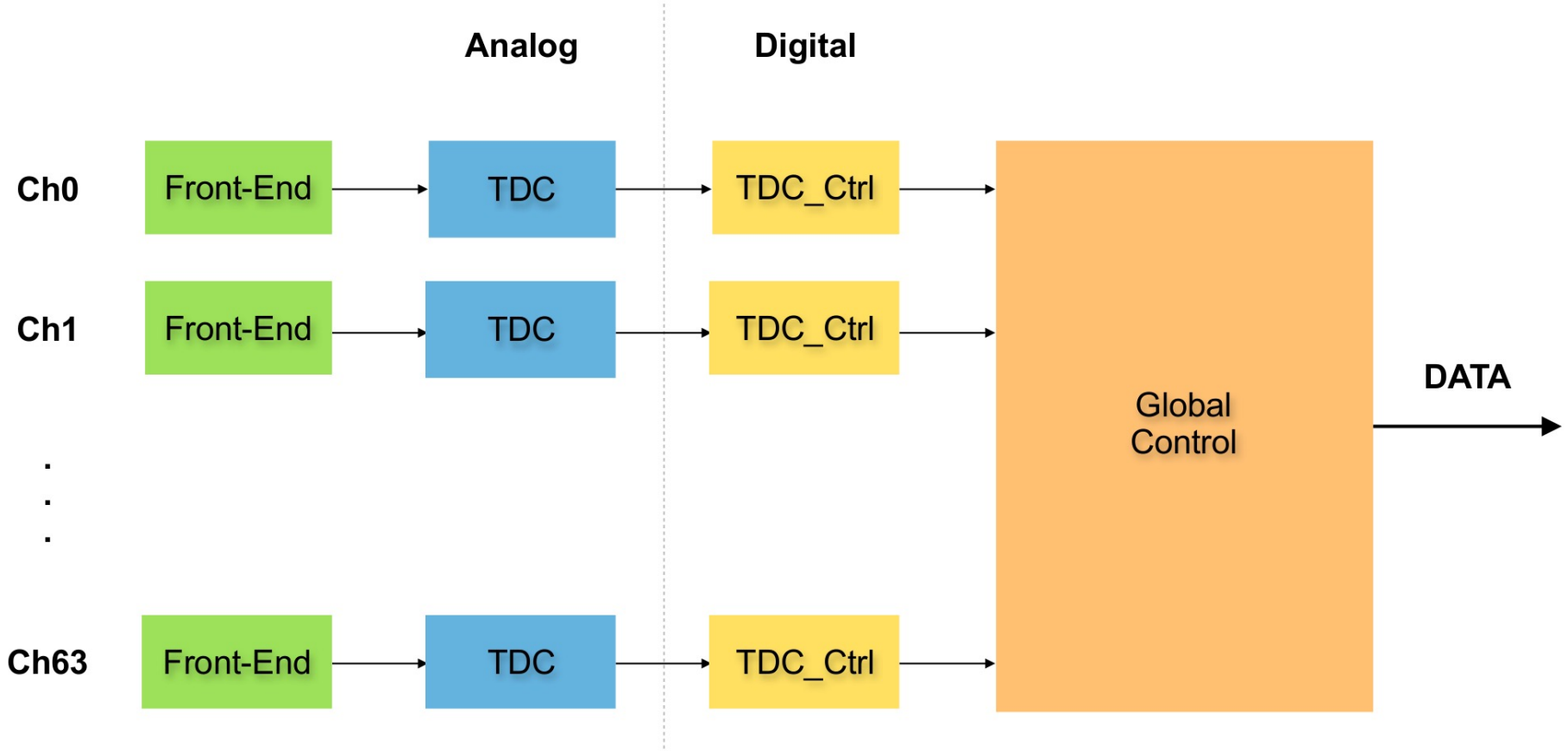
PASTA: PANDA Strip ASIC

Key features

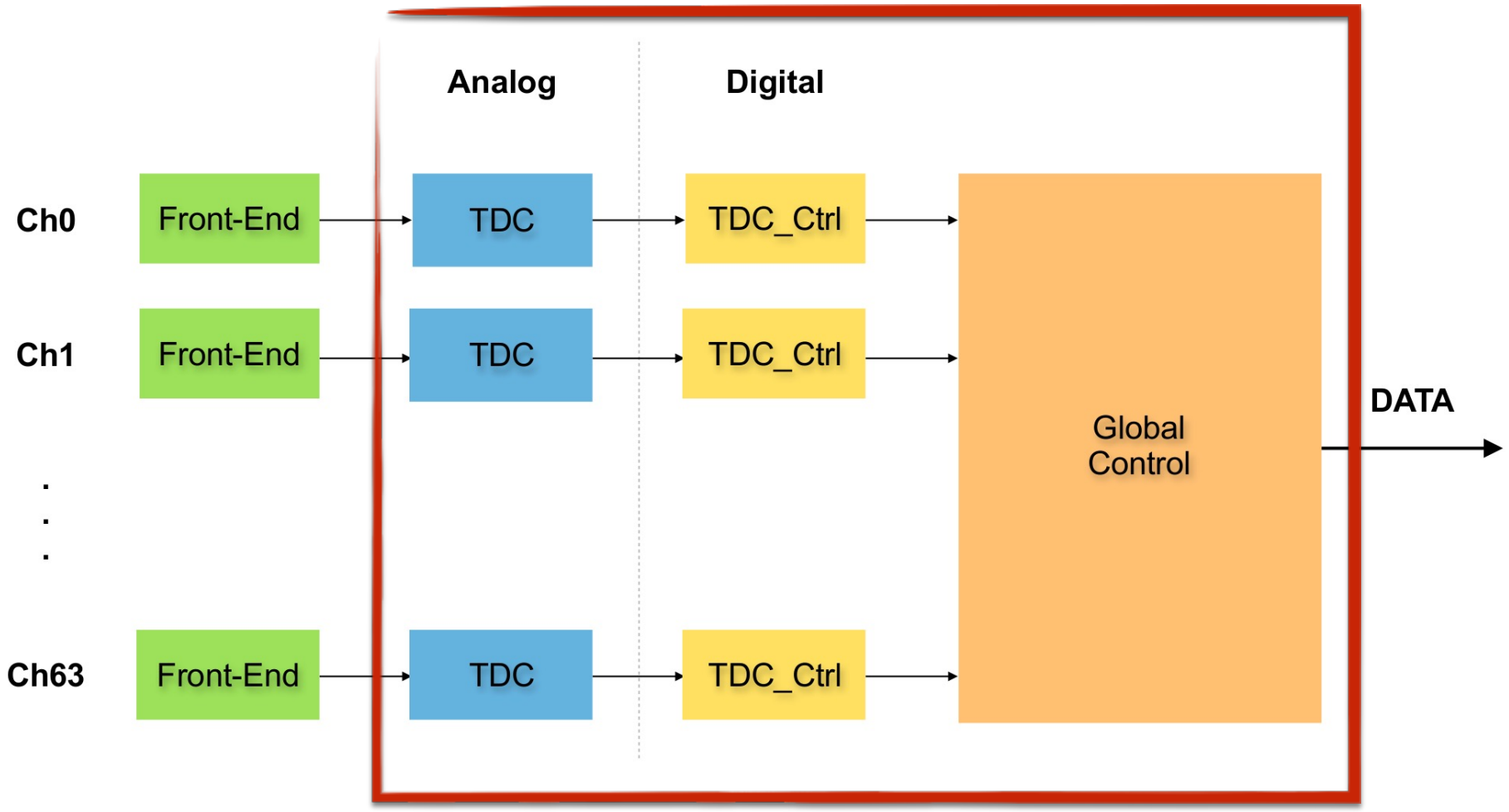
Channels	64
Input pitch	63 µm
Rate capability	100 kHz/channel
Power consumption	< 4 mW/channel
Front-end noise	< 600 e^-
Time bin width	50 - 400 ps
Charge resolution	8 bit (dyn. range) *
Radiation tolerance	100 kGy *

* Design goal

PASTA Architecture

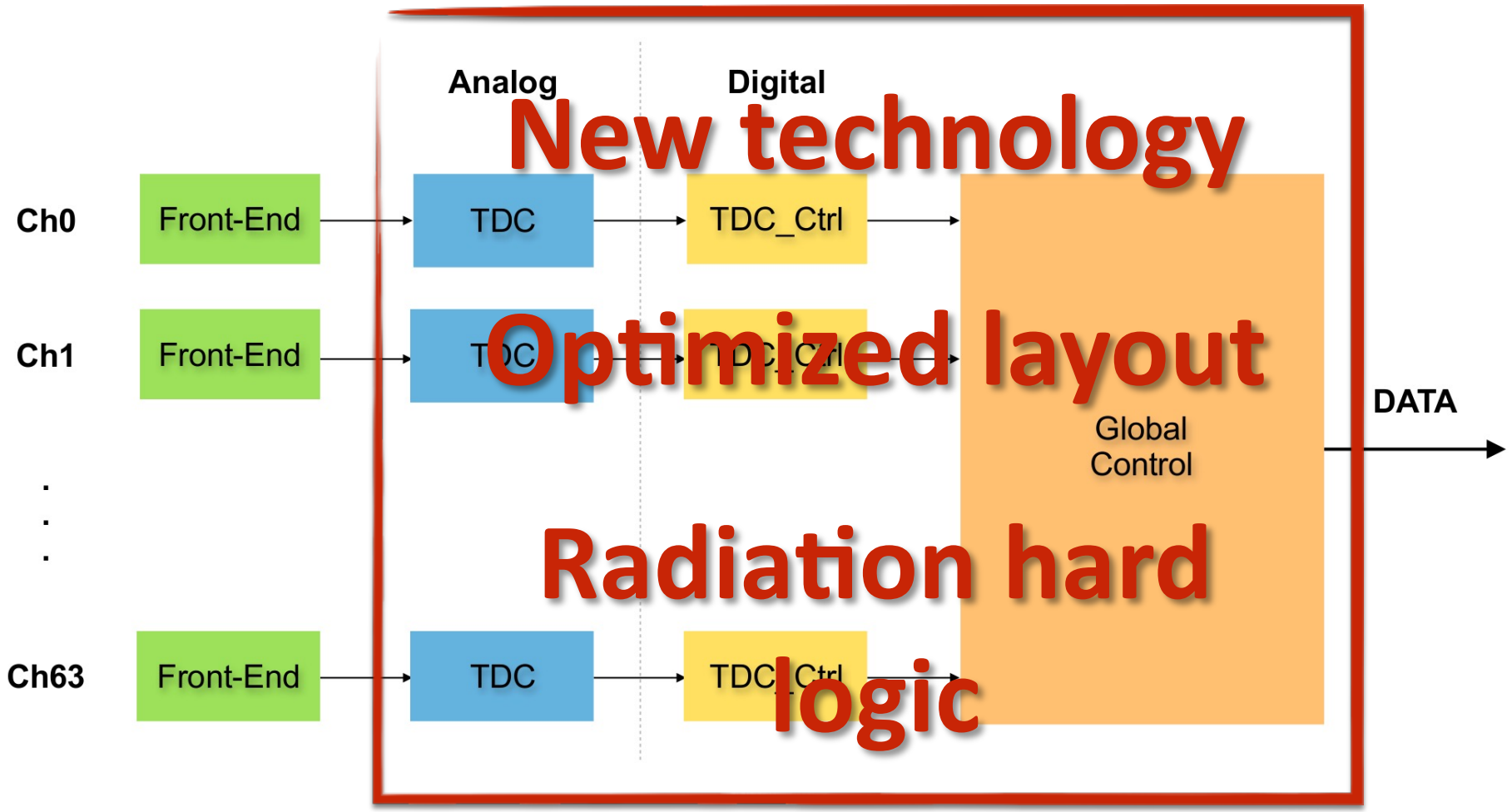


PASTA Architecture



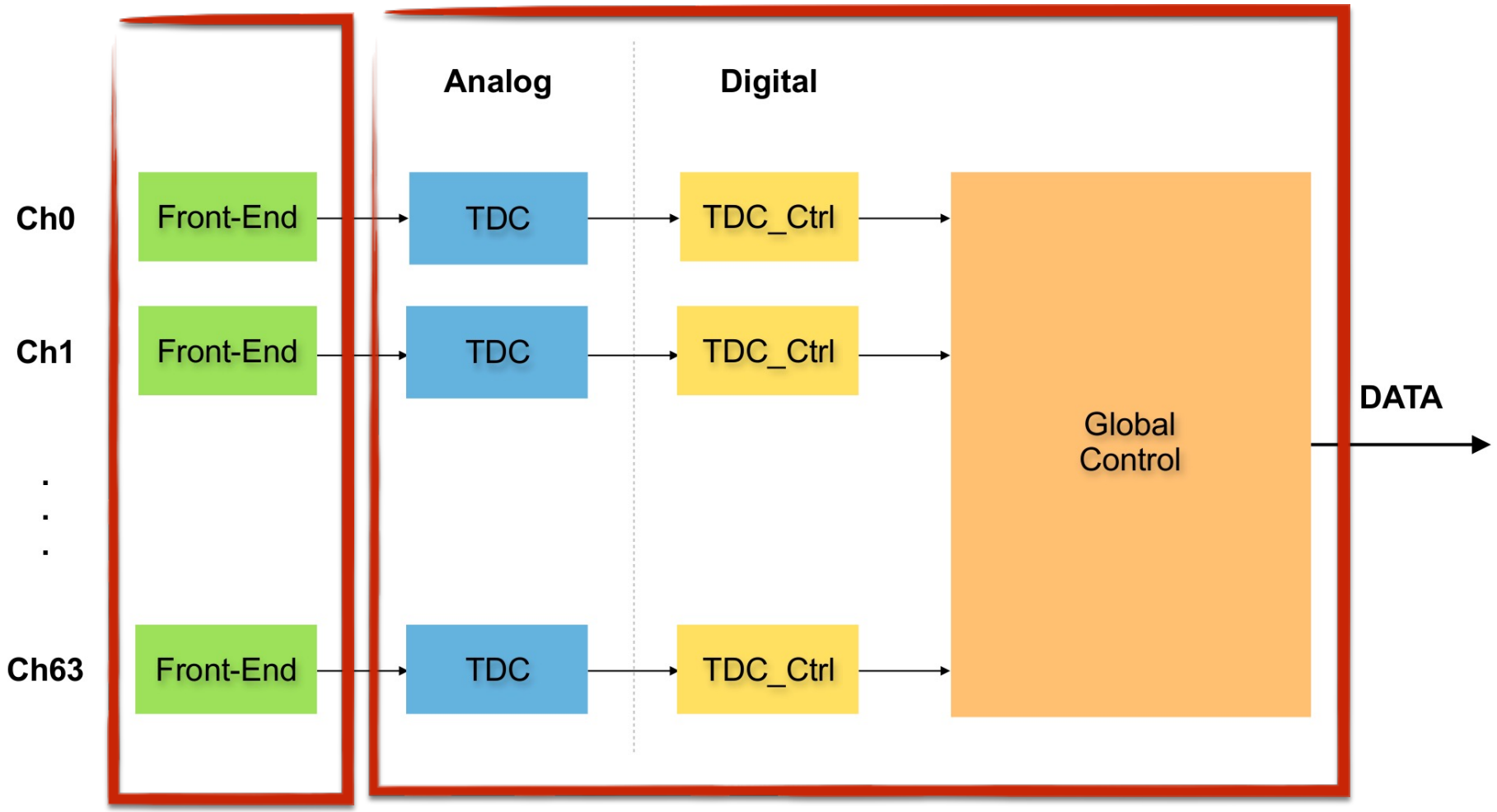
Based on TOF-PET

PASTA Architecture



Based on TOF-PET

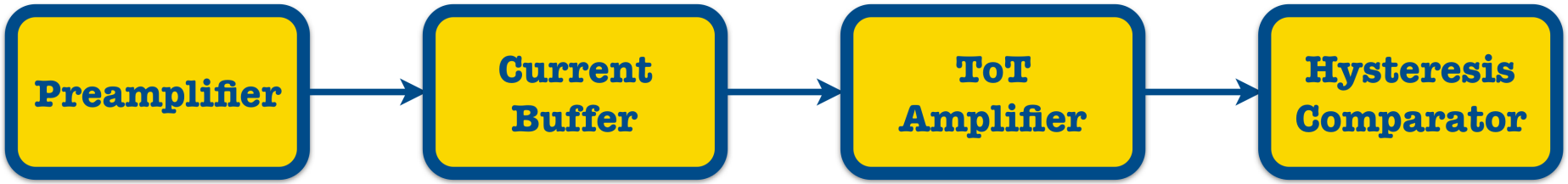
PASTA Architecture



New design

Based on TOF-PET

Front-end Amplifier



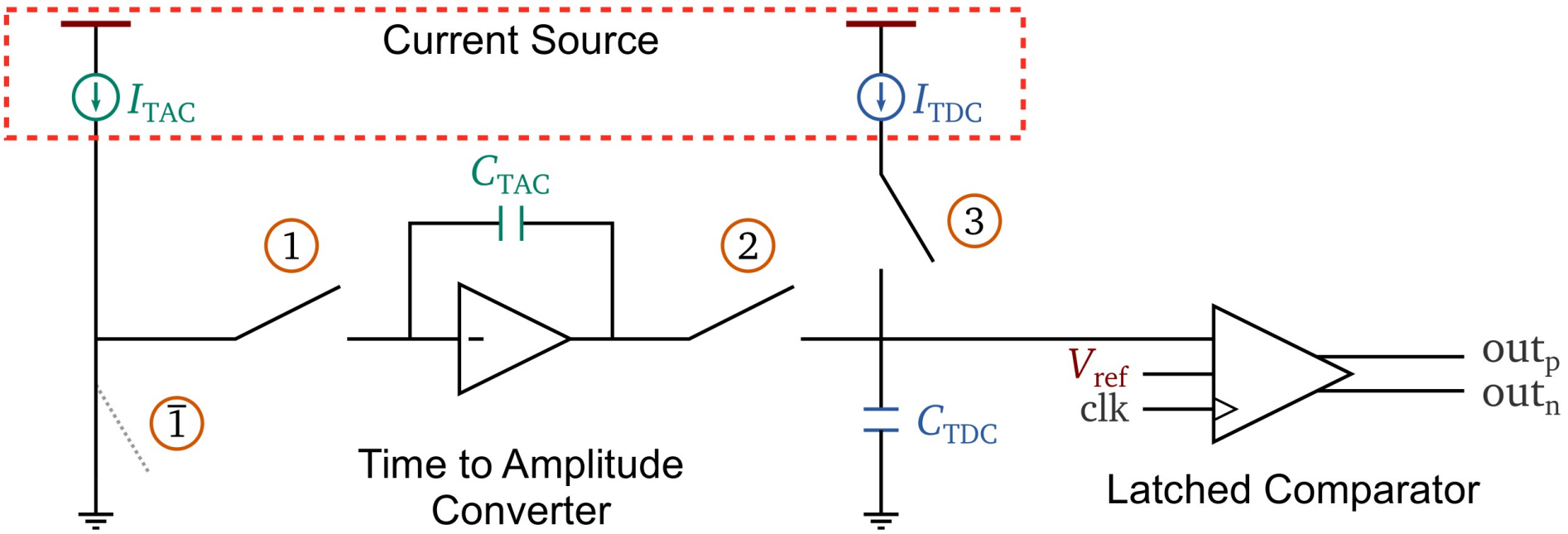
First amplification stage capable of processing signals of both polarities (n-type or p-type strips)

Stage providing both current gain and impedance adjustment

Second amplification stage for the linear discharge of the feedback capacitance

Low noise sensitivity

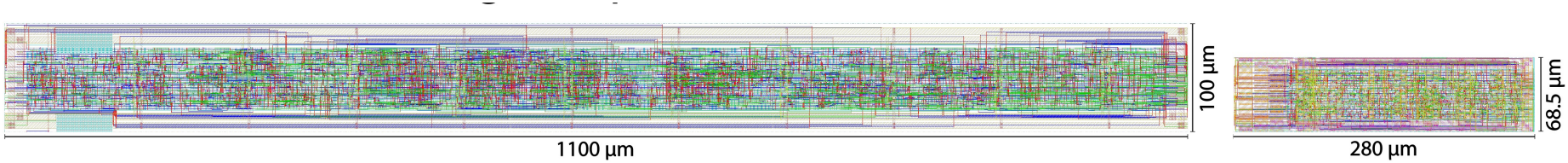
Analog TDC


Current Source
I_{TAC}
I_{TDC}
C_{TAC}
1
2
3
$\overline{1}$
Time to Amplitude Converter
C_{TDC}
V_{ref}
clk
out_p
out_n
Latched Comparator

Digital Blocks

Optimization of the TDC Control

- Size reduced by ~80%
- Radiation-hard logic implemented

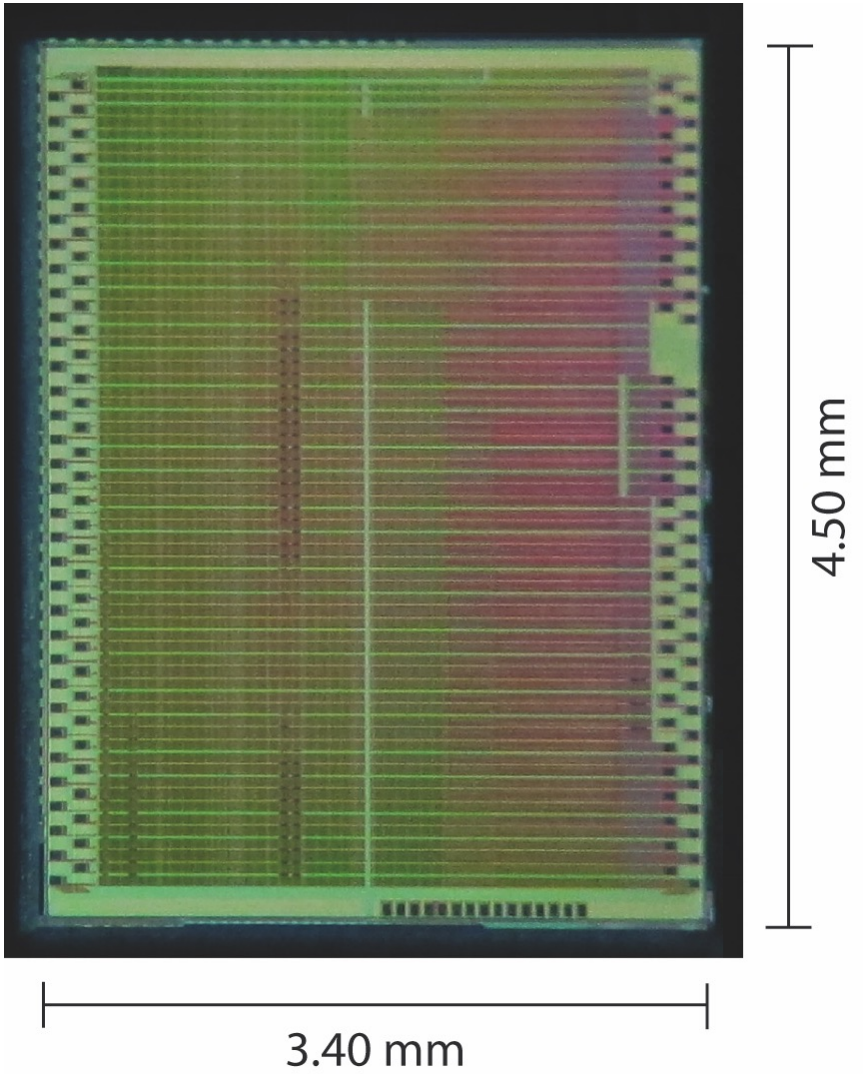


Single Event Upset (SEU) Protection

- 1 bit: Triple Modular Redundancy
- N bits: Hamming encoding

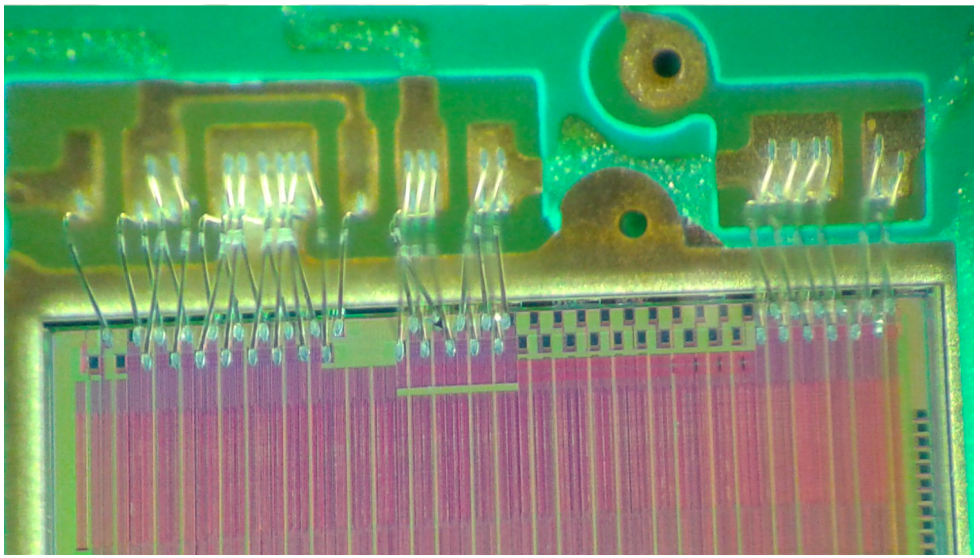
Current Status

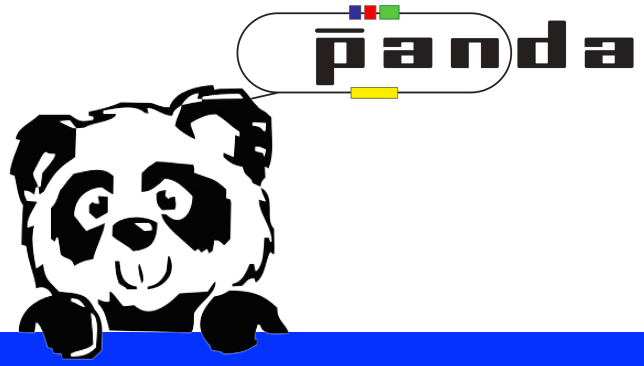
- Chip submitted in April 2015 and received in September
- Chip manual in preparation
- First board for power and bonding test designed and produced
- Chip bonded, first test in progress



Perspectives

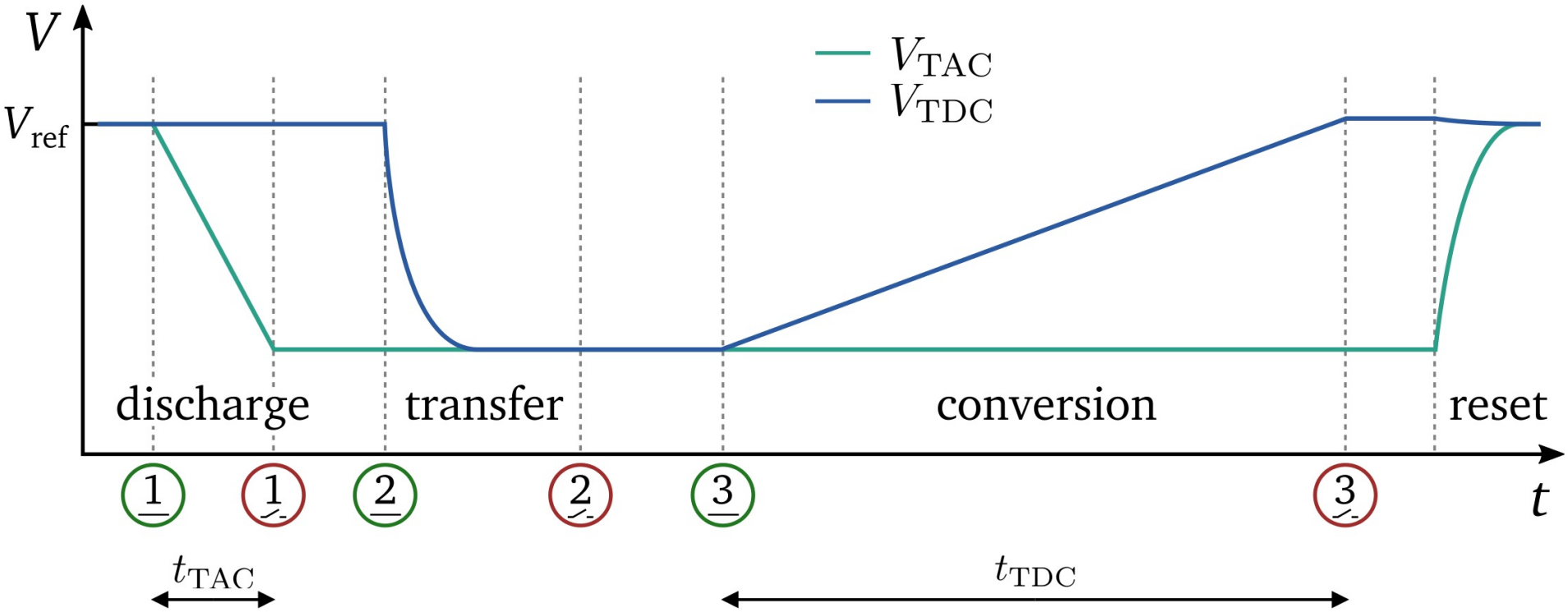
- Readout system (HW/FW/SW) under development (Gießen / Jülich) → lab tests
- Beam test at COSY planned in 2016
- Radiation hardness test: no information on this technology available! TID and SEU tests required





Thank you for your attention!

Time Amplification



$$C_{TDC} = 4 \cdot C_{TAC}$$

$$I_{TDC} = {}^{1}/_{32} \cdot I_{TAC}$$

$$V_{TDC} = V_{TAC} \iff \frac{I_{TDC} \cdot t_{TDC}}{C_{TDC}} = \frac{I_{TAC} \cdot t_{TAC}}{C_{TAC}} \implies t_{TDC} = 128 \cdot t_{TAC}$$